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2-in-1 Diodes with a Contact-Sidewall Structure for Small Pixel Pitch in Silicon-on-Insulator (SOI) Uncooled Infrared (IR) Focal Plane Arrays

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Interest continues to grow in the development of uncooled infrared (IR) focal plane arrays (IRFPAs) for high-resolution imaging using pixel pitch reduction technology. However, this approach causes two serious problems. The first is the reduction of IR responsivity that is caused by decreasing the incident IR ray intensity per pixel area. The second is the nonuniformity of the output DC level in the pixels caused by the increase in the production tolerance influence. Since pixel pitch and sensor performance exhibit an inverse relationship, we need two methods to improve these characteristics. The first is an increase in the conversion efficiencies from IR ray to electric signal. The second is a decrease in the production tolerance influence by improving the sensor structure. We investigated silicon-on-insulator (SOI) diode structures to address this challenge, and proposed a 2-in-1 diode with a contact-sidewall structure, whose key feature is a self-aligning fabrication process that reduces the temperature sensor size without degrading the responsivity and uniformity in the pixels. We fabricated a 17-μm-pixel pitch IRFPA to measure the performance of 2-in-1 diodes with a contact-sidewall structure. This new structure, which reduces the temperature sensor size in the 17-μm-pixel pitch by more than 14% compared with the 2-in-1 diodes used in previous studies, also enables pixel pitch reduction. Under a forward bias constant current of 6 μA, the temperature coefficient of V_f (dV_f/dT) increased to 4.1%, and the standard deviation of the diode forward voltage of the IRFPAs was reduced from 0.123 to 0.057 mV compared with 2-in-1 diodes without a contact-sidewall structure. Our proposed diode structure realizes pixel pitch reduction with increasing IR responsivity, which also improves the pixel uniformity.

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1. Introduction

Interest continues to grow in uncooled IR focal plane arrays (IRFPAs), and the number of pixels in them increases each year. IRFPAs have been applied to high-performance imaging in industrial, home security, defense,[1] and remote sensing systems.[2] Many technologies have been developed for pixel pitch reduction and to increase the number of pixels. Recently, the development of an uncooled IRFPA containing over 1 million pixels at a 17-μm-pixel pitch has been reported.[3–6] However, pixel pitch reduction usually causes two serious problems. The first is a reduction in the IR responsivity caused by reducing the incident IR ray intensity per pixel area. The second is the nonuniformity of the output DC level in the pixels caused by an increase in the production tolerance influence. Therefore, pixel pitch and sensor performance usually have an inverse relationship, and two methods are required to improve these characteristics. The first is the increase in the conversion efficiencies from IR ray to electric signal. The second is the decrease in the production tolerance influence by improving the sensor structure.

We address this technological challenge by proposing a new structure that reduces the pixel pitch, increases the IR responsivity, and improves the uniformity of the output DC level in the pixels.

Although resistive microbolometers are often used as temperature sensors in uncooled IRFPAs, we previously proposed a silicon-on-insulator (SOI) diode as a temperature sensor, in which single-crystal p-n junction diodes are formed in an SOI layer.[7] These single-crystal SOI diodes based on Si-LSI technology promise uniform IR responsivity and high productivity. We developed SOI-diode-based uncooled IRFPAs with 2000 × 1000, 640 × 480, 320 × 240, and 160 × 120 array formats.[8–11] An SOI-diode-based IRFPA with a 15 μm pixel pitch was constructed using 2-in-1 diode and uncooled IRFPA stitching technologies. The 2-in-1 diode technology reduced the SOI diode size more than 15% compared with the conventional p^+n or n^+p diode structure in the same design rule and in the 17-μm-pixel pitch,[10] and achieved uniform IR responsivity. The nonuniformity, defined as the ratio of the standard deviation to the mean value, was less than 1%.[11]

In this paper, we report the development of a new diode structure for further pixel pitch reduction and greater uniformity in the pixels. We fabricated and evaluated test elements to investigate our new diode structure. Furthermore, we fabricated 320 × 240 array format IRFPAs with a 17-μm-pixel pitch using this new diode structure.

2. 2-in-1 Diode Structure

Figure 1 shows the cross-sectional pixel structure of our SOI-diode-based uncooled IRFPA. The p-n junction diodes fabricated in the SOI layer were connected in a series for use as a temperature sensor, which is thermally isolated from the Si substrate by supporting legs that contain the electrical interconnections. The temperature sensor is active when a constant current flows through the diodes under a forward bias condition. The IR absorption system includes two different layers over the temperature sensor.

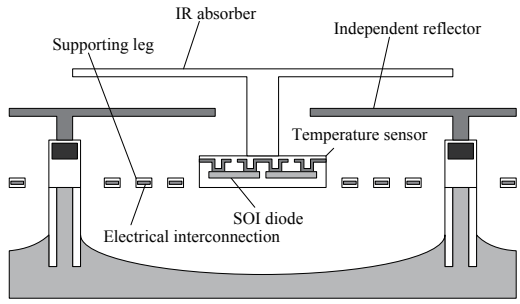

Fig. 1. Cross-sectional pixel structure of SOI-diode-based uncooled IRFPA.

The first layer is an IR absorber that is located at the top of the sensor and is connected to the temperature sensor. The second is an independent reflector located between the temperature sensor and the IR absorber. This reflector is thermally isolated from both the temperature sensor and the IR absorber. An incident IR ray is reflected multiple times between these two layers and efficiently converted into thermal energy at the IR absorber.[12] The thermal energy changes the temperature of the temperature sensor, causing a forward voltage shift of the SOI diodes. Since IR responsivity is proportional to the number of series diodes, the new diode structure that reduces the diode size is the main subject for reducing the pixel size.

Figure 2 shows the cross-sectional schematics of the manufacturing process and the scanning electron microscopy (SEM) surface image of the 2-in-1 diode structure used in previous studies. p^+n and n^+p vertical diodes are formed in the SOI region. The p^+n and n^+p diodes are connected in a series on the surface with a metal interconnection. The 2-in-1 diode structure reduces the SOI diode size of more than 15% compared with the conventional p^+n or n^+p diode structure. This characteristic enabled us to enlarge the number of diodes in a series to improve the IR responsivity. However, this 2-in-1 diode that was previously used has the following two problems:

1) The photolithography superposition margin of clearance C, which is the distance from the p^+ and n^+ contact hole edges to the high-impurity-doping region edges, and clearance D, which is the distance from the high-impurity-doping region edges to the p^- and n^- contact hole edges, must be designed to accommodate the production tolerances. These clearances hinder the reduction of the SOI diode size.
2) Clearances C and D must be long and nonuniform because of the production tolerances. The current in the diode flows across the vertical and lateral p-n junctions. The ratio of the two components depends on the diode structure. When clearances C and D are insufficient for the production fluctuation, the ratio varies. This worsens the effect in the smaller pixel design with the 2-in-1 diode used in previous studies.

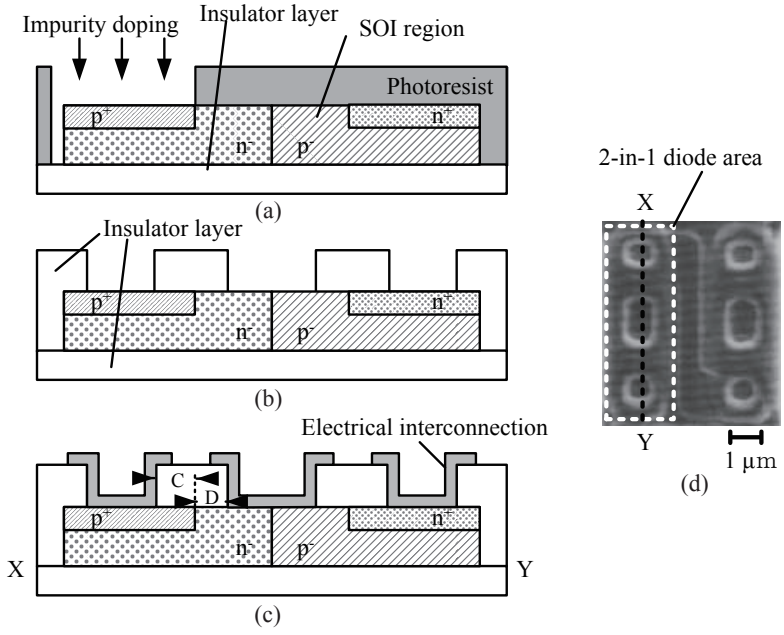

Fig. 2. Cross-sectional schematics of manufacturing process and SEM surface image of 2-in-1 diode structure used in previous studies. (a) Isolation of SOI diode and impurity doping. (b) Fabrication of contact hole by dry etching. (c) Fabrication of electrical interconnection. (d) SEM surface image of 2-in-1 diode structure.

3. Contact-Sidewall Structure

We proposed a new diode structure to reduce the pixel pitch to achieve a more uniform output DC level and called it the 2-in-1 diode with a contact-sidewall structure.

Figure 3 shows the cross-sectional schematics of the manufacturing process of the 2-in-1 diode with a contact-sidewall structure. Its key features are summarized as follows:

1) The p^+ and n^+ impurities are only doped through the contact holes as shown in Fig. 3(b). This is generally called a self-aligning process, which enables restrictions and better control of the high-impurity-doping region.
2) The insulator layer is deposited and anisotropic etching is performed. Because of the anisotropic characteristic of the etching process, the insulator film structure, which is wider near the bottom of the contact hole, is formed on the sidewall of the contact holes as shown in Figs. 3(c) and 3(d). We call this the contact-sidewall structure.

Clearance C', which is the distance from the contact hole edges to the high-impurity-doping region edges in Fig. 3(e), mainly depends on the insulator film's thickness, which is decided by the depth of the contact hole, the thickness of the insulator layer and the

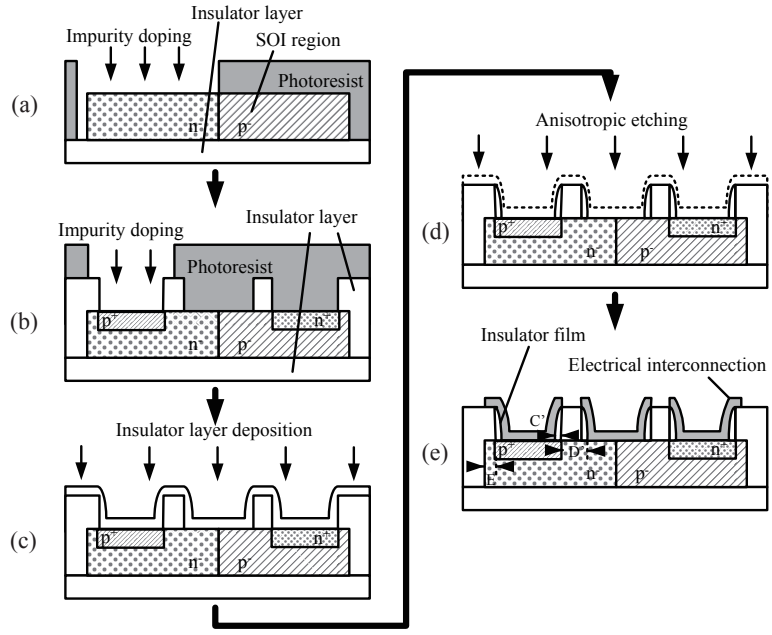

Fig. 3. Cross-sectional schematics of manufacturing process of 2-in-1 diode structure with contact-sidewall structure. (a) Isolation of SOI diode and impurity doping. (b) Fabrication of contact hole by dry etching and high-impurity doping. (c) Insulator layer deposition. (d) Fabrication of insulator film on sidewall of contact holes by anisotropic etching. (e) Fabrication of electrical interconnection.

isotropic etching rate of the anisotropic etching in Figs. 3(c) and 3(d). The production tolerances of these processes should outperform that of the photolithography process. This characteristic leads clearance C' to be shorter and more uniform than clearance C in Fig. 2(c).

The contact-sidewall structure provides two favorable features. The first is that the current flows through the lateral and vertical p-n junctions evenly and uniformly. When clearance C from the contact hole edges to the high-impurity-doping region edges is long and nonuniform, the current path in the SOI diodes is nonuniform. This leads to the nonuniformity of the output DC level in the pixels. Therefore, we can make the output the DC level more uniform by making clearance C' shorter and more uniform.

The second feature is further size reduction of the SOI diodes. We can reduce clearances C and D in Fig. 2(c) when using the 2-in-1 diodes with a contact-sidewall structure. Diode area reduction over 14% can be achieved in the 17-μm-pixel pitch and in the same design rule. Ten series diodes, which are five series of 2-in-1 diodes, can be arranged in a 17 μm pixel by reducing clearance C'.

4. Measurement and Discussion

We fabricated an IRFPA to measure the performances of 2-in-1 diodes with and without a contact-sidewall structure with a 17-μm-pixel pitch and a 320 × 240 array format. These diodes had the same overall dimensions.

4.1 *Improvement of output DC level uniformity*

Figures 4(a) and 4(b) show the evaluated interpixel dispersion of the diode forward voltage calculated from the measured IRFPA 100 × 100 pixel output DC level of the 320 × 240 array format IRFPAs based on 2-in-1 diodes without and with a contact-sidewall structure, respectively. The following are the calculation processes:

1) The dispersion components of the IRFPA output other than pixels are subtracted from the measured values by a calibration process.
2) The interpixel dispersion is measured by the dispersion from the mean voltage value of 100 × 100 pixel.

The standard deviation of the diode forward voltage was reduced from 0.123 to 0.057 mV using the contact-sidewall structure under forward bias conditions with a constant current of 6 μA. This means that the current path becomes more uniform with a contact-sidewall structure.

It is considered that this characteristic is the effect of the reduction and uniformity of clearance C', which is the distance from the contact hole edges to the high-impurity-doping region edges.

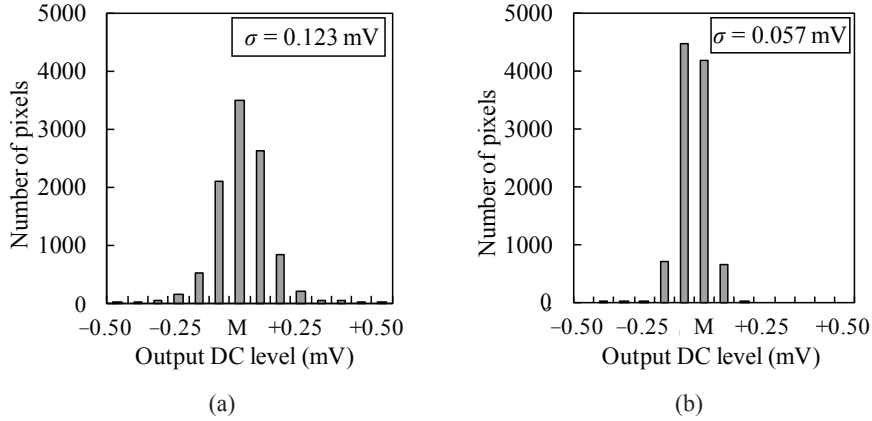

Fig. 4. Interpixel dispersion of diode forward voltage calculated from 100 × 100 output of IRFPAs with a 2-in-1 diode structure (a) without and (b) with contact-sidewall structure. Letter M is mean voltage of 100 × 100 pixel.

4.2 *Improvement of thermal characteristics*

We measured the intrawafer characteristics of V_f, which is the forward voltage of the diodes under the constant current, and the temperature coefficient of V_f (dV_f/dT), and compared the 2-in-1 diode test elements with and without the contact-sidewall structure. Although these diodes were designed to have the same overall dimensions, the 2-in-1 diode with a contact-sidewall structure had 55% downsized high-impurity-doping regions in comparison with the 2-in-1 diode without a contact-sidewall structure because the p^+ and n^+ impurities are only doped through the contact holes. Table 1 shows the average data measured at 36 points in a six-inch wafer. Forward voltage V_f decreased by about 2.3% under forward bias with a constant current of 6 μA, and dV_f/dT increased by about 4.1%.

The *I-V* characteristics of a p-n diode under forward bias are determined as

$$V_f = \frac{k_B T}{q} \ln\left(\frac{I_f}{I_S} + 1\right), \tag{1}$$

where V_f, I_f, and I_S are the forward voltage, forward current, and saturation current, respectively.

For a p^+n diode, I_S is

$$I_S = \frac{A_d \cdot q \cdot D_q \cdot p_{n0}}{L_p}, \tag{2}$$

where A_d, D_p, L_p, and p_{n0} are the effective p-n junction area, diffusion coefficient, minority carrier (hole) diffusion length, and equilibrium hole density on the n-side, respectively.

Under a constant current, dV_f/dT can be expressed as[7]

$$\frac{dV_f}{dT} \cong -\frac{1.21 - V_f}{T}. \tag{3}$$

For the n^+p diode, dV_f/dT can be expressed by a nearly identical equation.

Table 1
V_f and dV_f/dT of 2-in-1 diodes with and without contact-sidewall structure.

Contact-sidewall structure	V_f (V)	dV_f/dT (mV/K)	High-impurity-doping region (%)	Effective p-n junction area (%)
Without	1.594	−2.877	100	100
With	1.557	−2.997	45	135

Thus, the expansion of the effective p-n junction area leads to a reduction in V_f and an increase in dV_f/dT. Table 1 shows that the 2-in-1 diode with a contact-sidewall structure expands the effective p-n junction area by about 35% compared with a 2-in-1 diode without a contact-sidewall structure, as calculated from eqs. (1) and (2).

In short, the current pass becomes wider and the effective p-n junction area increases, despite the reduction in the size of the high-impurity-doping region using a 2-in-1 diode with a contact-sidewall structure.

The considered current path models at the p-n junction of the 2-in-1 diodes with and without a contact-sidewall structure are shown in Fig. 5. The current flows easily through the vertical p-n junction owing to the strong localization of the electric field under the contact hole. However, when the clearances from the contact hole edges to the high-impurity-doping region edges are long, such as without the contact-sidewall structure, the high resistance in the low-impurity-doping region at clearance C restricts the current flows through the vertical p-n junction. Thus, it mainly flows through the lateral p-n junction. In contrast, when the clearances are narrow, such as in the contact-sidewall structure, there is no large difference in resistance between the high- and low-impurity-doping regions at clearance C'. Under this characteristic, the current flows through the vertical p-n junction in addition to the lateral one. The parameter of clearances C and C' is dominant for the current path factor.

A 2-in-1 diode with a contact-sidewall structure is effective for both SOI diode size reduction and IR responsivity increase.

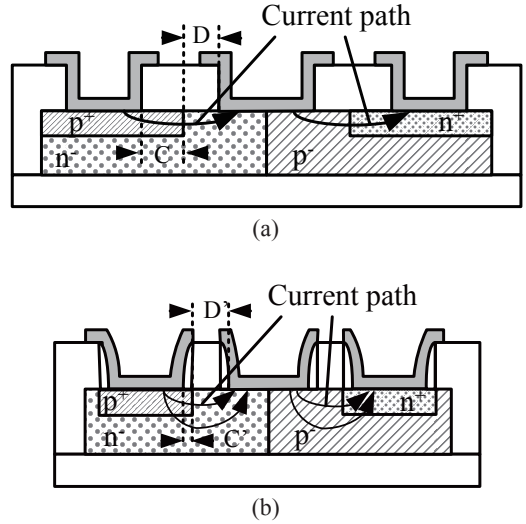

Fig. 5. Schematics of current path at p-n junction of 2-in-1 diodes (a) without and (b) with a contact-sidewall structure.

5. Conclusions

We proposed a 2-in-1 diode with a contact-sidewall structure and fabricated IRFPAs based on 2-in-1 diodes with a contact-sidewall structure, which had a 17-μm-pixel pitch and a 320 × 240 array format, to investigate our proposed diode structure's performance. The measured performances of these IRFPAs demonstrated the following two main results:

1) The standard deviation of the diode forward voltage calculated from the measured IRFPA 100 × 100 pixel output DC level was reduced from 0.123 to 0.057 mV using 2-in-1 diodes with a contact-sidewall structure.
2) Forward voltage V_f decreased by about 2.3%, and the temperature coefficient of V_f(dV_f /dT) increased by about 4.1% under a forward bias with a constant current of 6 μA compared with the 2-in-1 diodes without a contact-sidewall structure.

The high-impurity-doping regions were downsized by about 55%, and the effective p-n junction areas were expanded by about 35% with 2-in-1 diodes with a contact-sidewall structure. Our proposed structure widened the current path and improved the uniformity of the output DC level in the pixels.

It also reduced the SOI diode size by about 14% in the 17-μm-pixel pitch and in the same design rule. This structure achieves an arrangement of ten series of diodes, which are five series of 2-in-1 diodes, in a 17 μm pixel by reducing the SOI diode size.

The contact-sidewall structure is effective for pixel pitch reduction and improving both the IR responsivity and uniformity of the output DC level in the pixels. This is a key technology for high-performance uncooled SOI diode IRFPAs.

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