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Interconnection Characteristics of Rivet Packaging for Radio Frequency Microelectromechanical Systems Applications

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In this paper, we present an alternative method of rivet packaging for radio frequency microelectromechanical system (RF MEMS) devices and evaluate its electrical characteristics. The rivet packaging enables not only encapsulation but also through-via interconnection at the same time. Moreover, it is possible to achieve a wafer-level process. The electrical performance was evaluated using Cu hollow-filled through-via interconnection. The overall insertion loss of the through-via interconnection from the bottom CPW to the top CPW decreased from 0.04 to 0.11 dB at 2 GHz and from 0.06 to 0.23 dB at 5 GHz.

1. Introduction

System-in-Package (SiP) is defined as the vertical stacking of similar or dissimilar ICs with or without embedded active and passive components. Devices must be three-dimensionally (3-D) assembled and interconnected to obtain the smallest volume.(1) To achieve SiP technology, 3-D interconnection technologies, such as 3-D wiring, wireless interconnection, blind vias, and silicon through-vias, required.(2) In particular, the silicon through-via interconnection method is associated with SiP technology, such as the flip chip and the stacking technology.(3) In silicon through-via interconnection, device pads are electrically passed out of the encapsulation along the shortcut of the through-via.

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In the silicon through-via interconnection approach, there are some problems to be addressed.(4–7) The well-known "Bosch process" enables the realization of a high-aspect-ratio silicon through-via structure using the cycles of the combination of isotropic etch, surface protection deposition, and anisotropic etch of the passivation layer. However, a notch is basically generated from the charge build-up on the dielectric surface at the bottom. This notch structure will disturb the electrical interconnection.

Moreover, the silicon through-via structure is filled with a conductive material for the electrical interconnection. The metal-filled silicon through-via structure is mechanically vulnerable to thermal expansion because of the difference in the coefficient of thermal expansion (CTE) between silicon and metal. If it has a seam or an air-void inside, it will show the worst mechanical stability. The failure occurs in the metal-filled silicon through-via.

In particular, the silicon through-via interconnection for RF MEMS package has to not only solve these problems but also have good RF characteristics. It is very important to pass the signal outside with minimal loss using the RF MEMS package. The electrical performance of the packaged device is evaluated on the basis of its characteristic value according to the application. Basically, the average resistance or RF-loss per unit length of the feed through passing from the terminal pads to the final pad can be the representative value.

In this paper, we present not only the rivet packaging method that was previously presented(8,9) but also its electrical characteristics, to solve the problem of silicon through-via, improve RF-loss characteristics, and prove its usefulness.

2. Design and Simulation

2.1 *Rivet packaging*

Rivet packaging uses two types of wafer; one is a male wafer having a relatively thick solder as a donor, the other is a female wafer as an acceptor having structures similar to a mushroom or a through-via structure. The solder as the donor, when it melts, reflows along the wetting layers on under bump metallization (UBM). When it meets on the walls of the female wafer as the acceptor, the sidewall bonding begins and stops at the corner of the wall owing to the absence of a wetting layer as described in Fig. 1. Finally, the end of the solder become spherical owing to the tendency to minimize the surface energy, and consequently, generates a rivet structure. Therefore, in rivet packaging, both the encapsulation of the mushroom structure and the electrical interconnection of the through-via are simultaneously achieved.

2.2 *Design*

The proof-of-concept structure is shown in Fig. 2. The electrical performance of the rivet packaging method is studied using the coplanar waveguide (CPW)-to-CPW transition with a Cu hollow-filled through-via. The signal lines and ground lines on both wafers are designed to provide the characteristic impedance of 50 Ω. The two wafers are high-resistivity silicon (HRS, 300 μm thick, > 20,000 Ω·cm), which were chosen owing to their ease of processing, excellent mechanical properties, and good electrical

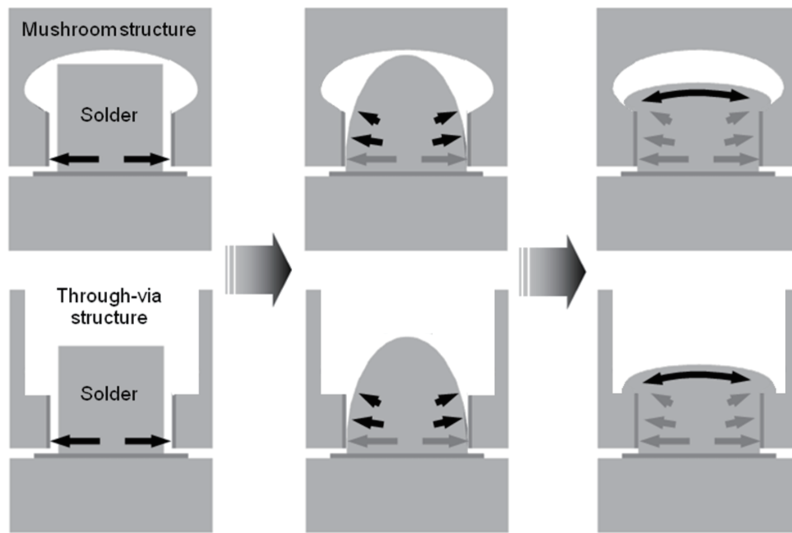

Fig. 1. Concept of the rivet packaging: the solder as the donor, and the mushroom and through-via structures as the acceptors.

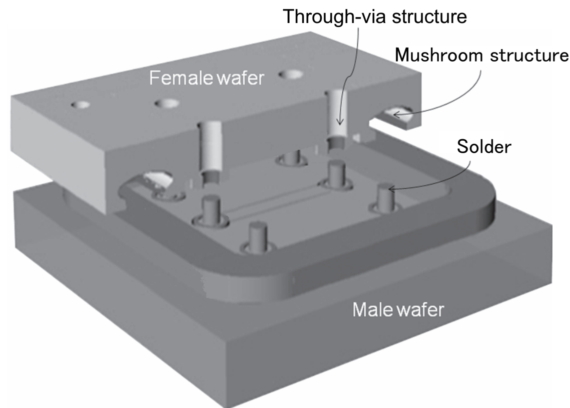

Fig. 2. Schematic of the rivet packaging.

performance.[10] The CPW line was an electrically interconnected through-via obtained by the rivet packaging method. The RF signal of the CPW line goes from the input port to the output port through the Cu hollow-filled through-via, as shown in Fig. 3.

The layout of the male wafer is shown in Fig. 4. The layout of the female wafer and its cross-sectional design are shown in Figs. 5 and 6, respectively. The CPW on the male wafer is composed of several layers of Ti (0.1 μm)/Ni (0.5 μm)/Au (0.4 μm evaporated)/Au (3 μm electroplated) and an antiwet layer of Ti (0.1 μm). Then, a pure Sn solder

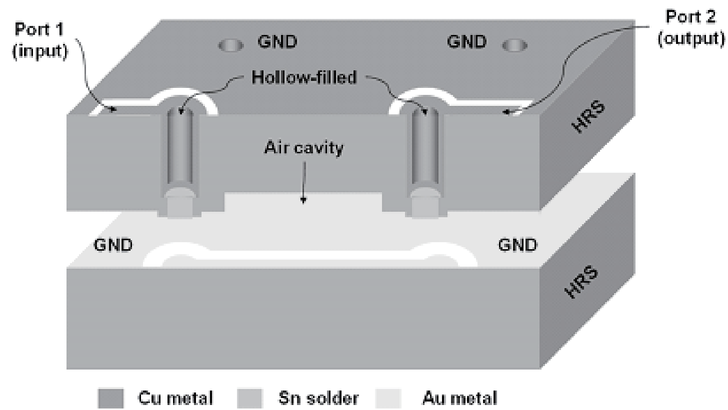

Fig. 3. Schematic of CPW-to-CPW transition with Cu hollow-filled through-via interconnection.

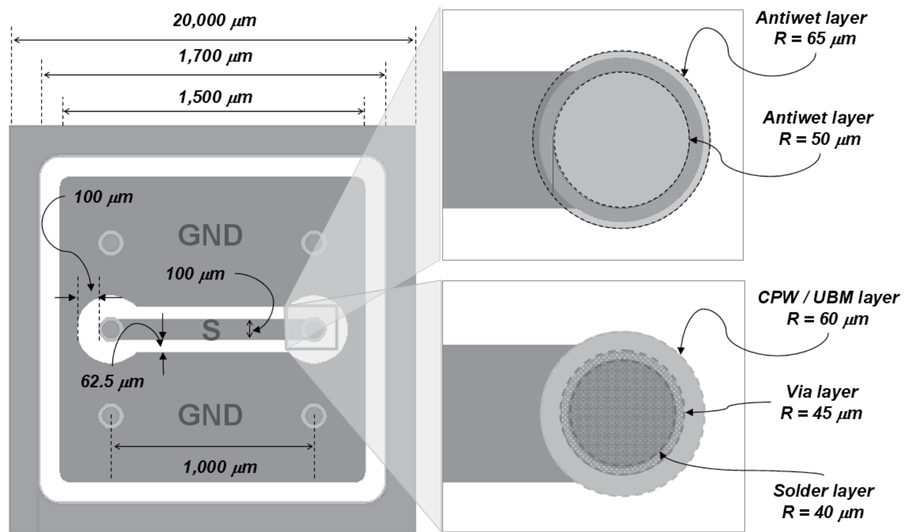

Fig. 4. Mask layout of the male wafer.

of about 70 μm height is electroplated for the reflow process. The antiwet layer was designed to be of 15 μm width restricts the solder reflow. The radius of the Sn solder region was designed to be 5 μm shorter than that of the through-via, and the inner radius of the anti-wet layer was 5 μm longer. The length of the signal line between the input and output ports was 1 mm, and the ground plane was 4 mm^2 in total.

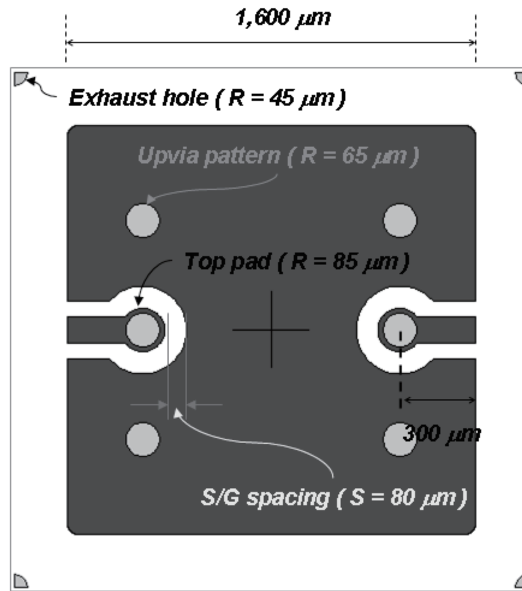

Fig. 5. Mask layout of the top electrode.

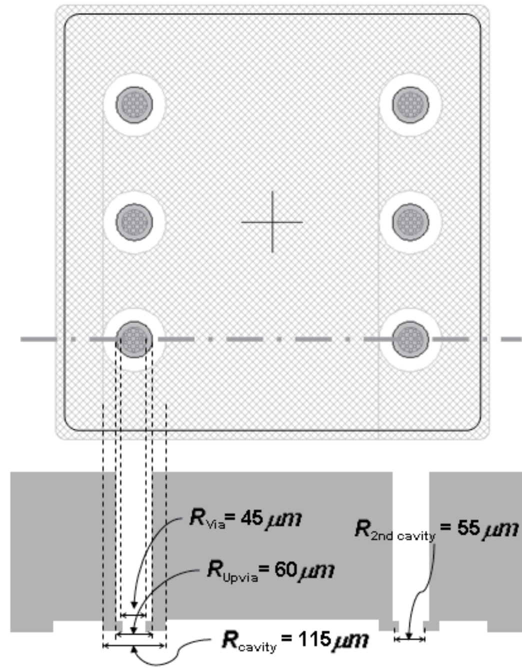

Fig. 6. Mask layout and cross section (through-via design) of the female wafer.

2.3 *Simulation*

The physical structure was simulated using the full 3-D software of Ansoft's High-Frequency Structure Simulator (HFSS). The 3-D model of HFSS is shown in Fig. 7, and the ports were matched to a characteristic impedance of 50 Ω. The CPW configurations were designed for operation from 1 to 10 GHz.

The simulation results are shown in Fig. 11. The results of CPW and the rivet-packaged CPW showed that the presence of the through-via caused mismatches between CPW transitions and then decreased insertion loss, owing to the presence of parasitic inductance and capacitance.

3. Fabrication of Wafers

The fabrication of the male and female wafers is based on a previously reported paper.(9) The process flow of rivet packaging is shown in Fig. 8. The mushroom structure in the seal line and the through-via structure are fabricated on the female wafer, and a pure Sn solder of about 70 μm height is electroplated on the male wafer. The through-via and pure Sn solder are successfully fabricated, as shown in Fig. 9. Two wafers are assembled into a rivet formation with appropriate force applied and then heated to 250°C in N_2 atmosphere. They are bonded following the principle of solder-reflow phenomena for making rivet structures. SEM images of the rivet package are shown in Fig. 10. The solder has a dome shape, which indicates that riveting using a solder is successfully achieved. The top electrode is fabricated by Cu electroplating using DFR photolithography on the bonded wafer. The through-via is also electroplated simultaneously at 20 μm thickness.

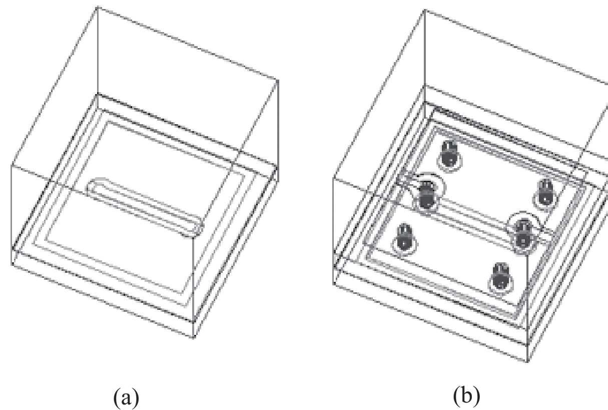

Fig. 7. HFSS physical models of (a) CPW line and (b) PKG with CPW line.

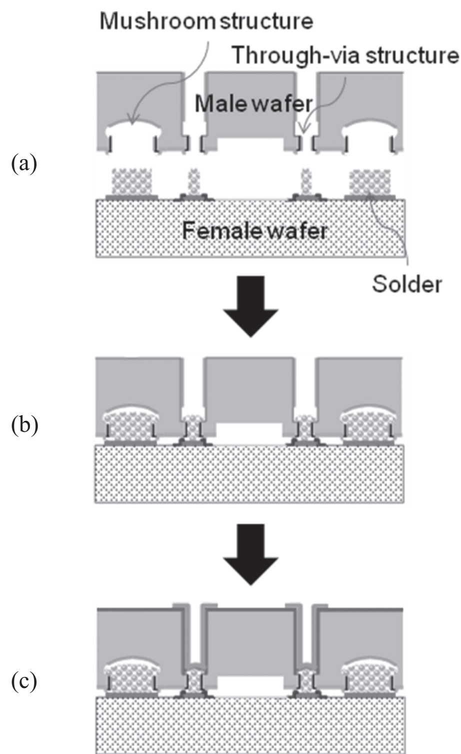

Fig. 8. Process flow of the rivet packaging: alignment of female and male wafers, solder reflow, Cu electroplating.

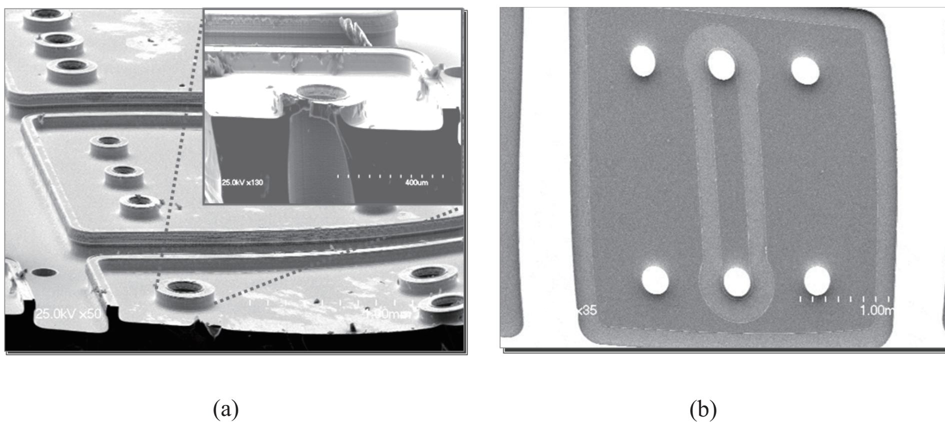

Fig. 9. SEM images of fabricated female and male wafers.

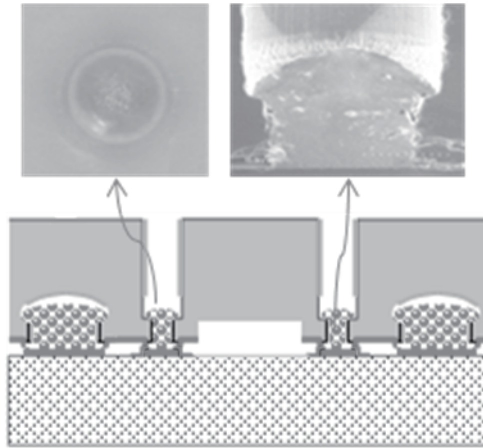

Fig. 10. SEM images of rivet bonding.

4. Results and Discussion

4.1 *Measurement results*

The measurement results are shown in Fig. 11. The fabricated CPW lines had an insertion loss of 0.1 dB up to 10 GHz. However, the overall insertion loss of the through-via interconnection decreased from 0.04 to 0.11 dB at 2 GHz and from 0.06 to 0.23 dB at 5 GHz. The higher the frequency, the larger the decrease in insertion loss. It is considered that the decrease resulted from the impedance mismatch caused by the parasitic inductance and capacitance of the through-via.

4.2 *Discussion*

Considering its insertion loss per unit millimeter, the results are valuable for application in RF-MEMS. However, at high frequencies, a better matching network for the design of through-vias must be investigated. The through-via design has to be compensated for by introducing appropriate capacitance at the transition point.

The measured S-parameter S21 agreed well with the simulated results from HFSS. Consequently, this result showed that HRS has merits as a suitable substrate for devices operating within microwave frequencies. Moreover, it is noted that the Sn solder material and the through-via size do not considerably affect the RF characteristics because the very thick Cu metal with high conductivity does not markedly affect the decrease in the insertion loss.

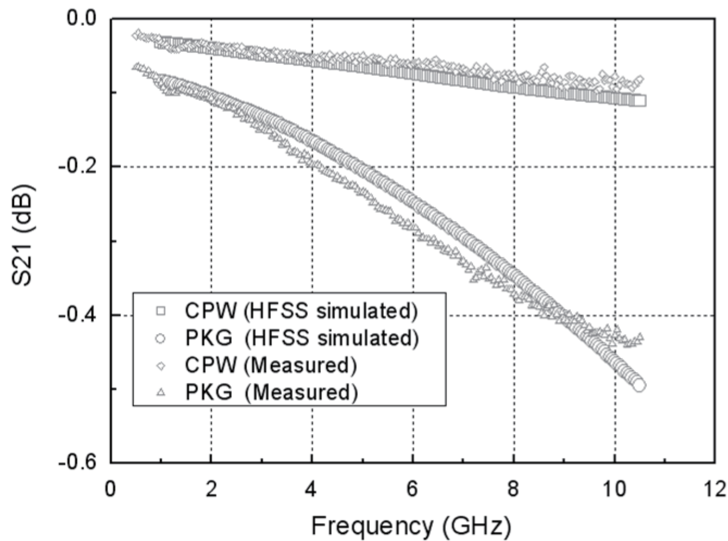

Fig. 11. Simulation and measurement results of CPW lines and PKG with CPW lines.

5. Conclusions

We successfully demonstrated an alternative packaging method, namely, the "rivet packaging method" for MEMS packages. It enables not only encapsulation but also through-via interconnection simultaneously. The electrical performance was evaluated using a Cu hollow-filled through-via interconnection. It was simulated by HFSS and measured using a network analyzer. The measured S-parameter S21 agreed well with the simulation results from HFSS. The overall insertion loss of the through-via interconnection from the bottom to the top CPW decreased. Considering its insertion loss per unit millimeter, the results are valuable for application in RF-MEMS. However, at high frequency, a better matching network for through-vias must be designed, which can be compensated for by introducing appropriate capacitance at the transition point.

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