

# Fabrication of Room-Temperature-Operating Carbon Nanotube Single-Charge Transistors

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Single-electron and single-hole transistors (SETs/SHTs) using carbon nanotube field-effect transistors (CNT-FETs) have promising practical applications owing to their unique electrical characteristics and potential for room-temperature operation. To realize a charging energy larger than the thermal energy, very small islands are necessary on a carbon nanotube channel. In this article, we review two recent challenges in fabricating room-temperature-operating CNT-SETs/SHTs. One is the introduction of defects into the carbon nanotube channel surface, and the other is the realization of a CNT-FET with an extremely small channel length. All the devices described here clearly show Coulomb oscillations even at room temperature. Room-temperature-operating CNT-SETs/SHTs are expected for applications in logic circuits and high-sensitivity chemical sensors.

## 1. Introduction

Carbon nanotubes (CNTs) are very attractive materials owing to their unique electrical characteristics and ideal one-dimensional structure.<sup>(1,2)</sup> In recent decades, there have been many reports on carbon nanotube field-effect transistors (CNT-FETs).<sup>(3–7)</sup> High-sensitivity chemical sensor applications using CNT-FETs are one of the most promising fields. In fact, many biosensors and gas sensors using CNT-FETs have been extensively investigated.<sup>(8–12)</sup> For more high-sensitivity sensor applications, the realization of room-temperature-operating single-electron/single-hole transistors (SETs/SHTs) is crucial.

The above-mentioned single-charge transistors (SCT) consist of three electrodes and one island, as shown in Fig. 1. To travel from the source electrode to the drain electrode,

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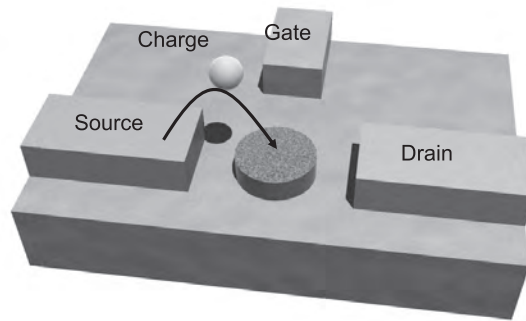


Fig. 1. Schematic illustration of quantum tunneling for charge between source and drain electrodes through intermediate island.

the charge must pass through the island. If the charge travels from the source electrode to the drain electrode by quantum tunneling, it can be blocked by the electrostatic energy of a single excess charge on the island (Coulomb blockade).

There are two requirements for single charge tunneling: (1) the tunneling resistance should exceed the quantum resistance ( $R_T \gg R_Q = h/e^2 = 25.8 \text{ k}\Omega$ ) and (2) the charging energy in single quantum wells should markedly exceed the thermal energy ( $E_C \gg k_B T$ ,  $k_B$ : Boltzmann constant,  $T$ : absolute temperature).<sup>(13)</sup> Since the contact resistance between SWNT channels and electrodes tends to be rather high (several tens of  $\text{k}\Omega$  to several  $\text{M}\Omega$ ),<sup>(14)</sup> the former requirement is comparatively easy to meet. On the other hand, the realization of a large charging energy is very difficult.

The charging energy of a single island is expressed as  $E_C = e^2/(2C_\Sigma)$ , where  $C_\Sigma$  is the total capacitance of the system. Here,  $C_\Sigma$  is given by  $C_\Sigma = C_G + C_S + C_D$ , where  $C_G$  is the gate capacitance, and  $C_S$  and  $C_D$  are the source and drain tunnel capacitances, respectively. For the SETs/SHTs to operate at room temperature,  $C_\Sigma$  must be much smaller than 3 aF ( $\sim 10^{-18} \text{ F}$ ). Therefore, an SWNT is a very suitable channel material for a single-charge island owing to its small diameter ( $\sim 1 \text{ nm}$ ).

If the environmental contributions around an SWNT channel such as water and residual contamination are neglected,  $C_G$  is expressed as  $C_G = 2\pi\epsilon_r\epsilon_0 L/\ln(2l/d)$  in a simple cylinder model, where  $d$  and  $L$  are the diameter and length of the SWNT channel, and  $\epsilon_r$  and  $l$  are the relative permittivity and thickness of the gate insulator, respectively. Therefore, a small channel length (less than 50 nm) is necessary for a small gate capacitance.

Tunnel capacitance, however, has complicated features. It has been considered to originate from the Schottky barrier between SWNT channels and electrodes. However, since such a Schottky barrier depends on the electrode metal material (i.e., work functions of the metal) and the diameter of SWNT channels and environmental molecules ( $\text{O}_2$  or  $\text{H}_2\text{O}$ ), the control of tunnel capacitance is difficult.

Generally, there are two techniques for fabricating CNT-SCTs. One is the use of defect-introduced CNT-FETs,<sup>(15–19)</sup> and the other is the use of CNT-FETs with a very small channel width.<sup>(20–23)</sup> Although the defect-introduced CNT-FETs showed SCT's phenomena even at room temperature, their stability and reproducibility is rather poor. CNT-FETs with a small channel width showed SCT's phenomena only at low temperatures (<80 K).<sup>(20–22)</sup>

In this article, we describe the fabrication techniques for CNT-SCTs operated at room temperature. In this review, we discuss the technology and characteristics of carbon nanotube SCTs, with particular reference to related works carried out in our laboratory. At first, CNT-FETs with defects introduced onto the SWNT surface by oxygen plasma irradiation<sup>(18)</sup> and focused-ion beam (FIB)<sup>(17)</sup> are described. Then, CNT-FETs with a very small channel width formed by a shadow evaporation method<sup>(23)</sup> are described.

## 2. Defect-Introduced CNT-SCTs

In this section, we describe defect-introduced CNT-FETs. In methods using these CNT-FETs, the SWNT channel is nicked or cut by oxygen plasma and FIB irradiation. CNT-FETs show clear room-temperature-operation of SCTs.

### 2.1 Defect-induced plasma process

Figure 2(a) shows a schematic illustration of the devices fabricated by a defect-induced plasma process (DIPP). The devices were fabricated on SiO<sub>2</sub>/Si substrates. First, a patterned Si (10 nm)/Mo (10 nm)/Fe (5 nm) catalyst layer was formed, and SWNT channels were grown by thermal chemical vapor deposition using ethanol as a carbon source. Next, to prevent hysteresis, the devices were annealed at 200°C for 8 h. The source and drain electrodes (Ti/Pt) were formed after a 1-nm-thick Ti layer was deposited on the substrate surface to entirely cover the CNT channel and protect it against contamination. Then 1-nm-thick Ti layer was oxidized at 300°C for 1 h in air ambient. Another protection film, that is, a 45-nm-thick SiO<sub>2</sub> layer, was deposited on the surface of the samples. Finally, O<sub>2</sub> plasma was irradiated onto the CNT channel under fixed conditions (O<sub>2</sub>: 60 sccm, 100 W, 10 s) using reactive-ion etching (RIE). Heavily doped Si substrates were also used as a back-gate electrode. We expect several defects to be introduced onto the surface of SWNTs.

Figure 2(b) shows the typical drain current ( $I_D$ ) – back-gate voltage ( $V_{BG}$ ) characteristics of the devices before DIPP obtained at 290 K. They showed typical *p*-type CNT-FET characteristics. However,  $I_D$  oscillated against  $V_{BG}$  for the device after DIPP, as shown in Fig. 2(c). The oscillation peaks were almost the same for all drain voltages ( $V_D$ ), indicating the effect of Coulomb blockade. The Coulomb oscillation peak period, however, showed no periodic characteristics, indicating multi-quantum-dot type SCTs. Figure 2(d) shows a contour plot of  $I_D$  as a function of  $V_{BG}$  and  $V_D$  for the device after DIPP. The red areas correspond to current-suppressed region, i.e., the Coulomb gap region, which exhibits the clear Coulomb diamond structures. It is considered that some Coulomb diamonds have piled-up structures, resulting from the formation of the multi-quantum dots in the CNT channel.

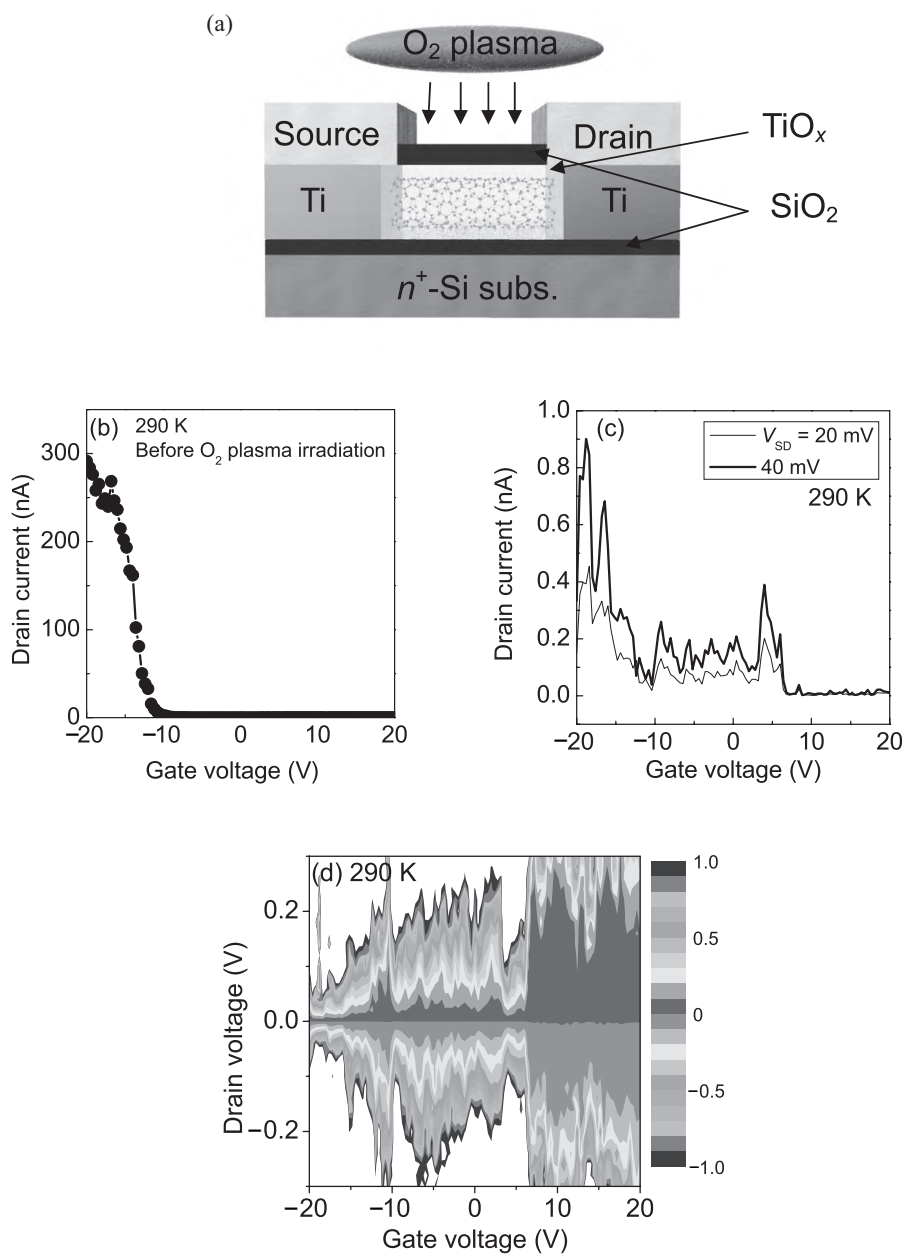


Fig. 2. (a) Schematic cross section of sample under  $O_2$  plasma irradiation; (b)  $I_D$  vs  $V_{BG}$  characteristics at 290 K before  $O_2$  plasma irradiation at drain voltage of 1 V; (c)  $I_D$  vs  $V_{BG}$  characteristics at 290 K after  $O_2$  plasma irradiation for drain voltages of 0.02 (thin solid line) and 0.04 V (thick solid line); and (d) contour plots of  $I_D$  at 290 K as a function of  $V_{SD}$  and  $V_{BG}$  after  $O_2$  plasma irradiation.

## 2.2 Damage by FIB

Next, we describe another defect-introduced technique. FIB techniques have been used for nanofabrication processes because they enable the focusing of ion beams and their irradiation at precise positions on the nanoscale order. By controlling the dose of the ion beam irradiated, two damaged regions can be introduced into an SWNT channel at precise positions using an FIB technique, as shown in Fig. 3(a). Then, these damaged regions are expected to act as tunnel barriers, thereby forming a quantum dot device.

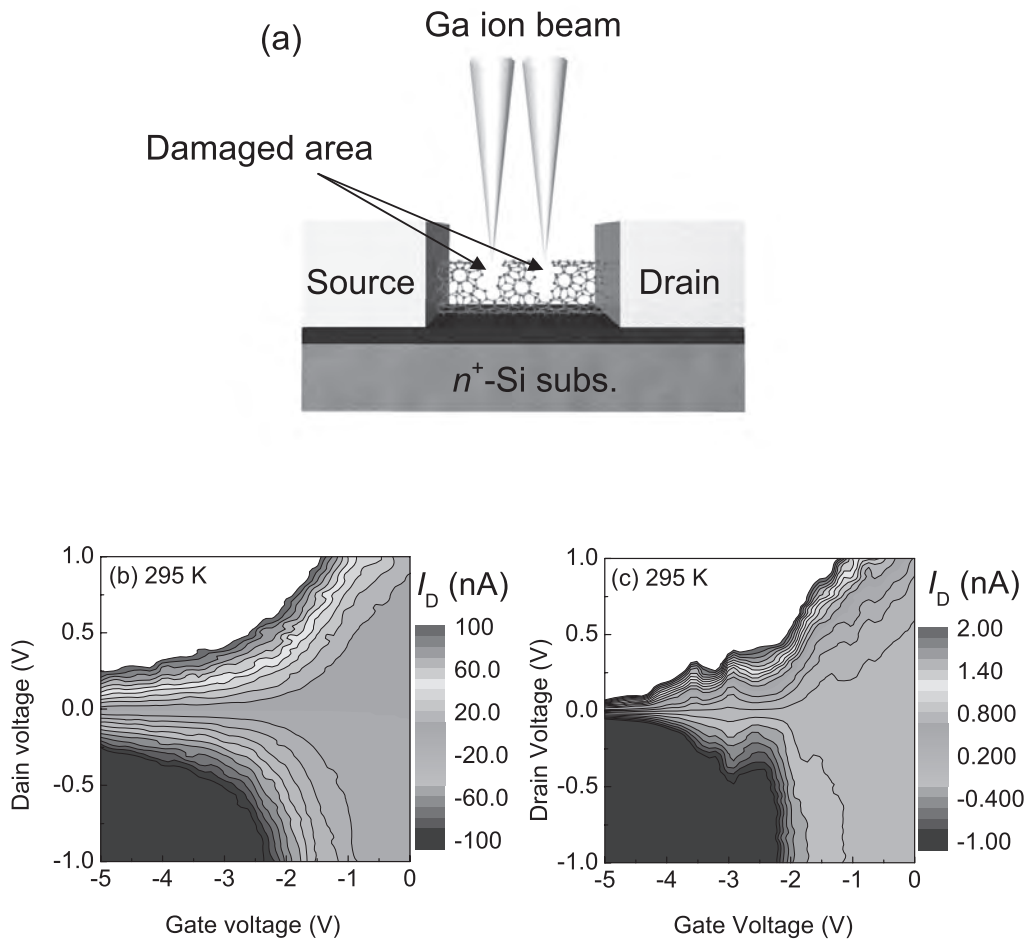


Fig. 3. (a) Schematic illustration of fabrication of single quantum dot in SWNT channel using FIB technique and contour plots of source-drain current at 295 K as a function of  $V_{SD}$  and  $V_{BG}$  (b) before and (c) after irradiation of focused Ga ion beam.

Therefore, we controlled the size and number of islands formed in an SWNT channel. In this section, we described a CNT-FET having an SWNT channel. Subsequently, two tunnel barriers with a separation of 50 nm were introduced into the SWNT channel by irradiating ion beams using an FIB technique. The acceleration voltage and diameter of the Ga-ion beam were 30 kV and 5 nm, respectively. A Ga ion dose of  $3 \times 10^{14} \text{ cm}^{-2}$  was used to fabricate a single quantum dot in an SWNT channel. According to the diameters of the Ga-ion beam (5 nm) and SWNTs (1–2 nm), the total number of irradiated Ga ions at  $3 \times 10^{14} \text{ cm}^{-2}$  is estimated to be approximately 15–30. Finally, the electrical transport properties of the fabricated device were determined.

Figures 3(b) and 3(c) show the contour plots of  $I_D$  at room temperature as a function of  $V_{SD}$  and  $V_{BG}$  before and after irradiation of the focused Ga ion beam, respectively. Before the Ga ion beam irradiation, the absolute value of  $I_D$  decreases with increasing  $V_{BG}$ , as shown in Fig. 3(b). This result indicates that typical *p*-type characteristics are obtained for CNT-FETs. On the other hand, after the introduction of two damaged regions with a separation of 50 nm into the SWNT channel using an FIB technique,  $I_D$  markedly decreased, as shown in Fig. 3(c). When  $V_{SD}$  and  $V_{BG}$  are 1 and 0 V, respectively, the difference in  $I_D$  is estimated to be approximately 2% of its original value, owing to the formation of two damaged regions in the SWNT channel by an FIB process. The contour plot shown in Fig. 3(c) reveals that the device basically maintains *p*-type characteristics, but  $I_D$  is suppressed when the  $V_{SD}$  is very small, and  $I_D$  is modulated by  $V_{BG}$  at room temperature.

### 3. CNT-SCTs with Very Small Channel Width

Although the CNT-SCTs described in §2 showed Coulomb oscillation and Coulomb diamond characteristics even at room temperature, their stability and reproducibility were rather poor owing to the defect introduced into the SWNT channel. To fabricate “stable” CNT-SCTs, it is necessary to realize defect-free CNT-SCTs. However, it is very difficult to fabricate a structure less than 50 nm in size even by electron beam lithography. In this section, we describe the CNT-SCTs fabricated by a shadow evaporation method at a small gate capacitance, and the insulator inserted between the SWNT channel and the electrodes at small tunnel capacitances.

We will focus on two devices, namely, CNT-FETs A and B, which were fabricated on a  $\text{SiO}_2/\text{Si}$  substrate. After SWNT growth by thermal chemical vapor deposition, a 1.5-nm-thick aluminum layer was deposited and naturally oxidized at room temperature for 24 h (CNT-FET A). Next, source electrodes made of Ti/Pd (1/30 nm) were formed by conventional photolithography and the lift-off method. Although drain electrodes were defined by a similar procedure, the substrate was angled, as shown in the inset of Fig. 4, such that the drain electrodes were partially shadowed by the source electrodes during evaporation. In the procedure, the electrode separation can be extremely small. Figure 4 shows a SEM image of the device fabricated by a shadow evaporation method.

Figures 5(a) and 5(b) show plots of  $I_D$  as a function of  $V_{BG}$  at 295 K for CNT-FETs A and B, respectively. The drain currents of both devices increased with decreasing  $V_{BG}$ , indicating *p*-type CNT-FET characteristics. CNT-FET B showed general *p*-type FET

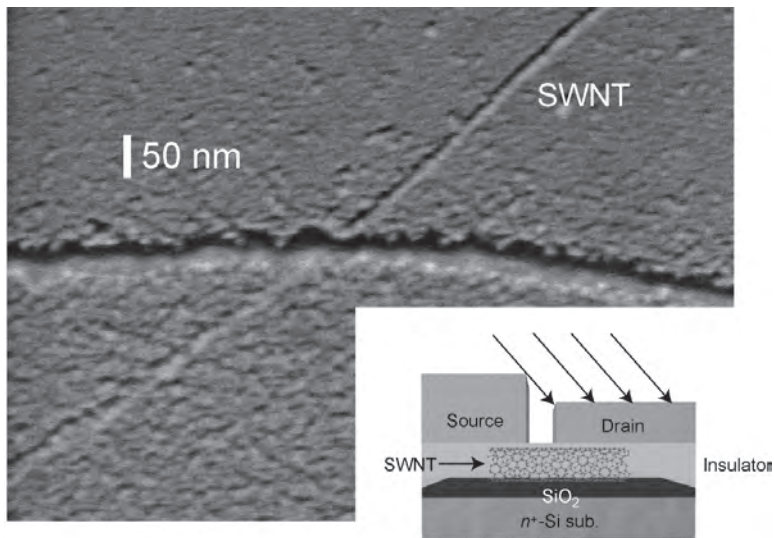


Fig. 4. SEM image of CNT-FETs fabricated by shadow evaporation method. The inset shows a schematic illustration of the devices.

characteristics, as shown in Fig. 5(b). This result agrees with other reports on CNT-FETs with nanogap electrodes. In contrast, the  $I_D$  of CNT-FET A apparently oscillated with  $V_{BG}$  even at room temperature, as shown in Fig. 5(a). The drain current peak positions are almost the same for all drain voltages owing to the Coulomb blockade effect. The inset of Fig. 5(a) shows  $I_D$  plotted against source-drain voltage for  $V_{BG}$  values of  $-20$  and  $-13.2$  V, which represent the no-blockade and blockade conditions, respectively. An approximately  $0.25$  V wide blockade gap can be observed. These results indicate that the inserted insulator is effective for realizing room-temperature-operating CNT-SCTs. These results indicate that tunnel capacitances derived using the Schottky barrier are larger than those of defects on the SWNT surface. The CNT-SCTs showed very stable operation at room temperature and good reproducibility.

#### 4. Conclusion

The realization of the room-temperature operated CNT-SCTs has great impact owing to their broad applications such as in logic circuit and high-sensitivity chemical sensors. In this review, we aimed to discuss the fabrication process of room-temperature-operating CNT-SCTs. Three types of CNT-SCT operating at room temperature were described. The defect-introduced CNT-SCTs were fabricated by oxygen plasma irradiation and a focused-ion beam technique. The former devices have several defects on the SWNT surface, and the latter devices have two defects separated by approximately  $50$  nm.

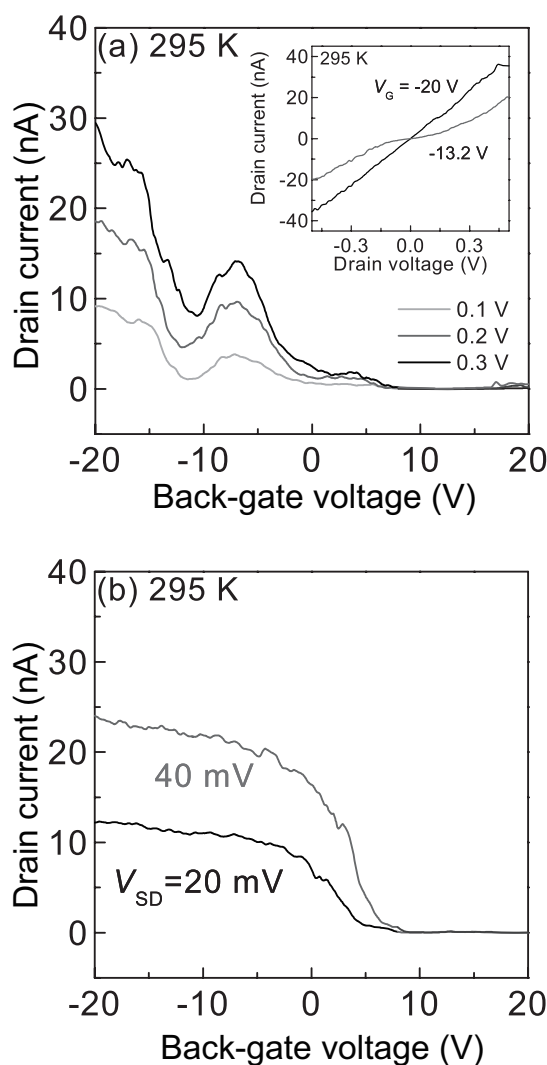


Fig. 5. Plots of drain current as a function of gate voltage for CNT-FETs A (a) and B (b). The inset of (a) shows the  $I_D$  vs  $V_{SD}$  characteristics for gate voltages of  $-20$  and  $-13.2$  V.

Although they showed the room-temperature operation of the SCTs, their stability and reproducibility were rather poor owing to their defects and complex fabrication processes. Therefore, CNT-FETs with a very small channel length ( $\sim 20$  nm) were fabricated by a shadow evaporation method. They showed stable SCT operation at room temperature. These room-temperature-operating CNT-SCTs have high potential for various practical applications such as in logic circuits and high-sensitivity chemical sensors.



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