New Microlink Structures for CMOS-Compatible Thermopiles

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A highly sensitive infrared (IR) detector requires a large absorption area and a low thermal conductance to maximize the temperature change and signal induced by the incident IR radiation. For the floating membrane of a microsensor, it is difficult to form a large area with suitable front-side etching windows at the same time. A new idea of improving complementary metal-oxide-semiconductor (CMOS) thermopile performance for a floating membrane with a large area is introduced to increase the absorption area, which is constructed by a series of microlinks between each quarter of the membrane. The design and fabrication of the proposed microlink-based thermopiles are realized using 1.2 μm CMOS IC technology combined with subsequent anisotropic front-side etching. Four V-groove etching windows were opened by a CMOS process, and then using tetramethylammonium hydroxide (TMAH) etching solution, the silicon substrate was etched along the <100> directions. Finally an Al/n-polysilicon thermopile was embedded in an oxide/nitride membrane. Our large floating membrane has an area of 1300×1300 μm² and is 2 μm thick. The floating membrane of the thermopile was formed using four anisotropic etching windows with each quarter of the membrane connected with its nearest membranes. Therefore, the area of the proposed membrane is increased greatly; thus, it absorbs more IR radiation than the conventional design and markedly enhances responsivity. To evaluate the performance of the proposed microlink-based thermopiles, the output voltage frequency response was measured and compared with that of a conventional thermopile. The surface morphology measurement of a proposed thermopile is implemented to evaluate the effect of residual stress and characterize the geometric shape of the membrane practically. The results of etching and the breakage of the microlink-based thermopiles are discussed.

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1.   Introduction

Complementary metal-oxide-semiconductor (CMOS)-compatible techniques have been investigated and successfully applied to microsensors in recent years.[1] Prototypes of certain thermal, mechanical and chemical sensors have been obtained by combining CMOS IC technology with postprocessing steps specific to the sensor function and compatible with the IC process. Thermal microsensors, which can also be fabricated by a micromachining process, have played an important role in the exploration of IR radiation applications.

A serially interconnected array of thermocouples forms a thermopile, which is one type of thermal microsensor. The thermocouple array is placed across the hot and cold regions of a structure, and the hot junctions are thermally isolated from the cold junctions. The cold junctions are typically placed on the silicon substrate to provide an effective heat sink while the hot junctions are formed over a thin diaphragm that effectively thermally isolates the hot junctions from the cold junctions. In the hot region, there is a black body for absorbing the IR energy, which raises the temperature according to the intensity of the incident IR energy. The thermopile shows an inherently stable response to DC radiation and is not sensitive to ambient temperature variations. It also responds to a broad IR spectrum and does not require a source of bias voltage or current.

Since thermal sensors are usually used to detect thermal radiation and are strongly affected by their thermal conductance properties, it is important to design a thermal microsensor with a low solid thermal conductance and a large active area to absorb more radiation energy. In the experiment of Du and Lee, using a geometric design of the parameters, namely, the width of polysilicon, the length of the thermopile, and the number of thermocouples, heat conductance was measured by applied bias heating. The results show a very strong correlation between the membrane area of the thermopile and the heat conductance.[2] Usually, it is desirable to increase the fill factor of the membrane area, which can be placed more thermocouples so as to give larger output. In this study, we report a high-fill-factor thermopile using a new proposed structure, referred to as a microlink.

To form the membrane, etching windows are opened by a CMOS process and a post-CMOS process. Then, using an etching solution, the silicon substrate is etched along the <100> directions. The central part of the silicon substrate beneath the masked membrane is removed and only a thin layer is left on top, which floats on the substrate. Nevertheless, it is generally very time-consuming and difficult to remove the substrate cleanly to form a floating membrane. Using a microlink structure, this problem can be improved.

During the etching process, stress-compensation techniques have been used in most studies to overcome the failure to form a large membrane.[3–10] Unfortunately, such techniques are not suitable for a wide range of MEMS devices fabricated by the standard CMOS process. Nevertheless, it is easy and efficient to connect and link different membranes with several microlinks. We have successfully used a microlink structure that is compatible with the CMOS process.

In this study, we propose a new microlink structure. This can not only improve CMOS thermopile performance by increasing the absorption area but also enable the formation of suitable etching windows so that the substrate beneath the floating membrane can be etched greatly and effectively. The membrane consists of a series of microlinks between each quarter of the membrane to form a single sensor. A number of microsensors such as a single sensor and a sensor array are fabricated successfully by careful design. Nevertheless, the substrate of the microlink-based sensor is etched away completely and leaving a hollow cavity at the bottom. The etching efficiency for the microlink-based thermopiles is very high.

2.   CMOS-compatible Sensors with Microlink Structures

IR sensors are important elements in a number of electronic applications. Silicon-based microfabrication in its present state could form the technological foundation for the inexpensive implementation of complete adaptive microsensors. However, most of these sensors are not fabricated by CMOS-compatible processes and require additional special fabrication conditions, which lead to greater difficulty in commercialization. The basic advantages of silicon are its compatibility with standard CMOS processes, its high reliability and temperature stability as well as the easy integration of additional signal-processing electronics. On the basis of CMOS-compatible processes, we have developed thermopiles with many pairs of thermocouples, which give a voltage signal when IR radiation impinges on the active area of the sensor.

Various materials have been used in CMOS processes; these materials include bulk silicon; n-polysilicon and p-polysilicon; dielectrics made of silicon oxide, silicon nitride or passivation material; and metal, which is usually an alloy with aluminum. All these materials can serve as thermal mass. For conducting heat, silicon and metal are efficient. The dielectric layers provide only moderate thermal isolation owing to their small thicknesses. In addition, the removal of material by micromachining is required for efficient thermal isolation.[11] In standard CMOS processes, metal, polysilicon and diffused bulk silicon can serve as thermocouple materials. We can use metal/polysilicon and n-polysilicon/p-polysilicon thermocouples to form a sandwich structure between the CMOS dielectric layers.[12]

The difference in Seebeck coefficient between different conducting CMOS materials, which include different types of doped silicon, is the basis of integrated thermocouples and thermopiles. The relative Seebeck coefficient, α_{ab}, between two materials a and b forming the thermocouple is used to describe thermocouple performance and the optimum figure of merit Z_{opt} defined as

$$Z_{opt} = \alpha_{ab}^2 \left[\left(\rho_a \kappa_a \right)^{1/2} + \left(\rho_b \kappa_b \right)^{1/2} \right]^{-2}, \qquad (1)$$

where ρ_a and ρ_b are the electrical resistivities and κ_a and κ_b are the thermal conductivities of the two materials.[12] Values of these two parameters for the various combinations of CMOS metal and polysilicon for a specific process have been suggested.[12] The

thermal properties of silicon depend on doping and structure regardless of whether it is monocrystalline or polycrystalline. The temperature coefficient of the resistivity of polysilicon can be positive or negative, depending on doping. All material properties are temperature-dependent. Moreover, the material properties are process-dependent and must be known before an optimized thermal sensor can be designed for fabrication by a specific CMOS process.

Typically, CMOS thermopiles consist of 5–100 thermocouples embedded in dielectric membranes with an internal resistance of 10^3 to 10^6 Ω and a thermal conductance on the order of 0.1 mW/K. Thermopowers and sensitivities are up to about 10 mV/K and 100 V/W, respectively.[11] Before this study, we successfully fabricated a conventional thermopile with 11 thermocouples in each quarter of the membrane. The total number of thermocouples was 44. The chip size and floating membrane area of this device were 1950×1720 μm^2 and 1100×1100 μm^2, respectively.

In this study, we propose a new structure consisting of a large floating membrane using several microlink structures, which link separate parts without any further modification of standard CMOS processes. A sensor with a larger active area gives a higher voltage signal that can easily be amplified. To demonstrate the functions of the microlink structures, structures both with and without microlinks are shown in Fig. 1. One can see that the structure with microlinks can have a flat plane and a larger extended area, whereas the structure without microlinks can easily bend or crack when the area is extended.[13]

To illustrate the design consideration for this purpose, Fig. 2 shows the anisotropically wet etching of undercut of the membrane extending from the etching windows between the microlink and membrane step by step. After undercut regions 1(a) and 1(b) overlap each other, undercut region 2(a) will be etched gradually. The etching process will then be extended to undercut region 2(b) and finally the undercut region 3 will be removed subsequently. Therefore, this process allows rapid release of the undercut of membrane and efficient removal of the substrate. It is worth noting that using the microlink
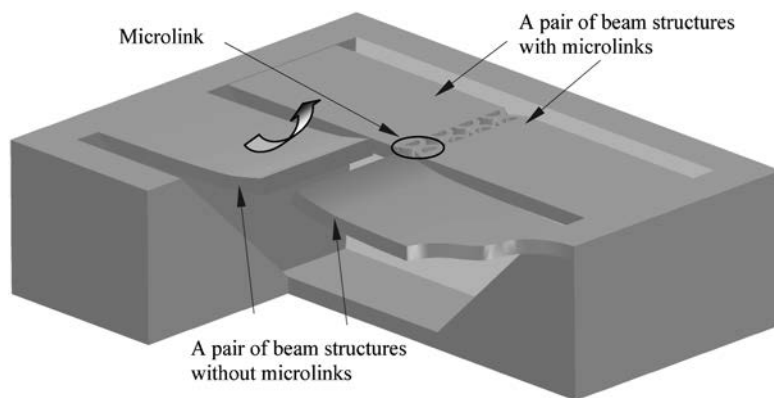

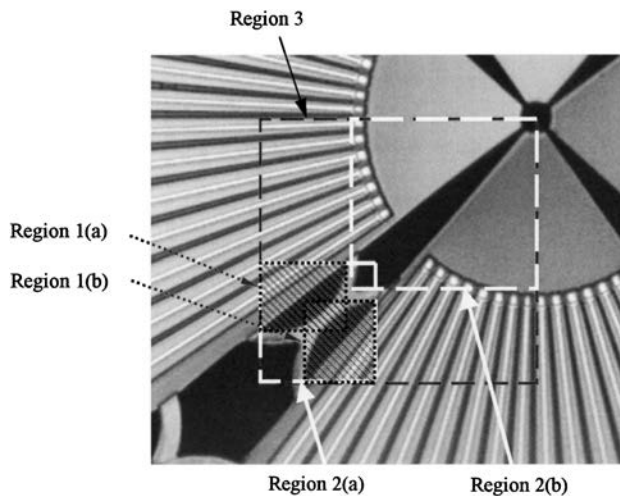Fig. 1.   Schematic of the structures with and without microlinks.

Fig. 2.   Design consideration of etching windows.

structure, we can easily open deep V-groove etching windows that approach the center of the membrane and achieve high etching efficiency. This has not been realized in previous studies.

To further increase the large absorption area, several new types of thermopile with microlinks are proposed in this study; the thermopiles are constructed using a series of microlinks between each quarter of the membrane or between the suspension beam and the substrate. The large active area is successfully generated by reducing the area of the etching windows.

The design and fabrication of the conventional and microlink-based thermopiles are realized using 1.2 μm CMOS IC technology combined with subsequent anisotropic front-side etching. The fabrication steps of these thermopiles are shown in Fig. 3. First, a nitride layer is grown on a silicon substrate as the membrane layer. Onto this membrane, the standard materials of two thermoelectric conductors (n-poly, Al) are deposited and structured. Both conductors have alternately placed junctions in the center of the membrane (hot junctions) and above the edge of the silicon substrate (cold junctions). Four etching windows are opened by CMOS processes, and then using tetramethylammonium hydroxide (TMAH) etching solution, the silicon substrate is etched along the <100> directions. The central part of the silicon substrate beneath the membrane is removed and only a thin sandwich layer of SiO_2/Si_3N_4 with 2 μm thickness is left on top.

The parameters for the pad oxide and nitride deposition layers of our thermopiles yielded the following approximate values: the same Young's modulus of 380 GPa, and thermal expansivities of 12×10^{-6}/K and 0.8×10^{-6}/K, respectively. The energy and dose of polysilicon implantation are 60 keV and 1×10^{14} cm^2, respectively. The energy of N+ implantation is the same as that of polysilicon, and the implantation takes 30 min at

Step 1. A LPCVD nitride layer is grown
on a silicon substrate

LP-nitride
Silicon substrate

Thermoelectric materials

Step 2. The thermoelectric materials
are formed

Al
Poly
LP-nitride
Silicon substrate

Step 3. Several passivation layers are
deposited

Passivation layer
Al
Poly
LP-nitride
Silicon substrate

Etching window

Step 4. Etching windows are opened

Passivation layer
Al
Poly
LP-nitride
Silicon substrate

Wet. etching (TMAH)

Step 5. Bulk micromachining process

Passivation layer
Al
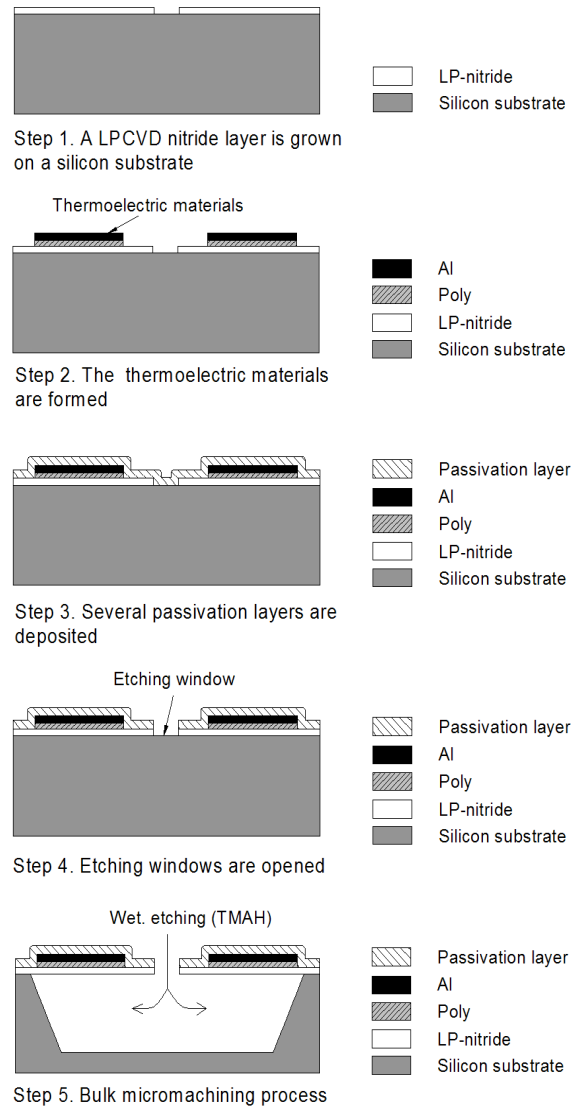Poly
LP-nitride
Silicon substrate

Fig. 3.   Fabrication steps using CMOS-compatible process.

1000°C. Moreover, the film thicknesses of the pad oxide, nitride deposition, polysilicon deposition, Al/metal sputtering, plasma-enhanced chemical vapor deposition (PECVD) SiO_2, and Si_3N_4 layers are 900, 1500, 3800, 9700, 5000, and 5000 Å, respectively.

Figure 4(a) shows the conventional thermopile without microlinks, and Figs. 4(b)–4(d) show the proposed microlink-based thermopile structures. We use an interference-type black body on the membrane shown in Figs. 4(a)–4(c), and one can see the
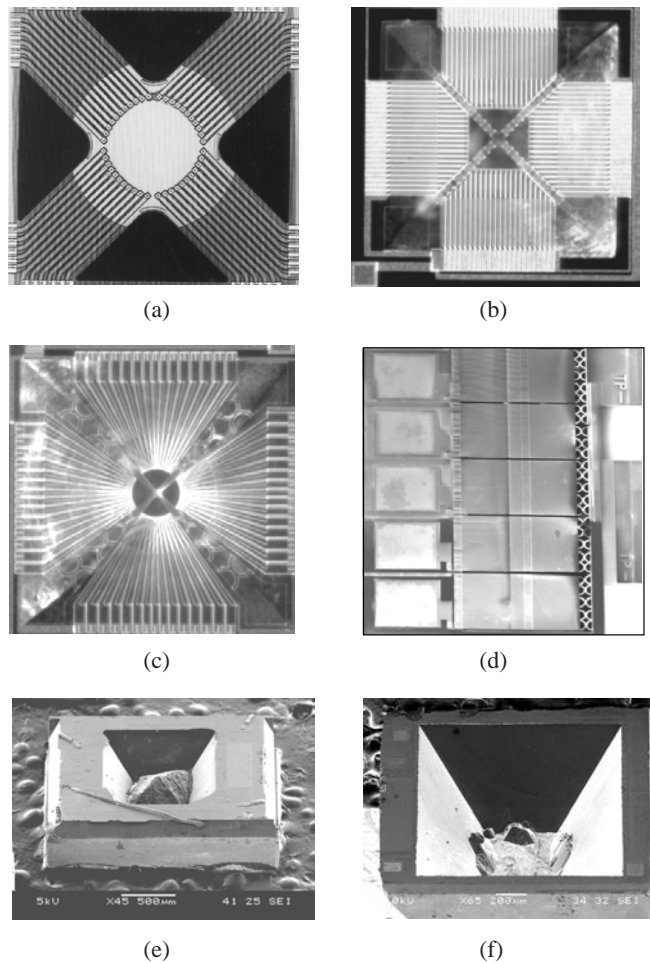
Fig. 4.   (a) Photograph of thermopile without microlinks, (b) photograph of thermopile ML-1 with microlinks. (c) photograph of thermopile ML-2 with microlinks, (d) Photograph of array of thermopiles with microlinks, (e) Result of V-groove etching conventional thermopile, (f) result of V-groove etching thermopile ML-2.

different color of the visible light under the microscope. The black body can increase the absorption of IR radiation, and the thickness is optimized under various process conditions.

To study the microlink-based sensors, we propose two new thermopile structures, denoted by ML-1 and ML-2, which have four large freestanding membranes that are each connected to neighboring membranes by microlink structures. The first structure, ML-1, with 90 pairs of thermoelectric elements, is constructed on an 1300×1300 μm² floating membrane with the same chip size as the conventional thermopile, and is

shown in Fig. 4(b). The typical responsivity of this thermopile is about 93.7 V/W and its resistance is around 36 kΩ. There are six microlinks with a width of 6 μm between two nearest-neighbor membranes. The use of such small links gives several advantages for the design beyond the inherent geometrical pattern of front-side etching. The larger etching windows around the four corners of the thermopile are designed to allow etching solution to enter more easily, which can reduce the etching time. The etching windows are opened carefully to enable silicon substrate etching, after which a hollow cavity is left.

The second sample, ML-2, with 60 pairs of thermoelectric elements, has a floating-membrane area of 1300×1300 μm^2 and is shown in Fig. 4(c). Each nearest-neighbor membrane is connected by three microlinks with a width of 10 μm, enabling the largest floating membrane yet realized to be created by a front-side etching technique. The etching windows are opened efficiently so that the silicon substrate beneath is anisotropically etched completely, leaving a hollow cavity. The chip size of this thermopile is the same as that of ML-1 and the conventional thermopile. The typical sensitivity of this thermopile is about 95.5 V/W and its resistance is around 35.2 kΩ.

In addition, we propose another application of microlinks, namely, an array of thermopiles with microlinks, as shown in Fig. 4(d). At each thermopile, the suspended end of its beam structure is connected by five microlinks with a width of 10 μm to prevent the structure bending. More applications of microlinks are currently being developed.[14]

Out of over 30 pattern designs of the conventional thermopile, the one used in this research is the largest one that can be formed without any adhesion between the membrane and the substrate, but some residue of the substrate beneath the membrane remains after etching. Nevertheless, using the microlink structure, we successfully enlarged the area of the membrane by 40%, i.e., 1300×1300 μm^2 vs 1100×1100 μm^2. Also the etching windows are opened so as to remove the substrate cleanly and achieve high etching efficiency. The microlink-based and conventional thermopiles are etched with the same process time, 6.5 h. For etching times longer than 6.5 h, the etching process is saturated. To inspect the results of etching, photographs are taken from the front of both thermopiles after removing the membrane, as shown in Figs. 4(e) and 4(f). One can see clearly that after etching the silicon substrate of the conventional sensor, residue remains beneath the membrane. However, the substrate of the microlink-based sensor is etched away completely and forms a hollow cavity at the bottom. The etching efficiency for the microlink-based thermopile is very high.

3.   Measurement and Discussion

To determine the performance of our proposed microlink-based thermopiles, measurements are carried out to compare the performance with results in previous research and for commercial thermopiles. Firstly, the optical and electronic characteristics of thermal sensors are measured and compared. Then, the surface morphology measurement of ML-2 is also performed to evaluate the effect of bending, and the damage to the microlinks of the thermopiles is inspected.

3.1 *Characteristics of different thermopiles*

To evaluate the performance of our proposed microlink-based thermopiles, a transistor cap with an IR filter is used to hermetically seal the sensor chip. The transmission range of the IR filter is chosen to be 5–14 μm in accordance with the application of detecting living objects. In the response measurement setup, the black body acts as a radiation source for the thermopile, and the output signal is delivered to a chopper amplification circuit to amplify the weak signal. The digital multimeter receives the output signal from thermopile sensing elements. All the experiments are performed inside an optical shield chamber to reduce the ambient light and other background noise.[15] A comparison between microlink-based thermopiles and the other thermopiles is performed, the measurement results of which are shown in Table 1.

Table 1 lists the characteristics for existing devices and the microlink-based samples. One can see that with the same chip size we can improve the fill factor of the membrane area by using microlinks. For the front-side-etched thermopile devices, the detectivity is always small, and $< 10^8$ cm(Hz)$^{1/2}$/W. Nevertheless, for ML-1 and ML-2, the detectivity is the highest yet reported using the front-side etching method.[4,5] The detectivity is comparable in performance to back-side-etched devices.[3] The membrane area of ML-2 is larger than that of ML-1 so that a larger active area can be used and the performance of ML-2 is as high as that of ML-1. By increasing the fill factor of the membrane area, ML-1 and ML-2 can be arranged with larger numbers of thermocouples than the conventional thermopile, OTC 236, of up to 92 and 60 pairs, respectively, and these devices give higher sensitivity and detectivity.

3.2 *Thermopile surface morphology measurement*

The silicon fracture strength and surface morphology of the membrane after etching are important in MEMS design. The film morphology depends on material properties such as average strain, strain gradient, Young's modulus, fracture strength and material damping constant, so the parameters specific to deposition and/or fabrication processing are the main factors affecting surface morphology. For a standard CMOS process, the film morphology is based on the material properties, which are restricted as mentioned earlier.

Table 1
Characteristics of different thermopiles.

		Sample				
		OTC236[5]	ML-1	ML-2	Baltes[4]	TPS434[3]
Parameter	Chip size (mm^2)	1.72×1.95	1.72×1.95	1.72×1.95	—	2.2×2.2
	Elements N	44	92	60	40	40
	Resistance (kΩ)	65	36	35.2	—	40
	Sensitivity (V/W)	55	93.7	95.5	30	48
	NEP (nW/(Hz)$^{1/2}$)	0.59	0.26	0.25	—	0.54
	Detectivity (cm(Hz)$^{1/2}$/W)D*	8.53×10^7	1.94×10^8	2.01×10^8	3×10^7	9.3×10^7
	Time constant (ms)	18	18	18	10	20
	Etching method	Front-side	Front-side	Front-side	Front-side	Back-side

The structure of proposed microlink-based sensors fabricated using a standard CMOS process might result in the concentration of stress and lead to deformation or damage of film. Therefore, we investigate the morphology and failure of the thermopile and microlink structures. To inspect the effect of residual stress, FOGALE nanotech: ZoomSurf 3D apparatus is used for noncontact measurement with a high vertical resolution of 0.1 nm to characterize the geometry of the membrane. The surface morphology measurement of ML-2 is performed. The instrument measures the microrelief of a surface and quantifies its roughness by statistical analysis. By
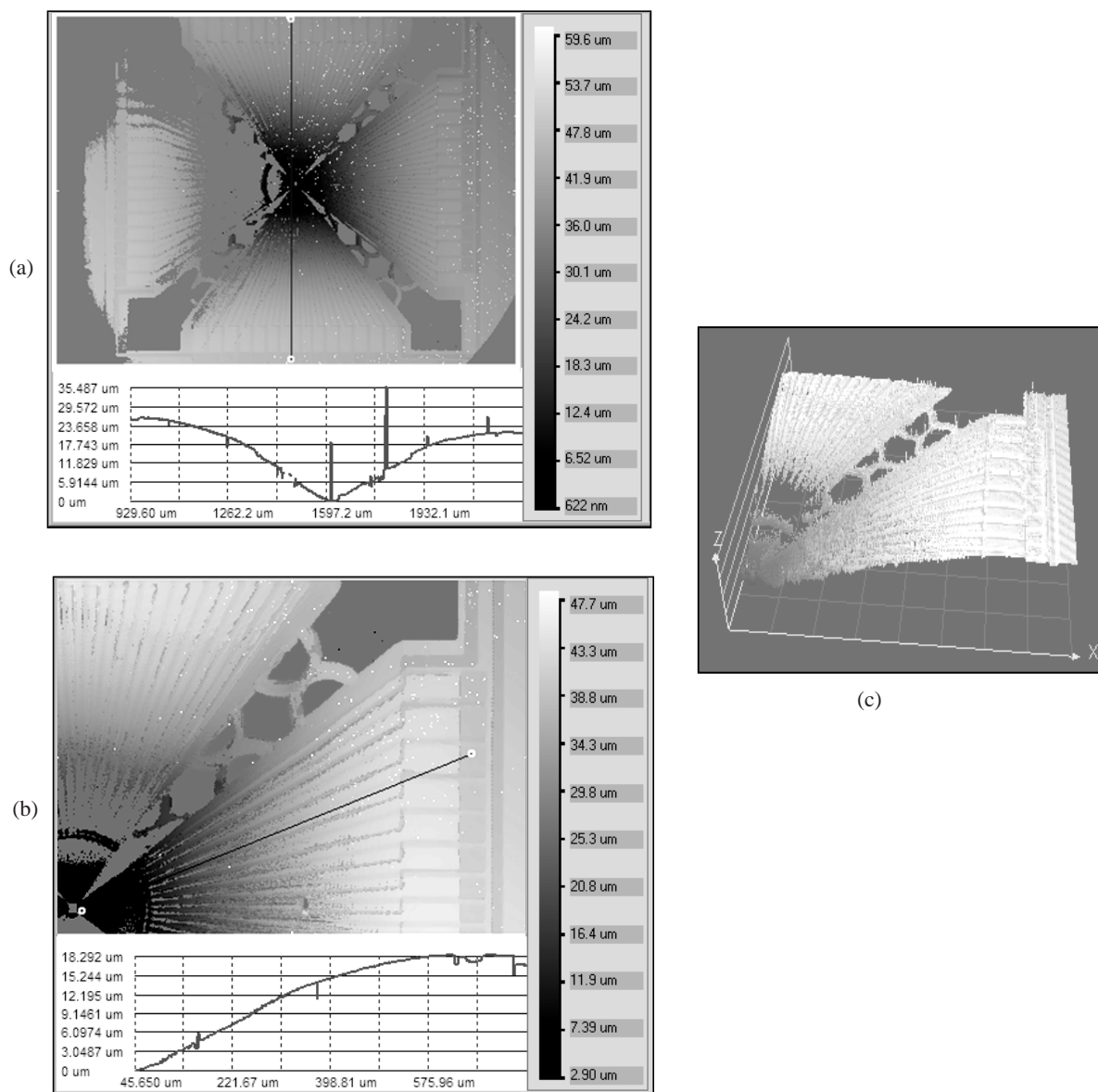

Fig. 5. (a) Morphology and cross-sectional profile of the whole microlink-based thermopile ML-2, (b) Morphology and cross-sectional profile of a quarter of microlink-based thermopile ML-2, (c) 3D morphology of a quarter of microlink thermopile.

measuring the whole thermopile surface and a quarter of it, complete and detailed surface morphologies are acquired, as shown in Figs. 5(a)–5(c).

From the results shown in Fig. 5, the side effects of microlink buckling are carefully inspected to demonstrate the practicality of our proposed microlink-based thermopile structure. Figure 5(a) shows the morphology and cross-sectional profile of the whole microlink-based thermopile ML-2. At the central part of the cross section, the curvature of the deformed variation is larger than that at the boundary. It still buckles slightly but does not cause any noticeable degradation of the sensor performance. The variation of deformation is around 18 µm over a distance of 500 µm, as shown in Fig. 5(b).

Figure 5(c) clearly shows the 3D morphology of a quarter of the microlink-based thermopile ML-2. The part with the darker tone means that the depth is greater. The roughness and missing part of the surface are due to measurement noise.

3.3   *Damage to microlinks of thermopile*

All our proposed devices are intentionally designed to have nonmoveable parts that absorb IR radiation to perform a given function. Most of the structures with microlinks used for our proposed thermopiles were in good condition after the postprocess etching. In Figs. 6 and 7, we compare a successful die and a failed die to investigate the condition of the microlinks. The microlink structures of thermopiles ML-1 and ML-2 and the array of thermopiles shown in Fig. 4 are in good condition apart from there being fewer microlinks on the array of thermopiles. The thermopiles and associated microlink regions are shown in Fig. 6. Figure 7 shows some breakages that initiated at the microlink structure. The microlinks are demonstrated to be applicable to thermal microsensors and to enhance the structure of the floating membrane.

4.   Summary

Using microlinks, we have proposed a new structure for floating membrane devices that enables a large membrane area to be obtained; thus, the etching windows can be opened efficiently. The improvements on the previous structures are summarized as

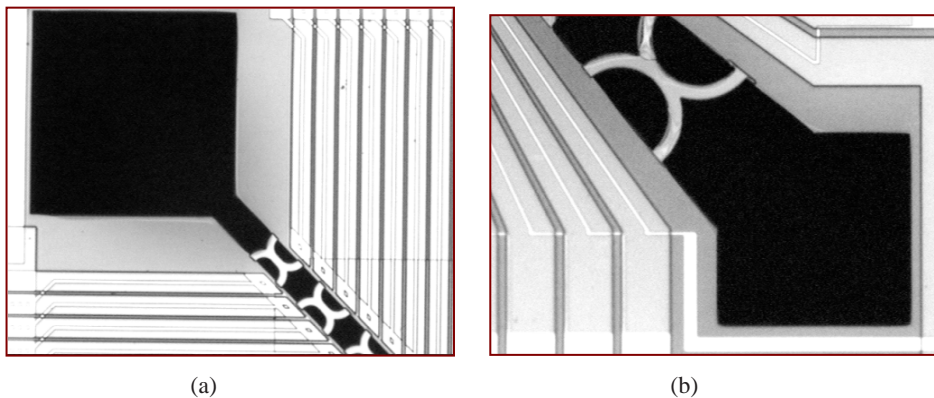| (a) | (b) |

Fig. 6.   (a) Close-up photograph of the microlinks of thermopile ML-1 in good condition, (b) Close-up photograph of a microlink of thermopile ML-2 in good condition.
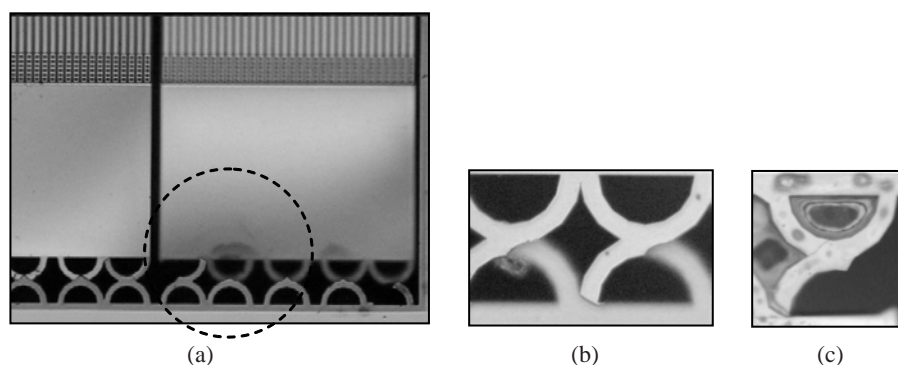
Fig. 7. (a) Photograph showing the failure of the microlink structure, (b) and (c) Close-up photographs showing the failure of the microlink structure.

follows. Firstly, using the microlink structure to reduce the area of the V-groove etching window, a larger active area can be designed and fabricated than in a conventional structure with the same chip size. On the other hand, more pairs of thermocouples can be arranged on the membrane at the same time. Hence, a stronger signal can be detected from the larger active area than that obtained using other sensors. Secondly, the microlinks provide a suitable etching window so that the substrate beneath the floating membrane can be etched greatly and effectively. Finally, the new structure prevents bending at the edges of the large floating membrane.

The design and fabrication of the microlink-based thermopiles were realized using 1.2 μm CMOS IC technology combined with subsequent anisotropic front-side etching. Aluminum and n-type polysilicon, which are the standard materials in the CMOS process, were used as the thermoelectric elements. Our large floating membrane has an area of 1300×1300 μm^2 and is 2 μm thick. The chip size of the thermopiles is 1950×1720 μm^2. The detectivity can reach $> 2 \times 10^8$ cm(Hz)$^{1/2}$/W, which is even higher than that of existing devices realized using back-side-etching techniques. Another application of microlinks, an array of thermopiles with microlinks, is proposed at the same time; at each thermopile in the array, the suspended end of its beam structure is supported by five microlinks to avoid the bending of the structure. A larger membrane structure area can be obtained using microlink structures, and more flexible structures can be designed incorporating such structures.

The morphology and cross-sectional profile of the whole microlink-based thermopile was acquired by FOGALE nanotech's ZoomSurf 3D apparatus. At the central part of the cross section, the curvature of the deformed variation was larger than that at the boundary. The variation of deformation was around 18 μm over a distance of 500 μm.

The results of etching and the breakage of the microlink-based thermopiles were obtained. Most of the structures and microlinks of our proposed thermopiles were in good condition after postprocess etching apart from there being fewer microlinks on the array of thermopiles. The microlinks are proven to be applicable to thermal microsensors and to enhance the structure of the floating membrane.

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