Fabrication and Characterization of a Low-Temperature Hermetic MEMS Package Bonded by a Closed-Loop AuSn Solder Line

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In this paper, we present a hermetic MEMS package bonded by a closed-loop 80Au20Sn solder line. We designed three different test specimens including a substrate-heated specimen without an interconnection line (SHX), a substrate-heated specimen with an interconnection line (SHI), and a locally heated specimen with an interconnection line (LHI). A pressurized helium leak test was carried out to evaluate the hermetic seal along a critical pressure test to measure bonding strength. In the bonding process, the substrate heating methods (SHX, SHI) require 400°C and 40 min, while the local heating method (LHI) requires a heater power of 6.76 W for 4 min. In the hermeticity test, SHX, SHI, and LHI show leak rates of $8.4\pm6.7\times10^{-10}$ mbar-l/s, $13.5\pm9.8\times10^{-10}$ mbar-l/s, and $18.8\pm9.9\times10^{-10}$ mbar-l/s, respectively, for the same internal volume of $6.89\pm0.2\times10^{-6}$ l. In the critical pressure test, no fracture was found in the bonded specimens at an applied pressure of 1 ± 0.1 MPa. From these results, we determine an approximate bonding strength of the test specimen as 3.53 ± 0.07 MPa. We have experimentally verified that LHI shows the potential of hermetic MEMS packaging with an interconnection line and a bonding process for mass production that requires little time.

1.   Introduction

Recently, packaging has became one of the most important issues for MEMS devices and integrated electronic components.[1] MEMS devices such as microgyroscopes, accelerometers and pressure sensors require hermetic packaging with an electrical interconnection line running across the bonding interface. The requirements of MEMS packaging are classified into two categories of basic and special requirements as shown in Table 1. The

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Table 1
Classification of the requirements of MEMS packaging.

MEMS packaging requirements		Purpose
Basic requirements	Strength	Protect device from external forces and pressure
	Low temperature	Protect device and metal line
	Low electric field	Protect electrons
Special requirements	Hermeticity	Protect device from the environment and maintain a high quality factor
	Step coverage	Bond with interconnection lines

basic requirements of MEMS packaging include high mechanical strength to protect the device from external forces, protection from low temperatures for the metal line, and protection of the electronics using a low electric field. As special requirements of MEMS packaging, hermetic sealing is required for a high quality factor. In addition, the interconnection lines can be designed for signal transmission or power supply to the MEMS device across the bonding interface. This will cause a step-up bump condition on the bonding interface and presents a common challenge for many packaging and bonding schemes. Therefore, step coverage of the interconnection lines is also a special requirement of MEMS packaging.

Several bonding methods are compared in Table 2 according to the MEMS packaging requirements. In the past, anodic, fusion, and polymer bondings were used for hermetic MEMS packaging. Anodic and fusion bondings have the drawbacks of high bonding temperature and surface roughness sensitivity,[2] which can cause problems in terms of hermeticity in cases where interconnection lines exist across the bonding interface.[3] While polymer bonding is a low-temperature process[4] and good for step coverage, it has problems with hermetic sealing and bonding strength.

Localized silicon fusion and eutectic bondings[1] have been proposed to protect circuits/devices from high bonding temperature by employing localized heating techniques using poly-Si thin films. Since the melting points of silicon (1410°C) and Au (1063°C) are too high to satisfy the basic requirement of a low-temperature process, we consider a metal solder indirect bonding method which provides good characteristics[2,4,5] for MEMS packaging requirements. We suggest a closed-loop 80Au20Sn (melting point 400°C) solder-line bonding including substrate heating and local heating methods. In addition, we focus on investigation of factors affecting the long-term stability of localized bonding such as hermeticity, leakage with respect to time and harsh environments, and accelerated tests in specific areas to be explored in MEMS postpackaging.[2] Thus, we also present the pressurized helium leak rate test and bonding strength measurement of the fabricated packages.

Table 2
Comparison of the bonding methods.[2]

Bonding methods		MEMS packaging requirements					Comments
		Basic			Special		
		Strength	Low temperature	Low electric field	Hermeticity	Step coverage	
Direct bonding	Fusion	Good	Poor	Good	Good	Poor	Sensitive to surface roughness
	Anodic	Good	Moderate	Poor	Good	Poor	
Indirect bonding	Polymer	Moderate	Good	Good	Moderate	Good	Weak to humidity
	Ceramic	Good	Poor	Good	Good	Good	High coefficient of thermal expansion
	Metal	Good	Moderate	Good	Good	Good	Requires insulating layer

2. Test Specimen Design

We design three different test specimens including a substrate-heated specimen without an interconnection line (SHX), a substrate-heated specimen with an interconnection line (SHX), and locally heated specimen with an interconnection line (LHI) to evaluate the effect of the heating method and interconnection line in the requirements for MEMS packaging. Figure 1 shows a cross-sectional view of a test specimen identifying features including various layer materials and their thicknesses. Schematic diagrams of the solder-line bonding design are illustrated in Fig. 2. The bottom substrate contains the poly-Si line heater, sandwiched by oxide and nitride layers, and the AuSn solder line on the Ti/Au adhesion layer shown in Fig. 2(a). In this design, we separate the heating and bonding materials by introducing an intermediate layer, which provides a better way to control the localized bonding processes for MEMS fabrication and packaging.[3] The cap substrate (Fig. 2(b)), with a 65±1-μm-thick square silicon diaphragm, contains the Ti/Au adhesion layer on a 200-nm-thick poly-Si electrical interconnection line, sandwiched by the oxide and nitride layers. For the hermeticity test, we include a silicon diaphragm in the cap substrate to measure the deflection caused by the difference between the internal cavity pressure and external pressure.

We include a Ti/Au layer around the diaphragm as a bonding adhesive material. When we flow current through the poly-Si heater, AuSn solder lines melt and bond with the Ti/Au layer in the cap substrate in the vacuum chamber. In the design of the silicon diaphragm, its width and thickness are constrained by deflection measurement systems and reliability with respect to applied pressure. The major constraint from the deflection measurement
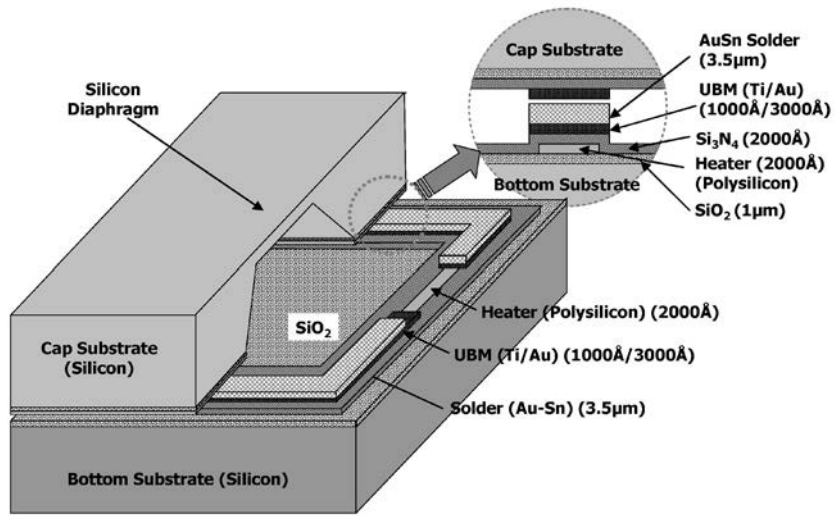
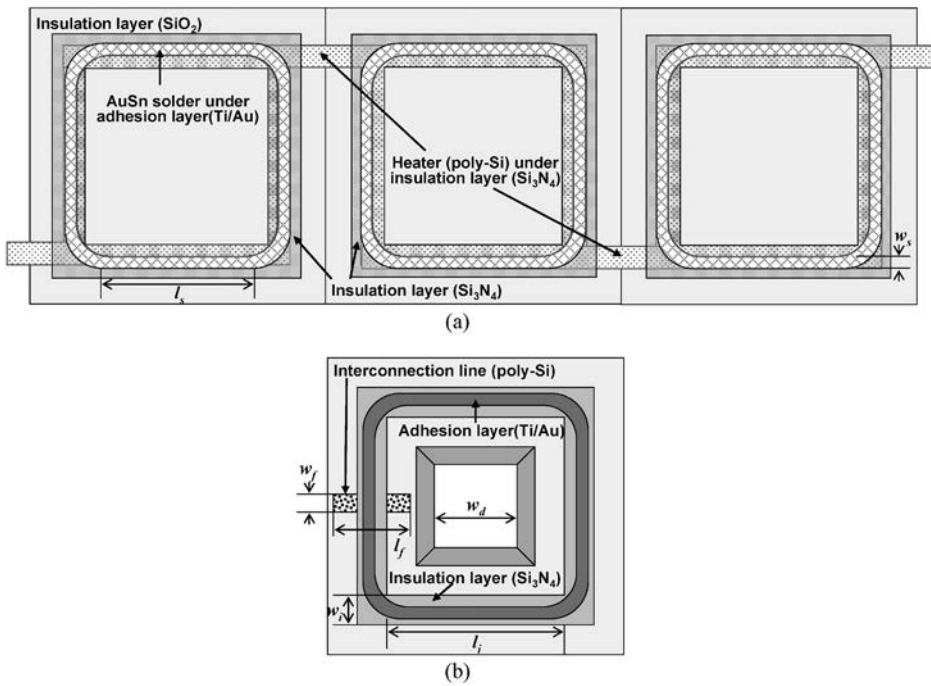Fig. 1.   Schematic view of the test specimen.

Fig. 2.   Test specimen with an electrical interconnection line passing through the bonding area: (a) bottom substrate showing the heater (poly-Si) network under insulation layer (Si$_3$N$_4$) for power feed-in of the LHI; (b) cap substrate.

systems of the laser interferometer (ACURA, Intek Inc.) is the width of the silicon diaphragm. An interferometer can measure the deflection of the silicon diaphragm over a maximum area of 2500×2500 μm at once. Therefore, we determined the width of the silicon diaphragm at 4000 μm, since it must be smaller than 5000 μm for the deflection of the edge and center of the silicon diaphragm to be measured at once.

The thickness of the silicon diaphragm is limited by reliability with respect to the applied pressure. A square diaphragm was chosen for easy fabrication and simple theoretical analysis. If an external force is uniformly applied to the diaphragm and the deflection is comparably small, the deflection at the center of the diaphragm and the stresses induced at the center and the edge of the diaphragm can be calculated as follows:

$$y_0 = 0.0151 \cdot \frac{Pw^4}{Et^3}\left(1 - v^2\right) \qquad (1)$$

$$\sigma_{center} = 0.1386 \cdot P\frac{w^2}{t^2} \qquad (2)$$

$$\sigma_{edge} = 0.3078 \cdot P\frac{w^2}{t^2}, \qquad (3)$$

where P, E, y_0, w, t, and v are the total applied pressure, Young's modulus for the silicon diaphragm (170 GPa), the diaphragm deflection, the width of the diaphragm, the thickness of the diaphragm, and Poisson's ratio (0.28),[6] respectively. Maximum stress is induced along the edge of the diaphragm, σ_{edge}, and it should not exceed the yield strength of the silicon substrate (630 MPa).[7] Considering a safety factor of 5 and measurement systems, the width-to-thickness ratio (w/t) and the thickness of the diaphragm are determined to be 63 and 65 μm, respectively, at maximum. An interconnection line of 2000-Å-thick poly-Si exists between the lower insulation layer of silicon dioxide and the upper insulation layer of silicon nitride in the cap substrate. For the bottom substrate, the width, length and thickness of one side of a closed-loop AuSn solder line are 500, 6700 and 3.5 μm, respectively. To improve the AuSn solder-line adhesion, a Ti/Au layer 1000 Å/3000 Å thick is used under AuSn solder lines of the same dimensions.

3. Fabrication Process

Figure 3 shows the fabrication process for the bottom and cap substrates of the closed-loop solder-line packaging. First, we fabricate the bottom substrate. On a silicon substrate, a thermal oxidation layer 1 μm thick is grown for insulation. Then, 2000-Å-thick poly-Si for the local heating line is deposited by low-pressure chemical vapor deposition (LPCVD) as shown in Fig. 3(a-1). The local heating line is defined by a photoresist (PR: AZ1512) and polycrystalline silicon etchant (HNO$_3$:H$_2$O:HF = 100:40:30). Silicon nitride (Si$_3$N$_4$) 2000 Å thick is deposited as an insulation layer in Fig. 3(a-2). A thick ZPN110 PR is spray-coated and patterned to form a PR mold and 1000-Å /3000-Å-thick Ti/Au and 3.5 μm-thick AuSn solder layers are sputtered as shown in Fig. 3(a-3). For low-temperature
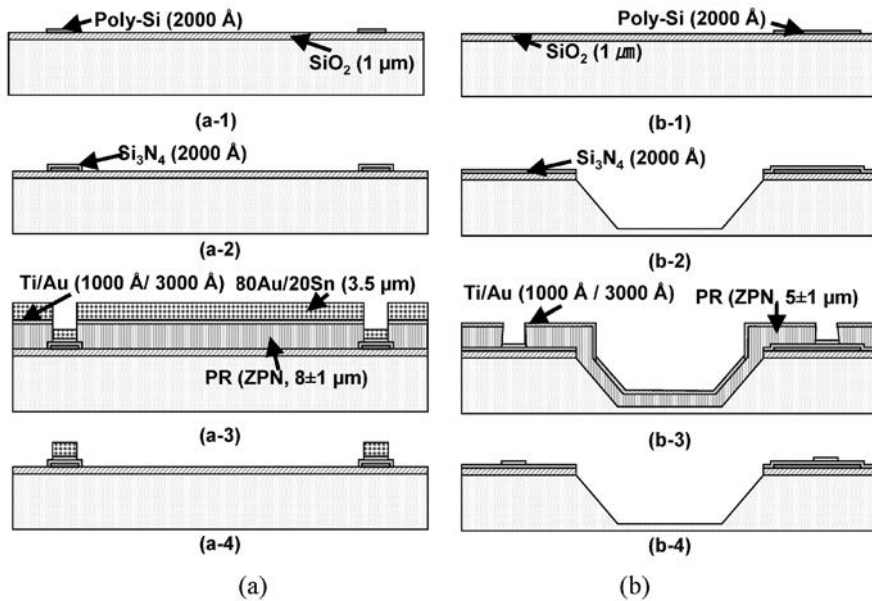
Fig. 3.   Fabrication process of closed-loop solder-line packaging: (a) bottom substrate; (b) cap substrate.

bonding and hermetic sealing over 2000-Å-thick interconnection lines, we use 3.5-μm-thick AuSn solder and a 1000-Å/3000-Å-thick Ti/Au adhesion layer. To lift off the Ti/Au and AuSn layers, we remove the PR mold using acetone.

Next, we fabricate the cap substrate. For insulation, an oxidation layer 1 μm thick is thermally grown. Then, poly-Si 2000 Å thick for feed-through lines is deposited by LPCVD as shown in Fig. 3(b-1). The PR is coated and patterned to obtain a mask for poly-Si wet etching. Feed-through lines are defined by the same polycrystalline silicon etchant used in the processing of the bottom substrate. Silicon nitride (Si_3N_4) 2000 Å thick for an insulation layer as well as a mask for silicon etching by KOH is deposited by LPCVD. The PR is coated and patterned for the RIE etching mask of the silicon nitride. A thermally grown silicon dioxide layer is wet-etched using buffered oxide etchant (BOE) solution. With a silicon nitride etch mask, silicon etching by KOH is carried out to create the 65±1-μm-thick silicon diaphragm in Fig. 3(b-2). Then, a thick ZPN PR is coated and patterned to form a PR mold. Ti/Au layers 1000 Å/3000 Å thick are sputtered as illustrated in Fig. 3(b-3). The PR mold is removed by dipping in acetone.

To compare the substrate-heated specimen and the locally heated specimen, we fabricate three different types of test specimens that include SHX, SHI and LHI in a bonding environment of 1 mTorr pressure.

Figure 4 shows the fabricated cap and bottom substrates that have the dimensions listed in Table 3. The substrate-heated specimens are heated in a vacuum oven with a bonding temperature of 400°C and a bonding time of 40 min. The specimen bonded by local heating in the 1 mTorr vacuum chamber is shown in Fig. 5. Bonding conditions for the test
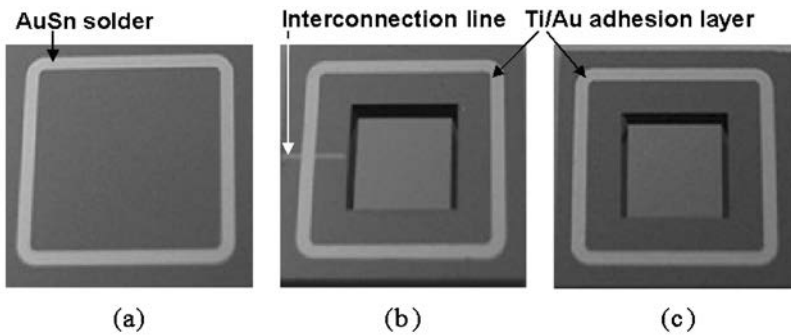
Fig. 4. Fabricated test specimen: (a) bottom substrate; (b) cap substrate with interconnection line; (c) cap substrate without interconnection line.

Table 3
Measured dimensions of the fabricated test specimens.

Layers		Specimen		
		SHX	SHI	LHI
Solder (AuSn)	w_s [μm]	502±2	501±2	502±2
	l_s [μm]	6,705±2	6,705±2	6,705±2
Adhesion metal (Ti/Au)	w_a [μm]	502±2	502±2	502±2
	l_a [μm]	6,705±2	6,705±2	6,705±2
Insulation layer (Si$_3$N$_4$)	w_i [μm]	701±2	701±2	701±2
	l_i [μm]	6,705±2	6,702±2	6,702±2
Interconnection line (Poly-Si)	w_f [μm]	–	198±2	199±2
	l_f [μm]	–	2,001±2	2,000±2
Diaphragm (Silicon)	w_d [μm]	3,888±2	3,887±2	3,887±2
	t_d [μm]	65±1	65±1	65±1

specimens are listed in Table 4. In the case of the locally heated specimen, we apply a current of 65±5 mA through the heater network as shown in Fig. 2 for 4 min. The temperature of the heater resistor rises to 420°C during the 4 min, which is 10 times faster than the bonding time of the substrate heating method.

4. Pressurized Hermeticity Test

The pressurized hermeticity test is performed for the investigation of the long-term stability of localized bonding. Leakage with respect to time and a harsh environment can be obtained from leak rate monitoring. The leak rate is used to analyze the hermetic sealing characteristics of the packaging. The standard leak rate, Q_{std} (mbar-l/s), is defined as the quantity in cm^3 of dry air at 25°C flowing through leak paths per second under a pressure difference of 760 mmHg between the internal cavity and the external cavity.[8] The leak rate, Q_m (mbar-l/s), of a given package is measured under specified conditions employing
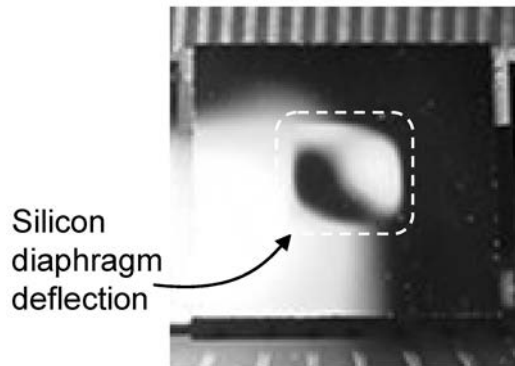
Fig. 5. Photograph of the test specimen showing the silicon diaphragm deflection of the cap substrate caused by the pressurized hermeticity test.

Table 4
Bonding conditions for the test specimens.

Bonding conditions	Specimen		
	SHX	SHI	LHI
Heater	Substrate heater	Substrate heater	Line (poly-Si) heater
Temperature or heating power	$400\pm5°C$	$400\pm5°C$	65 ± 5 mA@1.6 kΩ
Bonding time	40 min	40 min	4 min
Bonding load	2.069 kg	2.069 kg	2.069 kg
Bonding chamber pressure	1×10^{-3} Torr	1×10^{-3} Torr	1×10^{-3} Torr

a specified test medium. The measured leak rate, Q_m, should be converted to the leak rate under standard conditions, the equivalent standard leak rate, Q_{eq} (mbar-l/s), for comparison. The standard leak rate, Q_{std}, can also be defined by the cavity pressure change, ΔP_{cavity}, per second in the internal volume of the packaged cavity, when the internal cavity volume does not change or changes only slightly.

As it takes a long time to obtain a leak rate for a bonded specimen under atmospheric test conditions, an accelerated procedure is followed by adapting the pressurized test conditions. A medium lighter than air, such as hydrogen[9] or helium,[10] with a pressure of over 1 atm is used. We use helium as an internal medium under an external pressure of 30 psi. Figure 6 shows the test procedure for a pressurized leak test.

Using eq. (1), the cavity pressure change, ΔP_{cavity}, can be calculated from the deflection of the silicon diaphragm. The leak rate can be calculated from the measurement time interval. The leak rate, Q_m, can also be calculated from the deflection of the silicon diaphragm and the test conditions. The molecular leak mode[10] is used to convert the measured leak rate, Q_m, to the equivalent standard leak rate, Q_{eq}. The conversion equation is
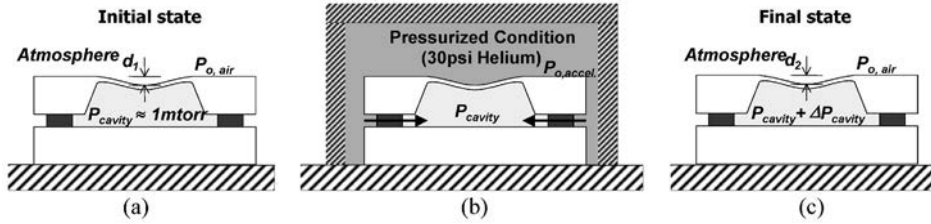
Fig. 6. Pressurized leak test (air tightness test) in a pressurized helium environment: (a) initial state after bonding; (b) pressurized state to make deflection change; (c) final state when the deflection change of silicon diaphragm is measured.

$$\frac{Q_{eq}}{Q_m} = \sqrt{\frac{M}{M_A}} \times \frac{P_o - P_{cavity}}{P_E - P_{cavity}},$$ (4)

where Q_m (mbar-l/s), Q_{eq} (mbar-l/s), M (g/mol), M_A (g/mol), P_E, and P_{cavity} are the measured leak rate, the equivalent standard leak rate, the molecular weight of the medium (helium) of 4 g/mol, the molecular weight of air of 28.7 g/mol, the external pressure of 2.04 atm, and the cavity pressure in a bonded specimen of 1 atm, respectively.

For the mechanical strength of the packaging, the bonding strength must be characterized. Tensile strength is the major mode of fracture in solder-line bonding. Among many test methods, the pull test and the critical pressurized test are conventional methods for characterizing bonding strength. Since the test specimens have very small dimensions compared with those of the test equipment, a small misalignment between the specimen and the equipment can cause a large deviation in the experimental results. To eliminate the effect of loading misalignment in a test specimen, we use the critical pressurized test to evaluate the bonding strength. Figure 7 shows a schematic diagram of the critical pressured test equipment.

5. Experimental Results

Using the bonded test specimen, we carried out the pressurized hermeticity test under conditions of pressurized helium.[10] We obtained the pressure differences and leak rates from silicon diaphragm deflections measured using the interferometer. Figure 8 and Table 5 show the experimental results of the deflection measurement and measured deflection of the silicon diaphragm over time, respectively.

In the hermeticity test, SHX, SHI and LHI show leak rates of $8.4\pm6.7\times10^{-10}$ mbar-l/s, $13.5\pm9.8\times10^{-10}$ mbar-l/s, and $18.8\pm9.9\times10^{-10}$ mbar-l/s, respectively, for an identical inter-
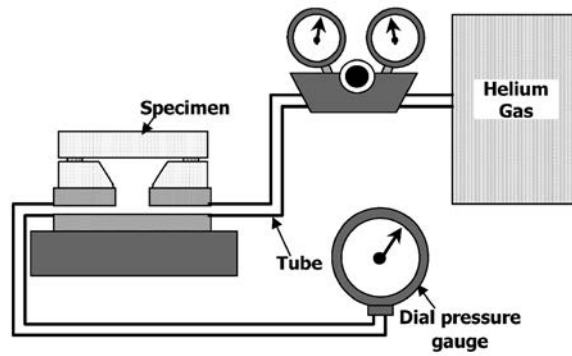
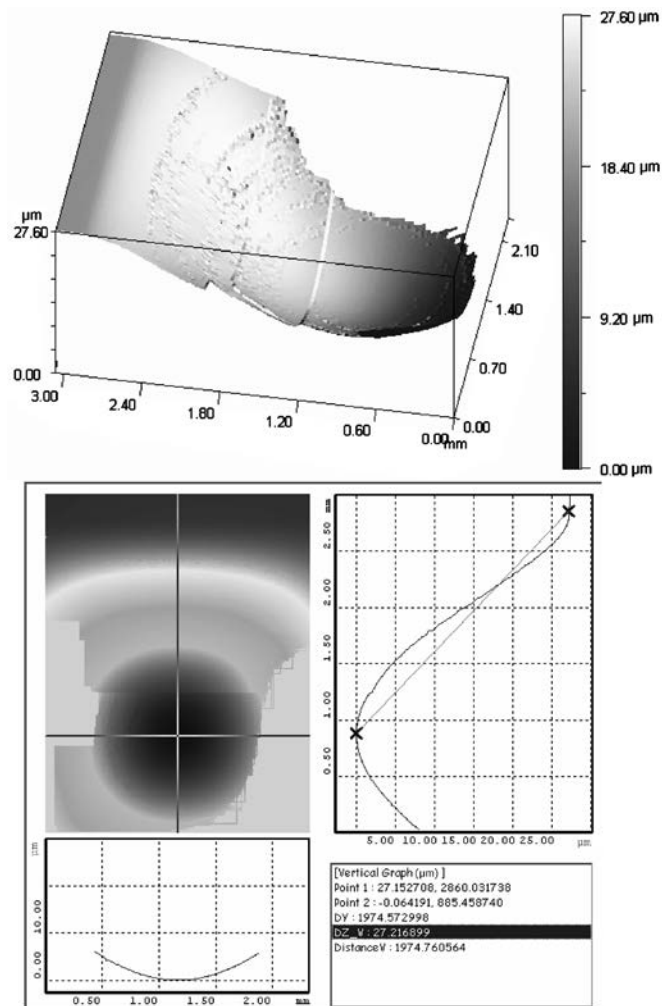Fig. 7.   Equipment for critical pressure test of bonding strength.

Fig. 8.   Deflection of the silicon diaphragm measured using an interferometer.

Table 5
Measured deflections of the silicon diaphragms.

Deflection	Specimen		
	SHX	SHI	LHI
Initial state	26.8±0.1 [μm]	27.9±0.1 [μm]	27.8±0.1 [μm]
After 24 h in air	26.6±0.1 [μm]	27.7±0.1 [μm]	27.4±0.1 [μm]
After 2 h in 30 psi He	26.6±0.1 [μm]	27.5±0.1 [μm]	27.1±0.1 [μm]

nal cavity volume of $6.89±0.2×10^{-6}$ l. Compared to the hermetic seal requirements of MIL-STD-883E (a leak rate of $5×10^{-8}$ mbar-l/s for an internal cavity volume of $4×10^{-4}$ l),[7,8] all three specimens, LHI, SHI, and SHX, satisfied the hermetic sealing criteria, although the specimens SHX and SHI bonded by the substrate heater show a lower leak rate than LHI. Therefore, all specimens satisfy the special requirements of MEMS packaging of hermetic sealing with an interconnection line.

For the bonding strength measurement, we performed the critical pressure test as depicted in Fig. 7. For a cavity pressure of up to 1±0.2 MPa, the specimens show no mechanical failure, resulting in a bonding strength of at least 3.53±0.07 MPa. This bonding strength is greater than that of indium-to-glass localized bonding (2.6 MPa).[3] To measure the ultimate bonding strength, a source pressure higher than the one in this work must be used.

To determine the influence of the heating area on leak rate, we divided the bonded specimens into cap and bottom substrates using pull test equipment, and then carried out the energy-dispersive X-ray spectrometer (EDS) analysis. Figures 9 and 10 show the results of EDS analysis. From the EDS analysis at a bonded interface, we find that the substrate-heated specimen failed primarily between the Ti/Au layer and the Si_3N_4 layer in the cap substrate as shown in Fig. 9, and the locally heated specimen failed primarily between the Ti/Au layer and the AuSn solder layer in the bottom substrate as shown in Fig. 10. Moreover, in the case of the locally heated specimen, an unbonded region was observed. We expect that these results are caused by insufficient bonding time. In the case of substrate-heated specimens, the adhesion strength of the interface between the Ti/Au and the Si_3N_4 layers is weaker than that between the Ti/Au and AuSn solder, while the bonding strength between the Ti/Au and AuSn solder is weaker than other deposited interfaces in the case of locally heated specimen. If the locally heated specimen is bonded under optimum bonding conditions, we may expect experimental results similar to those from the substrate-heated specimen.

6.   Conclusions

In this paper, we presented a hermetic MEMS package bonded by a closed-loop 80Au20Sn solder line. To investigate the requirements of MEMS packaging with regard to this bonding method, we carried out a pressurized helium leak test to evaluate the hermetic seal and a critical pressure test to measure the bonding strength. We designed three
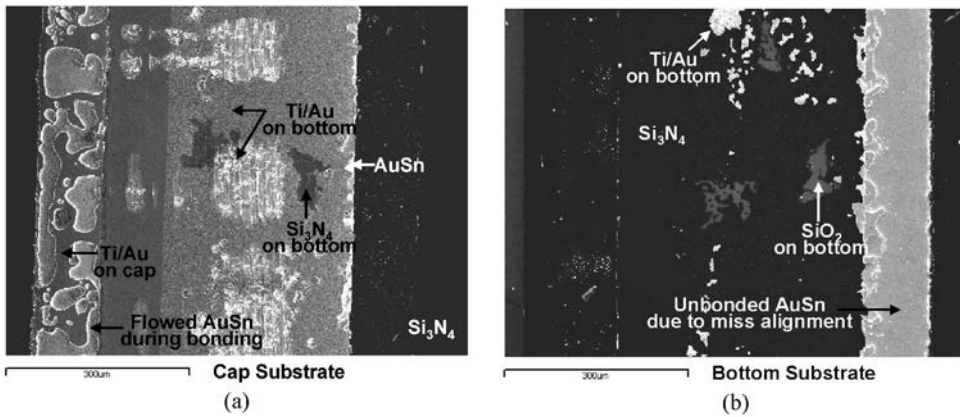
Fig. 9.   Analysis of material at the fracture surface of the substrate-heated specimens based on EDS: (a) cap substrate; (b) bottom substrate.
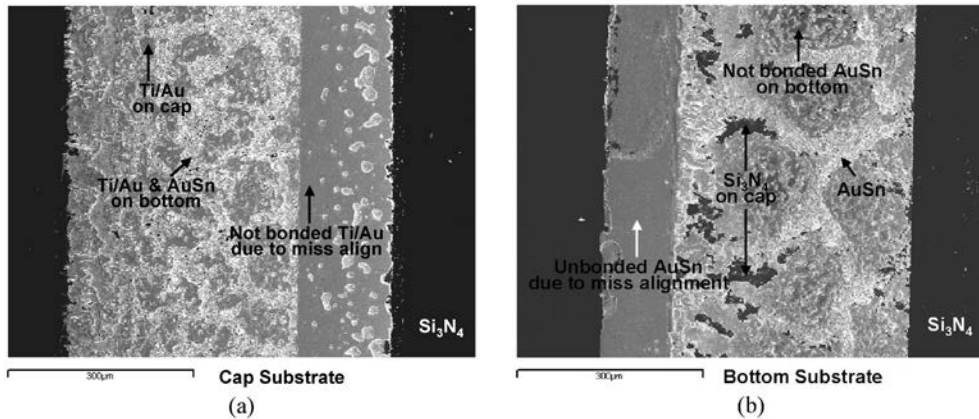

Fig. 10. Analysis of material at the fracture surface of the locally heated specimens based on EDS: (a) cap substrate; (b) bottom substrate.

different test specimens including SHX, SHI and LHI to verify the effect of the local heating method as well as the interconnection line. In the hermeticity test, SHX, SHI and LHI with the same internal volume of $6.89\pm0.2\times10^{-6}$ l show a leak rate of $8.4\pm6.7\times10^{-10}$ mbar-l/s, $13.5\pm9.8\times10^{-10}$ mbar-l/s, and $18.8\pm9.9\times10^{-10}$ mbar-l/s, respectively. The specimens of SHX and SHI, bonded by the substrate heater, show a lower leak rate than LHI, and all three test specimens satisfied MIL-STD-883E for the hermeticity test of the microcircuit. Considering the bonding process time, the local heating process requires only 4 min, while the substrate heating process requires 40 min. In the additional critical pressure test, no fracture was found in the bonded specimens at an applied pressure of

1±0.1 MPa. From these results, we determined an approximate bonding strength of the test specimen of 3.53±0.07 MPa. With EDS analysis at the bonded interface, we found that the bonded interface (between AuSn solder and Ti/Au) of the substrate-heated specimens is stronger than that of the locally heated specimen. However, we verified experimentally that locally heated closed-loop AuSn solder-line bonding may be applied for MEMS packaging with interconnection lines.

Consequently, AuSn solder-line bonding satisfies the basic and special requirements of MEMS packaging including high strength, low temperature, no electric field, and hermetic sealing with interconnection lines. In addition, the AuSn solder-line bonding based on local heating provides a high-speed packaging process for hermetic MEMS devices with interconnection lines.

Acknowledgement

References

1 Y. T. Cheng, L. Lin and K. Najafi: J. Microelectromech. Syst. **9** (2000) 3.

2 L. Lin: IEEE Transactions on Advanced Packaging **23** (2000) 608.

3 Y. T. Cheng, L. Lin and K. Najafi: 12th Int. MEMS Conference (IEEE, Orlando,1999) p. 285.

4 W. Y. Zhang, G. S. Ferguson and S. T.-Lucic: Int. Semiconductor Device Research Symposium (2003) p. 287.

5 Y. T. Cheng, W. Hsu, K. Najafi, C. T. Nguyen and L. Lin: J. Microelectromech. Syst. **11** (2002) 556.

6 D. G. Mario: Flat and Corrugated Diaphragm Design Handbook (Marcel Dekker, 1982) Chap. 20.

7 T. Yi, L. Li and C.-J. Kim: Sens. Actuators, A **83** (2000) 172.

8 Department of Defense: *Test Method Standard Microcircuits*, MIL-STD-883E, Method 1014.9 SEAL part.

9 S. Mack, H. Baumann and U. Gosele: 11th Int. MEMS Conference (IEEE, Nagoya, 1997) p. 488

10 R. C. McMaster: Nondestructive Testing Handbook (American Society for Nondestructive Testing, 1982) Chap. 3.

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