Silicon-on-Insulator Complementary Metal Oxide Semiconductor Image Sensor Using a Nanowire Metal Oxide Semiconductor Field-Effect Transistor-Structure Photodetector

Mi-Young Do, Sung-Ho Lee, Sang-Ho Seo, Jang-Kyoo Shin[*]
Pyung Choi, Jae-Hyoun Park[1] and Hoon Kim[1]

School of Electrical Engineering and Computer Science, Kyungpook National University,
1370 Sankyuk-dong, Buk-ku, Daegu, 702-701, Korea
[1]Korea Electronics Technology Institute, 68 Yatap-dong, Bundang-gu,
Seongnam-si, Kyunggi-do, 463-816, Korea

To design a silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) image sensor using a nanowire metal-oxide semiconductor field-effect transistor (MOSFET)-structure photodetector, SOI MOSFET model parameters were extracted by using the equation of bulk MOSFET model parameters. They were optimized by using a simulation program with integrated circuit emphasis (SPICE) level 2. Simulation results of the I-V characteristics of the SOI MOSFET using the extracted model parameters were compared to the experimental I-V characteristics of the fabricated SOI NMOSFET. The simulation results were in good agreement with the experimental results. An active pixel sensor (APS)-type unit pixel was designed for a SOI CMOS image sensor. The response time of the SOI CMOS image sensor is shorter than that of the bulk CMOS image sensor with the same structure. In accordance with the array simulation results of the SOI CMOS image sensor, they exhibited a clearer image than the bulk CMOS image sensor, due to a better frequency response.

1. Introduction

In general, image sensors are devices that convert optical signals into electric signals. There are two kinds of image sensors. One is a charge-coupled device (CCD) image sensor and the other is the CMOS image sensor (CIS). There are many kinds of electronic imaging products on the market and they are used in commercial and military systems such as camcorders, digital still cameras, and star-tracking systems. The CCD surpasses other

*Corresponding author, e-mail address: jkshin@ee.knu.ac.kr

devices in terms of noise characteristics and it has a larger gain than the CIS, but it requires a high supply voltage and special fabrication processes. On the other hand, the CIS can be operated with a lower supply voltage and fabrication cost can be reduced because it is fabricated by standard CMOS technology and can be integrated with other analog circuits. However, there are disadvantages such as considerable noise, low sensitivity and gain problem. Therefore, there is much ongoing research to improve the problems of the CIS.[1,2]

Silicon-on-insulator (SOI) technology has been proven to be advantageous in many applications as compared with conventional bulk technology. In particular, its radiation hardness has long been valued in space and military applications. The advantages of SOI technology arise from the fact that the active devices are built on top of an insulating layer. The use of the SOI wafer has been motivated by the full dielectric isolation of individual transistors, which prevents latch-up. This results in a considerably smaller pn junction area and parasitic capacitance, which is the source of the noise, making SOI devices superior to bulk-silicon devices regarding high-performance/low-power applications. Because of significant improvements with regard to the fabrication process and a reduction in manufacturing costs since the 1990s, SOI technology is now being developed for wide-scale consumer applications.[3]

As a result, image sensors built on SOI substrates have been used in many useful applications.[4,5] Image sensors on SOI substrates, however, suffer from low quantum efficiency. When a conventional pn junction photodiode is used, owing to the limited depth of silicon available on the top film, most of the photons pass through the sensing regions without being absorbed. This limitation inhibits the development of SOI-imaging systems. In order to overcome this barrier, CIS was developed using a nanowire metal-oxide semiconductor field-effect transistor (MOSFET)-structure photodetector.[6,7] The performance of the CIS on a SOI substrate is expected to possess the potential for a higher speed because of the lower parasitic capacitance.

In this study, regarding the design of the SOI CIS, SOI MOSFETs were fabricated and model parameters were extracted. A nanowire MOSFET was used as the photodetector for the CIS. The SOI MOSFET model parameters were calculated by a SPICE level 1 model equation and were optimized using HSPICE by SPICE level 2. In addition, an active pixel sensor (APS)-type unit pixel for the CIS was designed and simulated using extracted model parameters. The results were compared with those of the APS-type unit pixel on a bulk Si substrate.

2.   MOSFET Photodetector and Characterization

The nanowire MOSFET photodetector was fabricated on a 4-inch SIMOX wafer with a silicon film thickness of 190 nm and a buried oxide thickness of 360 nm. The nanowire MOSFET with a channel width of 30 nm was fabricated on a SOI wafer using conventional photolithography, anisotropic wet etching, and reactive ion etching (RIE) techniques.

Figures 1(a) and 1(b) show the fabricated SOI NMOSFET with a nanowire width of 30 nm and the SEM image of the 30-nm-width silicon wire, respectively. Figure 2 displays the drain current-voltage (I-V) characteristics of the fabricated nanowire MOSFET for gate biases between 0 and 1.5 V. Figure 3 shows the measured drain current as a function of

gate voltage at a drain voltage of 0.1 V. Figure 4 shows the drain current characteristics of the nanowire photodetector under various illumination intensities at a gate voltage of 1.5 V. The light source used in the experiment was a He-Ne laser with $\lambda = 633$ nm. With an increase in the illumination intensity between 0 and 4.1 mW/cm^2, the drain current was enhanced from the bottom curve to the top curve. As a result, the maximum responsivity of the nanowire MOSFET photodetector was calculated to be 1×10^2 A/W, which is higher responsivity than that of the conventional pn junction photodiode.[8] The basic operational principle of the photodetector is as follows.[2,6,7] The differences in Fermi level between the gate, the polycrystalline silicon, and the p-substrate cause built-in band bending in the channel region. The incident light to the gate generates electron-hole pairs (EHP) and a

(a)   (b)
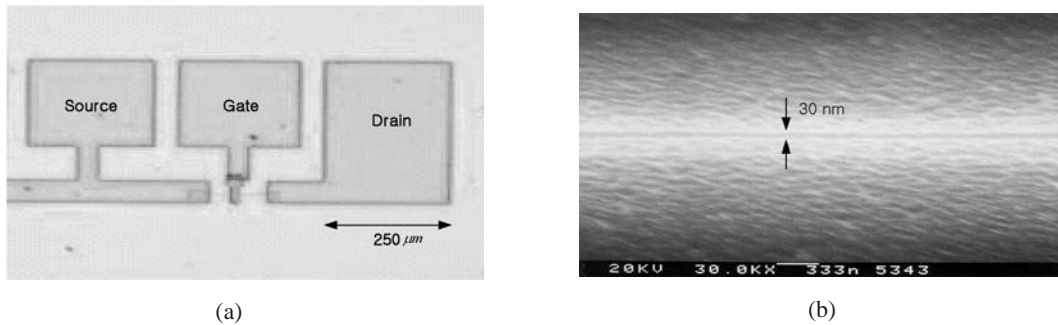
Fig. 1.   The fabricated SOI NMOSFET. (a) Photograph of the device. (b) SEM image of the 30-nm-width silicon wire.
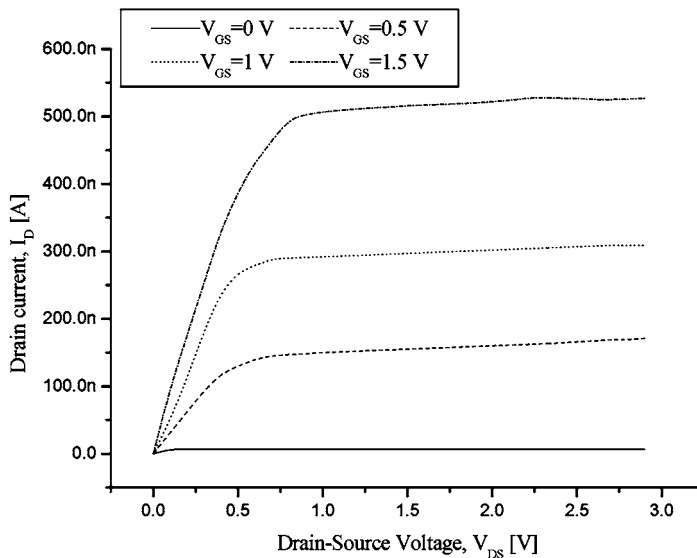

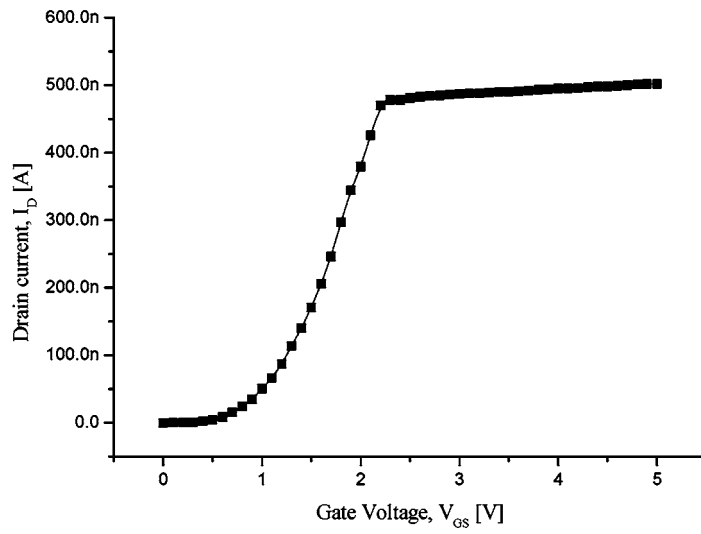Fig. 2.   Measured drain current characteristics as a function of drain voltage.

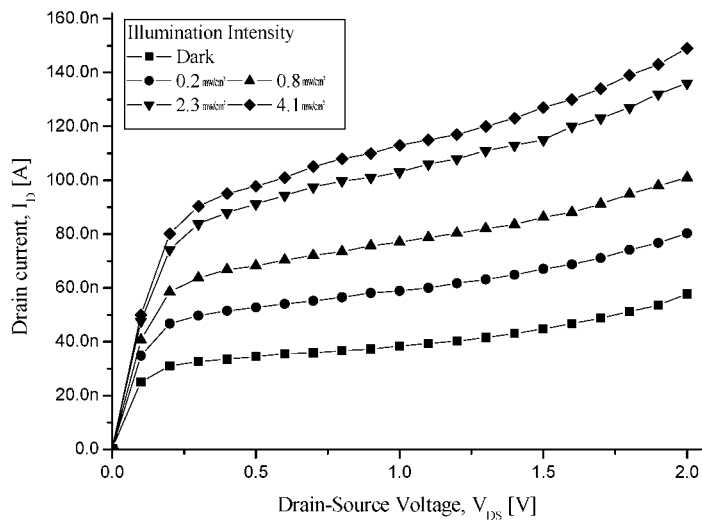Fig. 3. The measured drain characteristics as a function of gate voltage at a drain voltage of 0.1 V.

Fig. 4.   The drain current characteristics of the nanowire photodetector under various illumination intensities.

built-in field caused by the band bending separates the photogenerated EHP vertically. Electrons drift toward the channel and are then quickly swept to the drain by the bias voltage, whereas holes move away to the opposite side and experience a higher potential barrier than the electrons. Thus, these holes are effectively accumulated, and the operational principle of this device is similar to that of a heterojunction bipolar transistor. These accumulated holes lower the potential barrier for electrons, and then electrons can flow more easily through the channel. Consequently, a highly amplified photocurrent can be obtained. This result can be used to implement a high-responsivity photodetector.

3. The Design of SOI CMOS Image Sensor

Designers need model parameters in order to simulate SOI MOSFET circuits. Therefore, SOI MOSFET model parameters have been extracted and investigated for circuit simulation. We fabricated n-type SOI MOSFETs. The channel lengths of the fabricated SOI MOSFETs were 2 μm, and the channel widths varied between 2 and 20 μm. A GPIB-based PC and an HP 4145 parameter analyzer were used to measure the I-V characteristics of the SOI MOSFETs.

3.1 *Parameter extraction*

First, the zero-bias threshold voltage was determined from the measured data.[9] These results are given in Table 1. The method for finding the threshold voltage is shown in Fig. 5.

We calculated the SOI MOSFET parameters using the SPICE level 1 model equation for the bulk MOSFET parameter calculations; the thickness of the gate oxide (T_{OX}) was set at 40 nm, the junction depth (X_J) was set at 60 nm, and the temperature was set at 300 K. These parameters are not influenced by channel width because they depend upon the doping concentration level and the basic structure of the SOI MOSFETs. The calculated parameters of the SOI MOSFETs are given in Table 2.

The SOI MOSFET parameters were optimized by varying specific elements using SPICE; which include delta, delV_{TO}, theta, and K_P. Other parameters were set; these include the substrate doping concentration (N_{SUB}), T_{OX}, X_J, and temperature. The extracted parameters using HSPICE level 2 are shown in Table 3.

A comparison of the optimized parameters with measured elements, is shown in Fig. 6. The simulation results using the measured parameters are similar to the experimental results. The average error rate is 6.42%. When the channel width was larger, the error rate

Table 1
The zero-bias threshold voltage of the measured data.

	W= 2 μm	W= 5 μm	W= 10 μm	W= 20 μm
V_{TO}	–328 mV	–393 mV	–405 mV	–406 mV

was lower. This is due to the fact that the level 2 model has substantial errors in the output impedance and at the transition point between the saturation and triode regions. For narrow devices, the model is inaccurate. Thus, the CIS was designed using the SOI MOSFET with
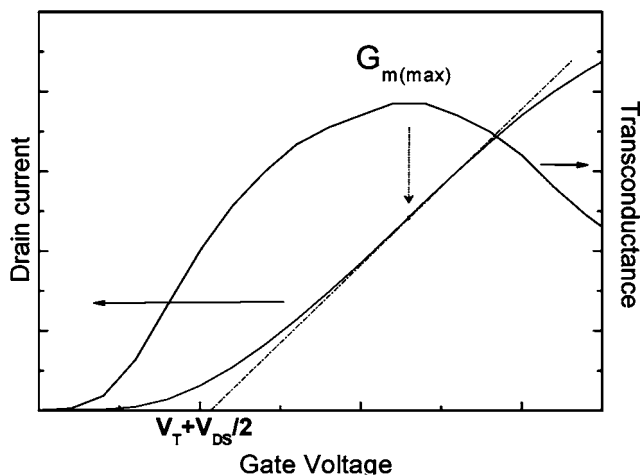

Fig. 5.   The method used for determining the threshold voltage.

Table 2
The calculated parameters of the SOI MOSFET.

V_{TO}	C_{OX}	U_O	lambda	K_p
158.22 mV	863 uf/m^2	600 cm^2/Vs	60 m/V	51.78 A/V^2

Table 3
The optimized parameters using HSPICE.

	$W = 2$ μm	$W = 5$ μm	$W = 10$ μm	$W = 20$ μm
V_{TO} [mV]	−495	−495	−478	−418
K_P [μA/V^2]	58.20	58.20	56.20	57.20
lambda [m^{-1}]	70	70	85	85
delV_{TO} [mV]	−260	−260	−240	−180
V_{MAX} [m/s]	1E + 6	3E + 5	5E + 5	5E + 5
delta	4	8	10	11
theta [V^{-1}]	0.06	0.15	0.18	0.19

a width of 20 μm.

3.2 *The design of the SOI CMOS image sensor*

We simulated a unit pixel for the design of the CIS by using extracted SOI MOSFET model parameters. A nanowire MOSFET with a channel width of 30 nm was used as a photodetector. By using measurement results of the nanowire MOSFET photodetector, the photocurrent was calculated in terms of photointensity. These data were applied to the simulation. Figure 7 shows the schematic of the designed APS structure.

In this schematic, M1 is the reset transistor, while M2 acts as a common drain amplifier. The pulse is applied to the gate of the reset transistor in order to reset the gate voltage of M2 to a high voltage before the start of the current integration. Then, the photodetector discharges the charge stored, which is at the M2 gate, and the resulting voltage is reflected by the common drain amplifier to the output. We compared the SOI APS with the bulk APS using the HSPICE simulation. The simulation results are shown in Fig. 8. The output
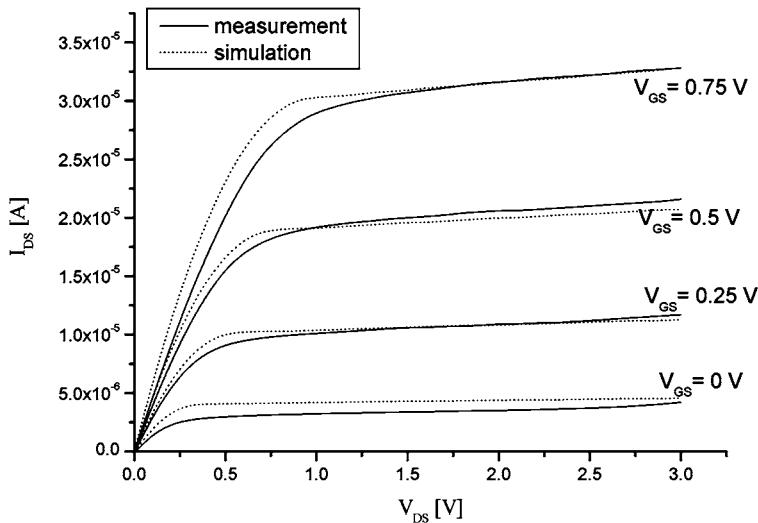

Fig. 6.   The I-V characteristics of the SOI MOSFET (line; measurement, dot; simulation).
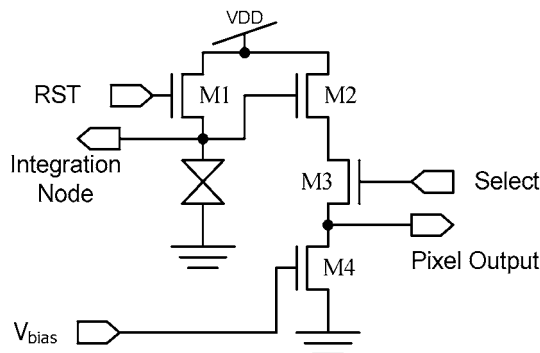

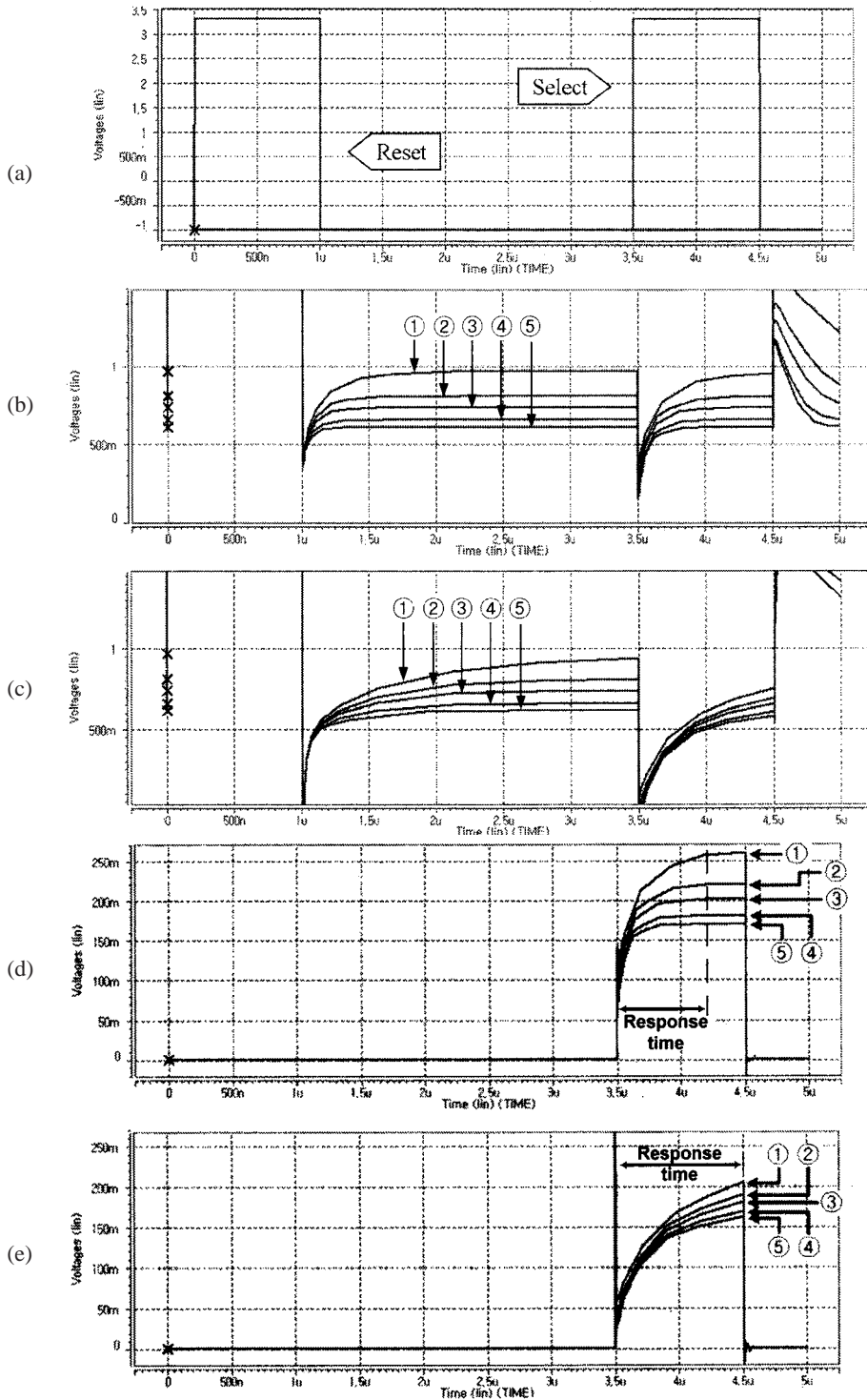Fig. 7.   The schematic of the designed SOI CIS using APS structure

Fig. 8.   The simulation results of the SOI APS and the bulk APS (illumination intensity; ⑩dark, ⒜ 0.2 W/cm², Ⓑ0.8 W/cm², Ⓒ2.3 W/cm², Ⓓ4.1 W/cm²). (a) The control signal. (b) The integration node voltage of the SOI APS. (c) The integration node voltage of the bulk APS. (d) The output voltage of the SOI APS. (e) The output voltage of the bulk APS.

voltage decreases with an increase in illumination intensity. When the photointensity varied between 0 and 4.1 mW/cm^2, the output voltage of the SOI APS varied between 259 and 170 mV and the output voltage of the bulk APS varied between 202 and 160 mV. The response times of the SOI APS and the bulk APS were 0.7 μs and 1.0 μs, respectively. The response time of the SOI APS is shorter than that of the bulk APS. This is because the parasitic capacitance of the SOI APS is smaller than that of the bulk APS.

3.3   *Array simulation*

We performed an array simulation of the SOI CMOS image sensor in order to understand the array characteristics of the designed SOI CMOS image sensor. We compared the output image quality of the SOI CMOS image sensor using a nanowire MOSFET-structure photodetector with that of the bulk CMOS image sensor using a conventional pn junction photodiode.

The block diagram of the CMOS image sensor array is shown in Fig. 9. We simulated the 256×256 array by using a special program. This program designed the HSPICE netlist file of the wanted pixel array and displayed an image that had 256 gray-scale levels from the HSPICE array simulation results file.

Figure 10 shows the array simulation results of the CMOS image sensor. The minimum output voltage is displayed in white and the maximum output voltage is displayed in black. Figure 10(a) is the raw image. Figures 10(b) and 10(c) are the output images of the SOI APS and the bulk APS, respectively. In these figures, the output image of the SOI CMOS image sensor is clearer than that of the bulk CMOS image sensor.
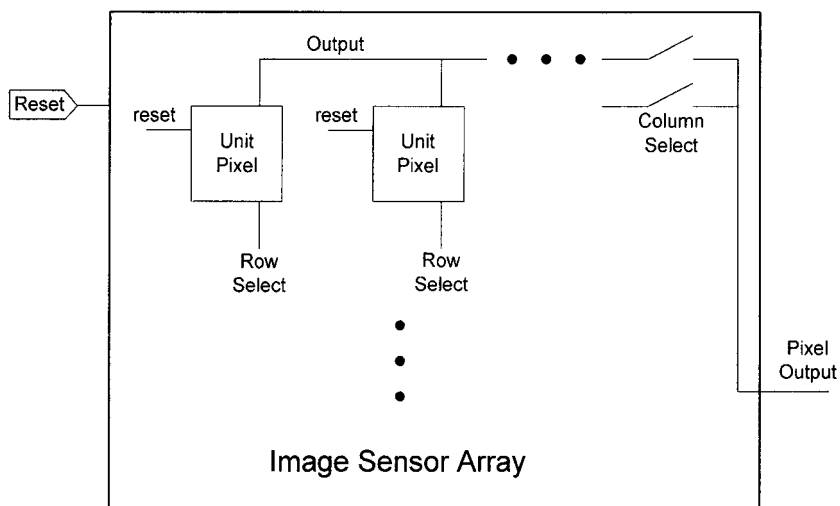

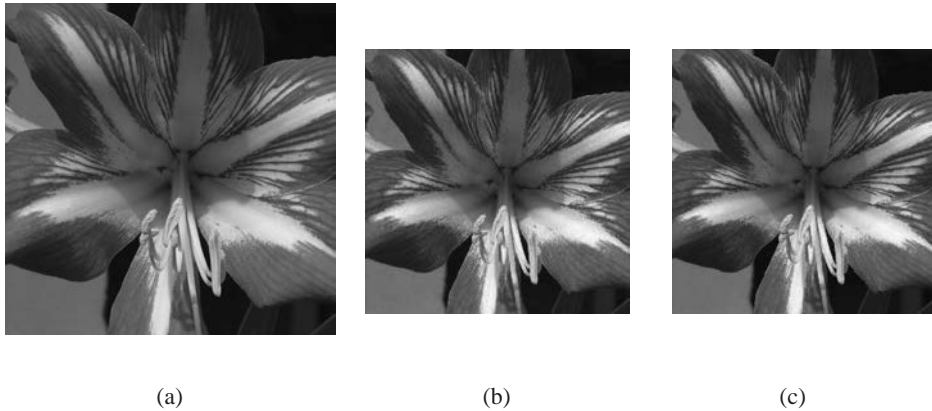Fig. 9.   The block diagram of the CMOS image sensor array.

<div align="center">(a)   (b)   (c)</div>

Fig. 10. Simulation results of the 256 × 256 array. (a) The raw image. (b) The output image of the SOI APS. (c) The output image of the bulk APS.

4.   Conclusion

In this paper, SOI MOSFET model parameters were extracted from the fabricated SOI MOSFETs, and the SOI CMOS image sensor was designed using the parameters. The SOI MOSFET model parameters were calculated using the SPICE level 1 model equation and were optimized using HSPICE by SPICE level 2. The extracted parameters were very similar to the measured data. The APS unit pixel for the CIS was designed and simulated by the extracted model parameters. In this CIS, a nanowire MOSFET photodetector was used. This photodetector works well in low-intensity illumination and has a large dynamic range. The response time of the SOI CMOS image sensor is shorter than that of the bulk CMOS image sensor. The array simulation results showed that the output image of the SOI CMOS image sensor is clearer than that of the bulk CMOS image sensor.

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