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Room Temperature Direct Wafer Bonding for Three Dimensional Integrated Sensors

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This paper reviews the state-of-the-art in room-temperature direct wafer bonding and its application to sensors and materials. The fundamental physical and chemical mechanisms that allow bond energies exceeding 1 J/m^2 to be obtained are discussed. Different techniques and configurations compatible with typical semiconductor production ambient conditions are described and compared to alternate bonding technologies. A variety of test structures and reliability results are presented illustrating the efficacy of the technology. A number of different types of sensor applications including substrates for sensor fabrication, the encapsulation of fabricated sensors, and the integration of sensors in three-dimensional systems demonstrate appropriate utilization of the technology.

1. Introduction

A summary of bonding technologies is given in Table 1. These technologies are compared on the basis of process ambient and capability. With the exception of room temperature (300 K) direct wafer bonding, all of these bonding technologies require at least one of a bond layer (i.e., adhesive, solder, etc.), voltage, pressure, temperature, or vacuum to achieve a bond. These requirements limit the specification of many applications and exclude others from consideration. For example, when materials of significantly different coefficient of thermal expansion (CTE) are bonded at elevated temperatures, a significant postbond strain results at lower temperatures. The resulting residual stress can be sufficient to fracture the bonded materials or otherwise be unsuitable for the application. Likewise, the use of a bond layer typically represents the introduction of an otherwise undesirable material at the bond interface for the application. For example, the fabrication of three dimensional integrated circuits by bonding two dimensional integrated circuits can require the etching and filling of vias through the bond interface. The presence of an adhesive or solder at this bond interface can be problematic for this type of postbond fabrication. The use of a bond layer can also be a limitation for applications that require a postbond temperature in excess of the bond temperature. For example, solders or eutectics are typically limited to postbond temperatures below the reflow temperature and adhesives

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Table 1
Comparison of Room Temperature Direct Wafer Bonding to Other Bonding Technologies.

Bonding Technology	Process Ambient				Process Capability		
	Bond Layer	Voltage	Pressure	Anneal	Vacuum	Hermetic	Die
Eutectic Metal	Yes	No	Some	Some	No	Yes	Yes
Thermocompression	Yes	No	Yes	Yes	No	Yes	No
Fusion (Glass Frit)	No	No	Yes	Yes	No	Yes	No
Adhesive	Yes	No	Some	Some	No	No	Yes
Anodic	No	Yes	Yes	Yes	No	Yes	No
Direct Wafer Bond	No	No	No	Yes	Yes	Yes	No
300 K Direct Wafer Bond	No	No	No	No	No	Yes	Yes

are typically limited to postbond temperatures within 100°C of the cure temperature.

Room temperature direct wafer bonding does not suffer from these limitations because a high density of covalent bonds are spontaneously formed at room temperature by simply placing surfaces into contact after suitable surface preparation. The density of covalent bonds is sufficiently high that bond energies exceeding 1 J/m^2 are obtained. These bond energies are adequate to withstand CTE induced mismatch > 10^{-3} ppm at 100 mm scale, and shear forces induced by high-throughput backgrind or chemical mechanical polish thinning processes. The bonding is intrinsically hermetic as expected from the high density of covalent bonds and the lack of any bond layer that may be susceptible to helium diffusion.

2. Room-Temperature Direct Wafer Bonding Methods

Direct wafer bonding has been used to obtain high bond energies for about 20 years.[1–3] The direct wafer bonding process typically includes the steps of polishing, cleaning, bringing surfaces into contact to form van der Waals bonds, and annealing to convert weak van der Waals bonds to strong covalent bonds. A number of different approaches to cleaning including plasma and a variety of wet processing techniques have been used, but they are typically followed with a water rinse.[4]

The typical bond energies resulting from this conventional direct wafer bonding of 100 mm plasma enhanced chemical vapor deposition (PECVD) silicon oxide coated silicon wafers are shown in Fig. 1.[5] These and other bond energies reported in this paper were obtained by the crack opening method. This figure shows the increase of bond energy with postbond time and temperature. However, postbond temperatures in excess of 400°C for an extended period of time are typically required to achieve a sufficient bond energy (~ 1 J/m^2) adequate for a broad range of applications and postbond processing. These postbond temperatures are clearly unacceptable for a number of applications. Furthermore, the generation of voids at the bond interface, attributed to water vapor resulting from the conversion of weakly bonded hydroxol groups to covalent oxygen bonding according to eqs. (1),[4] is often observed with these postbond anneal cycles.

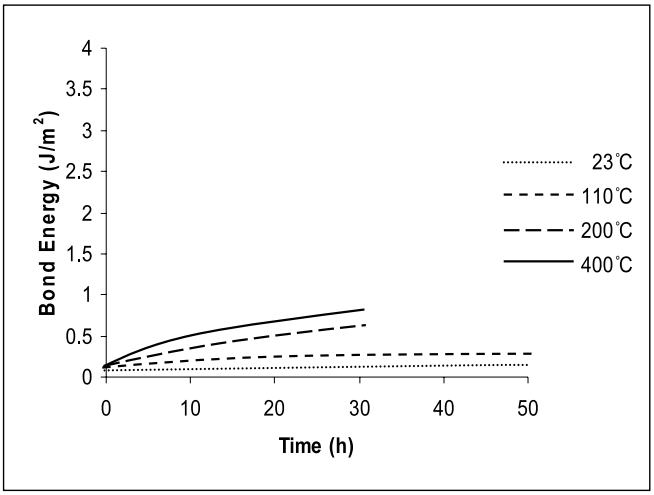

Fig. 1. Typical bonding energy vs time for conventional direct wafer bonding at postbond temperatures of 23°C, 110°C, 200°C, and 400°C of 100 mm PECVD coated silicon wafers.

$$\text{Si-OH} + \text{Si-OH} = \text{Si-O-Si} + H_2O \quad (1)$$

A direct wafer bonding technology capable of achieving bond energies in excess of ~ 1 J/m^2 without heating is clearly desirable for the technology to be broadly applicable. It is further desirable to be able to heat bonded wafers to temperatures higher than 1000°C for some applications; for example, sensor fabrication from silicon bonded wafers that requires thermal oxide growth. A direct wafer bonding technology with these bond characteristics has been developed trademarked as ZiROC, and patented.[6]

The ZiROC direct wafer bonding technology is capable of achieving very high bond energies greater than ~ 1 J/m^2 at room temperature. These high bond energies are attributed to a very high density of covalent bonds formed spontaneously as a result of appropriate surface preparation, followed by initiating contact between two appropriately prepared surfaces. The appropriate surface preparation consists of a mechanical and chemical specifications. The purpose of the mechanical specification is to produce a sufficiently planar and smooth surface of a wafer or die such that the bond energy resulting from the direct bonding of two such surfaces is sufficient to deflect bonded wafer or die to eliminate any gaps resulting from direct contact between two surfaces with nonzero surface bow, warp, planarity, or roughness. The purpose of the chemical specification is to remove all surface contaminations, achieve a minimum absorption to predetermined surface reaction byproducts, and terminate surface atomic bonds of the first surface with a species that self-reacts with a comparably prepared second surface to form covalent bonds and predetermined surface reaction byproducts that are absorbed by prepared surfaces at room temperature.

This bonding technology is broadly applicable to any surface by the deposition or growth of an oxide or nitride followed by chemical mechanical polishing (CMP) to obtain the suitable mechanical specification. This generic implementation also allows a similar

chemical specification to be used for bonding a wide variety of disparate materials. After the mechanical specification is met, a wafer may be singulated into die if dies-to-wafer vs wafer-to-wafer bonding is desired. An example of a suitable chemical specification for a typical silicon oxide coated wafer or die is given below.

(1) Removal of surface contaminants with RCA cleaning solution
(2) Increase silicon oxide surface porosity with an inert RIE process
(3) Expose porous silicon oxide surface to aqueous ammonium hydroxide

After two wafer and/or die surfaces are prepared according to these mechanical and chemical specifications, contact between their respective surfaces is initiated. This is typically accomplished in a wafer-to-wafer alignment tool for wafer-to-wafer bonding, or a pick-and-place tool for die-to-wafer bonding. After contact is initiated, the reaction given by eq. (2) spontaneously occurs.

$$Si\text{-}NH_2 + Si\text{-}NH_2 = Si\text{-}N\text{-}N\text{-}Si + 2H_2 \quad (2)$$

The reaction byproducts of eq. (2) are preferable to those of eq. (1) in that the absorption for a given silicon oxide surface porosity is greatly enhanced. This increased absorption substantially reduces the byproduct concentration, drives the reaction to completion, increases the interface covalent bond density and achieves a very high bond energy. This bond energy is obtained without the need for externally applied pressure, temperature, voltage, or vacuum required by other bonding technologies. The result is a bond with reduced residual stress that requires a minimal tool set to achieve the bond.

The typical bond energy that results from the ZiROC bond is shown in Fig. 2.[5] As in Fig. 1, this figure shows the bond energy increasing with postbond time and temperature for 100 mm PECVD silicon oxide coated silicon wafers. However, distinct from Fig. 1, the ZiROC bond is capable of exceeding bond energies of 1 J/m^2 at room temperature. This increase in

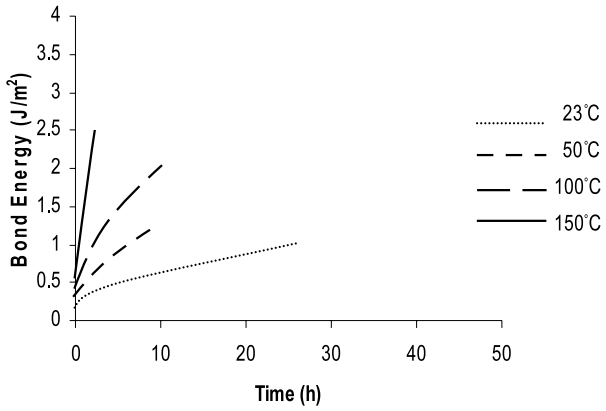

Fig. 2. Typical bonding energy vs time for ZiROC room-temperature direct wafer bonding at postbond temperatures of 23°C, 50°C, 100°C, and 150°C of 100 mm PECVD coated silicon wafers.

bond energy is consistent with an increasing density of covalent bonds. Furthermore, very modest temperature increases after bonding, as small as 25°C, are capable of substantially increasing the rate of postbond bond energy increase. These modest temperature increases are typically benign to the covalent bonds formed immediately after bonding and can thus be used to substantially reduce the time to achieve maximum bond strength for optimum throughput in a production environment.

A number of variations of the ZiROC direct wafer bonding technique described are possible. For example, when bonding a silicon wafer to a second wafer, it is possible to bond the silicon directly to a second wafer coated with silicon oxide. In a second variation, the mechanical specification of the bond surfaces need only be met on the surfaces to be bonded and not on the entire wafer and/or die surface. For example, an encapsulation cavity can be formed by etching a recess in one wafer and bonding it to another wafer without a cavity as long as the bonding surfaces meet the mechanical and chemical specifications.[7] The direct and covalent nature of the bond is capable of forming a hermetic encapsulation as described in more detail in § 3 below. In a third variation, the chemical specification of the bond surface can be met by exposing the surface to ammonium hydroxide vapor instead of aqueous ammonium hydroxide. This may be desirable for applications sensitive to aqueous ammonium hydroxide exposure, i.e., the encapsulation of exposed aluminum metal or delicate MEMs.

Another variation of the ZiROC direct wafer bonding technique is the bonding of surfaces with exposed metal.[8] When these surfaces are ZiROC direct bonded with an alignment tolerance that results in silicon oxide contacting silicon oxide and metal contacting metal, a low resistance, high isolation electrical connection can be made. The result is a bonding technology suitable for applications currently served by flip-chip solder bump, In-bump, or Au-bump with the advantage of not requiring reflow, pressure, or underfill.

3. Test Structures / Reliabilty

The ZiROC direct wafer bond reliability has been evaluated with a number of test structures representative of bond requirements for typical sensor applications. Reliability data presented here includes pressure sensor temperature and pressure cycling, hermeticity, and pressure burst.

Pressure and temperature cycling reliability was evaluated by the fabrication of a pressure sensor cavity with ZiROC direct wafer bonding followed by pressure and temperature cycling tests according to the Automotive Engineering Council specification.[9] Pressure sensor fabrication consisted of etching cavities to form silicon diaphragms in a 100 mm CMOS wafer with integrated sensor electronics followed by ZiROC direct wafer bonding a 100 mm chemical mechanical polished PECVD silicon oxide coated silicon wafer to encapsulate the cavities. The die size was 2.5 mm×2.5 mm and the cavity size was 2 mm×2 mm. Void free bonding was verified with an acoustic microscope. Dies were singulated with a dicing saw with a kerf of 0.1 mm resulting in a bond ring of 0.2 mm around the encapsulated cavity. After dicing, 35 of 35 pressure sensors from 3 ZiROC bonded wafers were leak free as determined by testing at 100, 450, and 500 kPa for 15 m with a 1 kPa resolution. These pressure sensors were then temperature cycled from –40 to

125°C with a 15 m dwell and a 5 m ramp at atmosphere pressure for over 1000 cycles and were determined to be leak free.

The hermeticity of the ZiROC direct wafer bond was verified according to MIL-STD-883E.[10] Encapsulation cavities were formed by etching cavities approximately 7 mm×7 mm wide by 0.1 mm deep into a silicon wafer, spaced by 1 mm. Approximately 0.5 microns of a PECVD silicon oxide was deposited then chemical-mechanical-polished on this and a second, unetched, silicon wafer. The ZiROC chemical specification described above was then performed on both wafers and the two wafers were wafer-to-wafer bonded using flat alignment. Void-free bonding was verified with an acoustic microscope. Die approximately 8 mm×8 mm were singulated with a dicing saw with a kerf of 0.1 mm resulting in a bond ring of 0.5 mm around the encapsulated cavity. Singulated dies were then pressurized in a helium ambient and immediately placed in a vacuum chamber with a residual gas analyzer and a calibrated helium leak. The helium partial pressure was measured as a function of time after helium pressurization. The results obtained are given in Fig. 3, indicating compliance to the fine leak specification of MIL-STD-883E by an order of magnitude. The singulated dies were also tested for gross and fine leaks by a vendor and found to be hermetic according to MIL-STD-883E.

The bond energy of an encapsulation cavity was measured by ZiROC direct bonding an encapsulating die over an orifice in a wafer and increasing pressure in the resulting bonded cavity through the orifice until debonding or fracture of the bonded materials.[11] The encapsulating die was made from a 100 mm, 0.5-mm-thick borofloat. The ZiROC mechanical specification was achieved by depositing a silicon oxide PECVD layer and chemical mechanical polishing to a thickness of approximately 2 microns. The silicon oxide was then patterned with a 0.5-mm-thick rim, with a 7 mm×7 mm square exterior dimension, using photolithography and etched to the borofloat. Then, 7 mm×7 mm dies with a 0.5 mm rim were diced from the 100 mm borofloat wafer, and ZiROC direct bonded to a 0.5-micron PECVD silicon oxide coated silicon wafer with a Datacon 2200 apm pick-and-place tool. The silicon wafer had 2 mm×4 mm slots etched through the wafer prior to bonding. After bonding, the cavities were pressured through the slot until failure.

Two failure modes were observed, debonding of the borofloat die or the fracture of the borofloat interior to the bond rim. Failure pressures below 140 psi were typically due to debonding and failures at 140 psi were typically due to the fracture of the borofloat. Failure

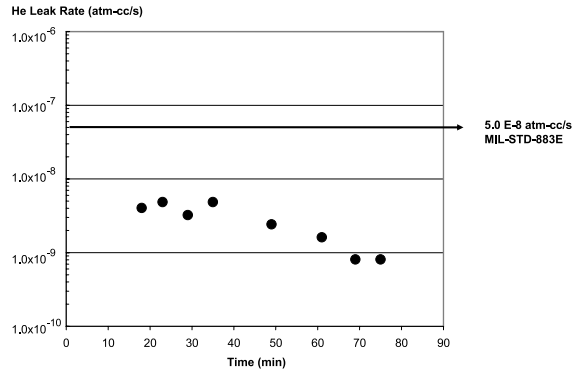

Fig. 3. Helium partial pressure vs posthelium pressure time for ZiROC bonded silicon cavity to silicon wafer.

pressures in excess of 100 psi were typically observed after one day at room temperature as shown in Fig. 4. This failure pressure corresponds to a bond energy of about 0.5 J/m^2, or about half of the bond energy expected from Fig. 2 for critical loading resulting in adhesive failure to a rigid medium for a bonded disk with a small penny shaped crack under uniform pressure.[12] Failure pressures of 140 psi resulting in fracture of the borofloat interior to the bond rim were typically obtained for ZiROC bonded after baking at 100°C for one hour.

3. Applications

The demonstrated capability of the ZiROC direct wafer bond to achieve a very high bond energy at room temperature is enabling for applications that require a bond technology without residual stress, or a minimum bond energy for postbond fabrication or use, that would otherwise be detrimental to the bonded materials. There are a number of applications for the fabrication of substrates for sensor fabrication, encapsulation of sensors, and three-dimensional integration of sensors that require or benefit from this bond capability. Two examples of applications for the fabrication of substrates for sensor fabrication are temperature compensated surface acoustic wave (SAW) RF filters, and silicon-on-insulator (SOI) or silicon-on-quartz (SoQ) wafers for CMOS IC wafer fabrication.

SAW devices fabricated from piezoelectric substrates like lithium tantalite and lithium niobate have a significant temperature coefficient of frequency (TCF) that results from the high coefficient of thermal expansion (CTE) of these materials. The high TCF precludes the use of SAW RF filters in some applications like US PCS duplexers. The fabrication of

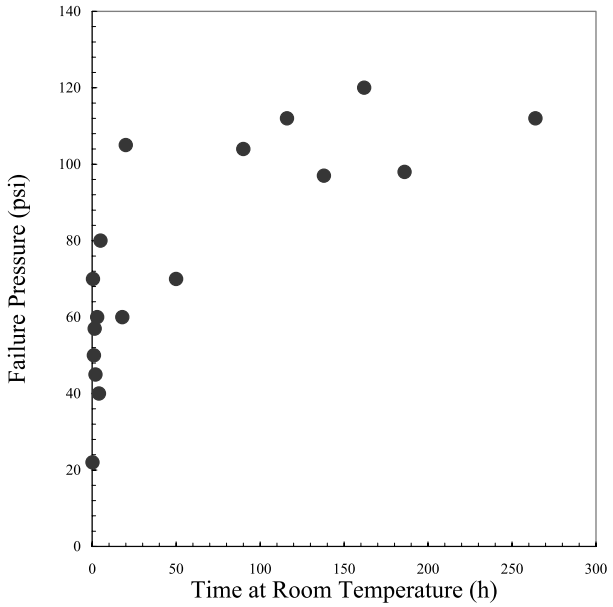

Fig.4. Failure pressure vs postbond time for ZiROC bonded borofloat cavity to silicon wafer with orifice.

SAW RF filters from ZiROC bonded temperature-compensated substrates (TCS) can reduce the TCF by about half and allow the UC PCS duplexer specification to be met with an RF SAW filter.[13] A TCS is fabricated by bonding a high-CTE piezoelectric material to a low-CTE material using the ZiROC bond technology. Examples of low-CTE materials include silicon, sapphire, and fused quartz. RF SAW filters fabricated from TCS substrates exhibit a substantial reduction in TCF due to a reduction in the piezoelectric CTE on a TCS substrate. A TCS substrate fabricated with a ZiROC bond has a greater reduction in TCF than a TCS substrate fabricated with a conventional direct wafer bond because a bond strong enough to restrain the high-CTE mismatched materials from slipping against each other is created at a lower temperature. Furthermore, TCS substrates fabricated with a ZiROC bond have the advantage of minimum bow during typical room-temperature SAW filter pattern definition, because TCS wafers bonded at elevated temperatures exhibit a residual bow resulting from the CTE mismatch and the elevated temperature. Moreover, TCS wafers bonded at elevated temperatures are subject to fracture when cooled to room temperature due to tensile stress in the brittle piezoelectric material.

Thin-and thick-film SOI and SOQ wafers are desirable substrates for a number of applications including high frequency low-power CMOS IC fabrication micro-electro-mechanical systems (MEMS) and active matrix or thin film transistor (TFT) LCD displays. As with TCS substrates, SOI or SOQ wafers are subject to residual stress when fabricated using a direct wafer bonding technology that requires an elevated temperature to obtain a high bond energy. The ZiROC bond eliminates this component of stress in these materials, which can facilitate improved sensor sensitivity, uniformity, reproducibility, and reliability. The potential for stress reduction in SOQ wafers is greater than in SOI wafers due to the CTE mismatch between silicon and quartz.

An additional requirement for some thin-and thick-film SOI applications is thermal silicon oxide growth compatibility that requires postbond temperatures higher than 1000°C. SOI wafers with an insulator (silicon oxide) thickness of less than 150 nm fabricated with the ZiROC direct wafer bond have been shown to be compatible with thermal oxide growth and not plagued with interface debonding attributed to byproduct accumulation observed with other direct wafer bonding technologies.[5]

Another category of applications that require or benefit from the ZiROC direct wafer bond capability is sensor encapsulation. The ability to obtain very high bond energies at room temperature results in an encapsulation solution with minimal stress compared with conventional encapsulation solutions that rely on adhesive layers, temperature, voltage, and / or pressure. Moreover, the demonstrated hermetic capability of the the ZiROC direct wafer bond is required for sensors that degrade when exposed to moisture. Achieving minimum stress and hermetic capability with a direct bonding technology at room temperature facilitates the scaling of this encapsulation solution from the die scale to the wafer scale at 300 mm or larger. This fundamental ability of the ZiROC direct wafer bond to scale is expected to play a significant role in reducing cost for sensor technologies where packaging cost is significant.

Another category of applications that require or benefit from the ZiROC direct wafer bond capability is the three-dimensional integration or fabrication of sensors. One example of an application for three-dimensional integration of sensors is staring hybrid

focal plane arrays (FPA). These arrays are typically hybridized by In-bump bonding a detector array, often fabricated from InGaAs or silicon,etc., onto a readout integrated circuit (ROIC) electronics array, typically fabricated from silicon. The In-bump bonding can limit the pixel pitch of the FPA and significantly increase cost. Furthermore, in FPA applications where the detector array substrate is not transparent, this substrate must be thinned after bonding to the ROIC. Variable mechanical support of the detector by the ROIC can make thinning problematic. Conversely, FPAs hybridized with the ZiROC direct wafer bond 1) can be fabricated with a sub-tenmicron pitch and 2) the detector is uniformaly supproted by the ROIC, enabling repeatable and reproducible removal of the entire detector substrate if desired.

A three-dimensional FPA can also be fabricated by bonding an ROIC wafer onto a detector array, removing the ROIC substrate, and then etching vias and forming an interconnection between individual pixels in the ROIC and the detector array. Figure 5 provides a scanning electron micrograph (SEM) of a focused ion beam (FIB) cross section of a via with an electrical interconnect ion between an ROIC wafer and a detector wafer. The ROIC wafer was fabricated with an SOI wafer. The ROIC wafer was then ZiROC direct wafer bonded to a detector wafer using silicon oxide with a +/- 1 micron alignment, and the SOI substrate was removed. Two-micron vias on seven-micron centers were then etched and metalized to fabricate a 125,000-via chain with a via resistance less than the ROIC and detector metal sheet resistance. The bond interface was not revealed by the via etching, indicating that the via etching of ZiROC-direct-wafer-bonded silicon oxide is similar to the via etching of homogeneous silicon oxide.

An example of a three-dimensional sensor fabrication application that requires the capabilities of the ZiROC direct wafer bond is symmetric intrinsic heterojunction bipolar transistor (SIHBT) fabrication for millimeter-and sub-millimeter-wave imaging at 35, 94, 140, and 220 GHz for aviation safety and phased array radiometers. SIHBT fabrication requires submicron pattern definition on both sides of a 1-to 2-micron thick multi-layer epitaxial structure.[14,15] Building this structure typically requires patterning one side of the

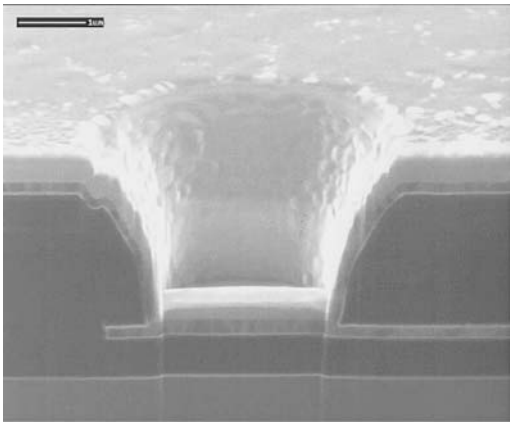

Fig. 5. SEM cross section of FIB cut of ROIC wafer ZiROC bonded to detector wafer with two micron via and metal interconnection between ROIC and detector wafers.

structure with submicron features to fabricate the emitter-base component of the transistor, bonding the partially fabricated transistor to a surrogate substrate, and patterning the second side of the structure with submicron features to fabricate the collector-base component of the transistor. The bonding typically involves materials of different CTEs to obtain optimum frequency, thermal, and impedance matching performance. The ZiROC direct wafer bond eliminates alignment run-out of submicron features due to bonding at elevated temperatures with CTE-mismatched materials that otherwise prohibits wafer-scale transistor and circuit yield.

5. Conclusion

A direct wafer bonding technology capable of exceeding bond energies of 1 J/m^2 at room temperature was reviewed. The versatility of the technology with regard to wafer-to-wafer vs. die-to-wafer bonding format, varying chemical specification, minimum residual strain, pressure and temperature excursions, hermeticity, various cavity formation techniques, and electrical interconnections traversing the bond interface has been shown. The technology is suitable for engineered sensor substrates, sensor encapsulation, and three-dimensional integrated sensor applications.

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