Analog Integrated Circuit for Edge Detection with Massively Parallel Processing Based on Vertebrate Outer Retina

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An analog circuit for edge detection was proposed based on vertebrate outer retinas. In order to realize a wide dynamic range of light intensity, a simple logarithmic compression photocircuit based on a photoreceptor in the retina was utilized at the first stage of a unit circuit. A function for digitizing an output current was inserted at the last stage to solve the problem of incorrect operation caused by noise and device mismatches. The chip which contains 40×40 unit circuits in a two-dimensional array was fabricated with 0.35 μm complementary metal oxide semiconductor (CMOS) process. The measured results of the chip and the results with the simulation program with integrated circuit emphasis (SPICE) showed that edge positions can be detected correctly with a dynamic range of 6 decades. It was clarified that the fabricated chip can detect edge positions even if regions with extremely different brightness levels were contained in an input image. In addition, an edge pattern of a moving object was detected at 100 frames/s and the capability for massively parallel processing was confirmed.

1. Introduction

Real-time image processing is difficult in conventional image processing systems using Neumann-type computers since the information processing is performed in a time-sequential way. However, the image processing is easily accomplished in the biological vision system because the information processing is performed in massively parallel nerve networks with hierarchical structures. Thus, it has been expected that visual sensors, which perform the image processing in real time, can be realized based on biological vision

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systems. Such chips can be applied to information systems for robotics, collision avoidance and others.

In vertebrate outer retinas, the edge position of an input image is detected in real time. The motion of an object is detected in a brain from the edge signals. Analog circuits for edge detection have been proposed based on vertebrate outer retinas.[1–4] The realization of a wide dynamic range of light intensity has been tried by mimicking a horizontal cell in the retina. However, these circuits only had a dynamic range of about 3 decades, although vertebrate retinas have that more than 6 decades. The voltage, which logarithmically depends on the light intensity, is generated at photoreceptors in the retina. Thus, a wide dynamic range could be realized by logarithmic compression.

Moreover, these circuits[1–4] had the problem of incorrect operation caused by noise and device mismatches. Although there are the signal fluctuations in the biological system, output signals of the retina are generated correctly. This is due to the function for digitizing an output signal.

Thus, we tried to fabricate the edge detection circuit with a wide dynamic range using parallel image processing based on vertebrate outer retinas. In order to realize a wide dynamic range, a simple logarithmic compression photocircuit was utilized at the first stage of a unit circuit. A function for digitizing an output current was inserted at the last stage to solve the problem of incorrect operation caused by noise and device mismatches. The measured results of a fabricated chip and the simulation results with the simulation program with integrated circuit emphasis (SPICE) showed that our proposed circuit can correctly detect edge positions with a dynamic range of 6 decades.

2.   Edge Detection Model

An edge detection model based on vertebrate outer retinas is shown in Fig. 1(a). A previously proposed model was constructed with photoreceptors P, horizontal cells H and bipolar cells B. However, the output current of the analog circuit[3,4] fabricated based on the model varied widely due to noise and device mismatches. Thus, $I_{b,i}$ is input to a digitized cell D in our model, which outputs 0 at edge positions and a constant signal at other positions.

Figures 1(b)–1(d) show the output signals from each cell when an object in Fig. 1(a) is projected on the retina. The signal $I_{p,i}$ of P is proportional to light intensity, as shown in Fig. 1(b). A voltage $V_{h,i}$ depends logarithmically on $I_{p,i}$. A wide dynamic range is realized by logarithmic compression. The difference in potential of $V_{h,i}$ occurs near an edge position. A constant signal I_{con} is diffused into neighboring horizontal cells. Then $I_{b,i}$ is generated. $I_{b,i}$ at the nearest edge position is larger than that at other positions, as shown in Fig. 1(c). $I_{b,i}$ is transmitted to D. A threshold signal I_{th} is set in D. When $I_{b,i}$ is larger than I_{th}, the output signal $V_{out,i}$ of D is 0, as shown in Fig. 1(d).

3.   Edge Detection Circuit

A unit circuit based on the model in Fig. 1 is shown in Fig. 2(a). When the light was projected on a photodiode PD_i, a current $I_{p,i}$ which is proportional to light intensity is generated. $I_{p,i}$ is input to a logarithmic compression photocircuit constructed with metal
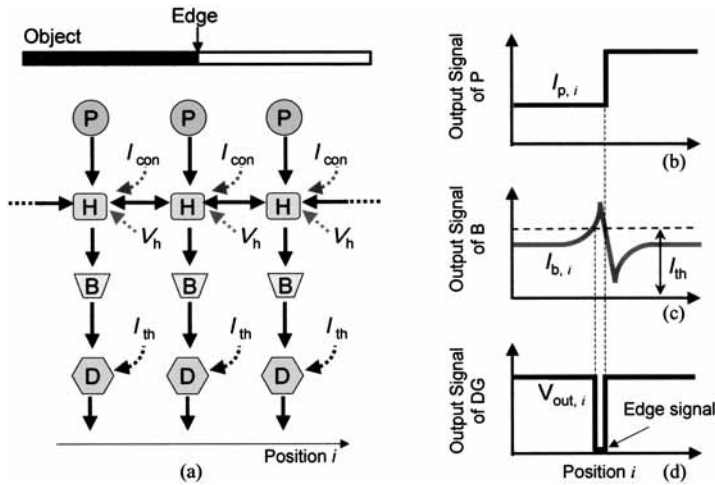
Fig. 1. Edge detection model. (a) Model based on vertebrate retina. (b) Output signals of photoreceptors P. (c) Output signals of bipolar cells B. (d) Output signals of digitized cells D.

oxide semiconductor (MOS) transistors MN_1, MN_2, MN_3 and MP_1[5] on the basis of the photoreceptor. These transistors operate in the subthreshold region. The voltage $V_{h,i}$ is given by the following equation,

$$V_{h,i} = \left(\frac{1+\kappa}{\kappa^2}\right) U_T \log\left(\frac{I_{p,i}}{I_0}\right) + \left(\frac{1+\kappa}{\kappa^3}\right) U_T \log\left(\frac{I_{con}}{I_0}\right),$$

(1)

where I_0, k and U_T are the leakage current, the ratio of capacitive coupling from gate to channel and the thermal voltage, respectively. The voltage $V_{h,i}$ depends logarithmically on $I_{p,i}$ and a wide brightness range is realized by logarithmic compression. In addition, this photocircuit is one of the negative feedback buffer circuits. The advantage of the negative feedback buffer circuit[5] is that the output voltage $V_{h,i}$ hardly depends on the characteristics of the gain stage, which consists of MP_1 and MN_3. Thus, it is expected that the device mismatch error of the gain stage may be reduced to some extent.

A constant current I_{con} is diffused into neighboring unit circuits through a smoothing circuit constructed with pMOS transistors MP_2 and MP_3 since the difference in the voltage $V_{h,i}$ occurs near an edge position. A current $I_{b,i}$ is generated at the smoothing circuit. $I_{b,i}$ at the edge position is larger than that at other positions.

$I_{b,i}$ is input to a digitized circuit constructed with MOS transistors MN_4, MN_5 and MP_4. The output voltage $V_{out,i}$ is represented by the following equation,[3,6]
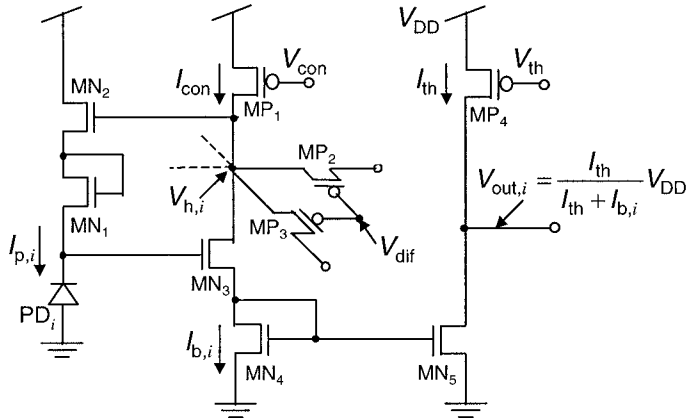
Fig. 2.   Unit circuit for edge detection.

$$V_{\text{out},i} \cong \frac{I_{\text{th}}}{I_{\text{th}} + I_{\text{b},i}} V_{\text{DD}}, \qquad (2)$$

where V_{DD} is the supply voltage. The voltage $V_{\text{out},i}$ is about 0 at the edge position since $I_{\text{b},i}$ is larger than the threshold current I_{th}. On the other hand, the voltage $V_{\text{out},i}$ at the other positions becomes about V_{DD} since $I_{\text{b},i}$ is smaller than I_{th}. Similarly, when the incorrect signals of $I_{\text{b},i}$ due to noise and device mismatches are smaller than I_{th}, the digitized circuits output about V_{DD}. Thus, the digitized circuit can reduce the incorrect signals. In the unit circuit in Fig. 2(a), MP_2 and MP_3 are utilized as the smoothing circuit. In this circuit, the control of V_{dif} is needed in each case.[2–4]

4.   Experimental Results

The logarithmic compression photocircuit in Fig. 2(a) was fabricated with a 0.35 μm CMOS process through VLSI Design and Education Center (VDEC). Measured results and simulation results with SPICE are shown in Fig. 3. V_{con} and V_{DD} were set to 2.4 V and 3V, respectively. $I_{\text{p},i}$ was varied from 1 pA to 1 μA. The Level 49 SPICE model parameter provided via VDEC was used for simulation. As shown in Fig. 3, the measured results were approximately equal to the simulation results. The voltage $V_{\text{h},i}$ depended logarithmically on $I_{\text{p},i}$ in a range of 6 decades. Therefore, a dynamic range of 6 decades is realized by the edge detection circuit using the logarithmic compression photo-circuit.

A chip for edge detection, which contains 40×40 unit circuits in Fig. 2(a) were arranged two-dimensionally , was fabricated with the same process. The area of the unit circuit was 88×88 μm². The schematic of the measuring equipment is shown in Fig. 4(a). The image generated with a personal computer (PC) was irradiated on the chip through a lens using a projector. A photograph of the chip is shown in Fig. 4(b). $I_{p,i}$ generated at white and black regions were I_{max} and I_{min}, respectively. I_{th} was set to 13 nA. V_{dif} was changed in each measurement. While the chip operated in parallel, output signals of $V_{\text{out},i}$ were obtained
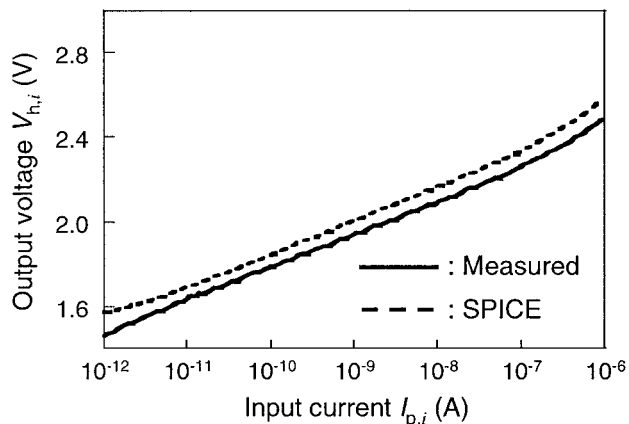
Fig. 3.   Relationship between input current $I_{p,i}$ and output voltage $V_{h,i}$.

with a time-sequential display system by using two external shift registers (vertical and horizontal shift registers). On every clock cycle, the output signal of a unit circuit selected by the vertical and horizontal shift registers was read out and transferred to an A/D converter one by one. This measurement process was repeated and a time-sequential data was formed. The time-sequential data was transformed to a two-dimensional image by software running on a PC every one frame. The results are shown in Fig. 5. The image of the edge positions is represented as black. The chip detected edge positions successfully.

In addition, a moving object was projected on the chip, and the edge patterns of the moving object were measured. The object moved along an arrow shown in Fig. 6(a). Output signals were obtained at 100 frames per second using the external shift registers. The results are shown in Figs. 6(b), 6(c), and 6(d). It was confirmed that the edge patterns of the moving object were successfully detected at 100 frames/s.

5.   Discussion

An analog circuit for edge detection was proposed based on vertebrate outer retinas. The measured results in Fig. 5 show that the fabricated chip can detect edge positions. However, edge detection with a dynamic range of 6 decades could not be confirmed since the image with a brightness range of 6 decades could not be provided by the measuring equipment in Fig. 4(a). The measured results of the logarithmic compression photocircuit showed that the voltage $V_{h,i}$ depended logarithmically on $I_{p,i}$ in the range of 6 decades. Therefore, it was expected that the fabricated chip can generate edge signals even if an image with a brightness range of 6 decades is projected.

As compared with the previous proposed edge detection circuits,[1–4] the proposed circuit has a wider dynamic range of light intensity. This is due to the insert ion of a simple logarithmic compression photocircuit based on a photoreceptor in a retina to the first stage of a unit circuit.

The previous proposed circuits[1–4] had a problem of incorrect operation caused by noise and device mismatches. Our fabricated chip could detect edge positions, as shown in
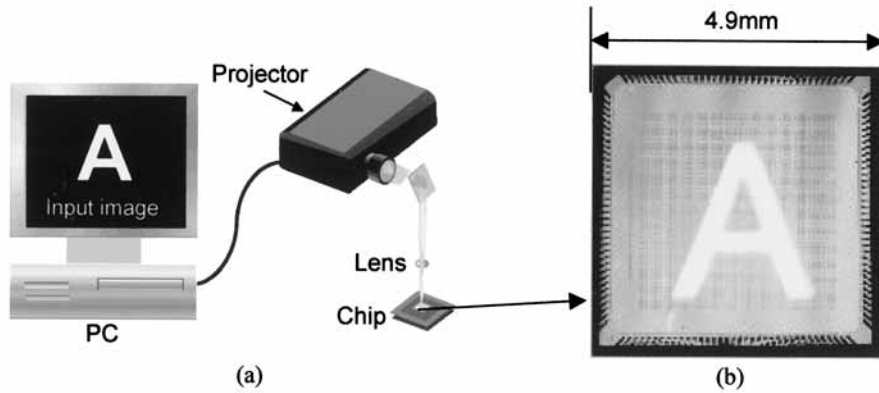
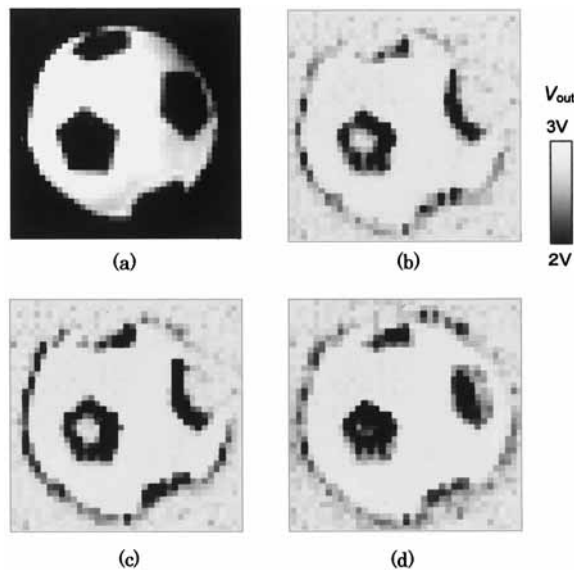Fig. 4.   (a) Schematics of measuring equipment. (b) Photograph of chip.

Fig. 5.   Measured results of edge detection chip. (a) Input image, (b) I_{max}=6.9 nA, I_{min}=530 pA, V_{dif}= 1.0V. (c) I_{max}=1.43 nA, I_{min}=34 pA, V_{dif}=0.9 V. (d) I_{max}=510 pA, I_{min}=6.2 pA, V_{dif}=0.7 V.

Fig. 5. Thus, it was clarified that the problem of incorrect operation is solved by inserting a function for digitizing an output current to the last stage of a unit circuit.

We proposed analog circuits for motion detection based on the biological vision system.[3, 6,7–9] Edge detection circuits proposed by H. Yamada *et al.* were inserted to the first stage of motion detection circuits. Therefore, previous proposed motion detection circuits had only the dynamic range of about 3 decades. The motion detection chip with a wide dynamic range can be realized by inserting the proposed edge detection circuit to the first stage of motion detection circuits.

    As shown in Fig. 6, the chip can detect edge patterns at 100 frames/s. The frame rate was limited by the maximum clock speed of the external shift registers. However, the chip operated in parallel and the response time in each unit circuit could be shorter than the clock of the external shift registers. It was assumed that the response time was about several ten microseconds. Thus, if the edge signals are output by optical signals from each unit circuit, the edge pattern will be observed instantaneously.

    For realization of these novel systems, i.e., optoelectronic integrated circuits (OEICs), it has been an essential technology to combine III -V compound semiconductors with Si. We have already succeeded in the growth of a dislocation-free Si/GaPN/Si structure by molecular beam epitaxy.[10] Novel OEICs could be constructed based on the Si/GaPN/Si structure. Optical devices, which consist of III-V-N alloys, would replace the GaPN layer. Integrated circuits could be formed on the top Si layer. Recently, an InGaPN/GaPN double-heterostructure light-emitting diode (LED) was fabricated on a Si substrate.[11] Moreover, a fabrication process for OEIC has been investigated and surface inversion was obtained in a MOS diode fabricated on the Si/GaPN/Si strucutre.[12] Combining these technologies, edge detection circuits with LED could be realized and operate in a massively parallel manner.
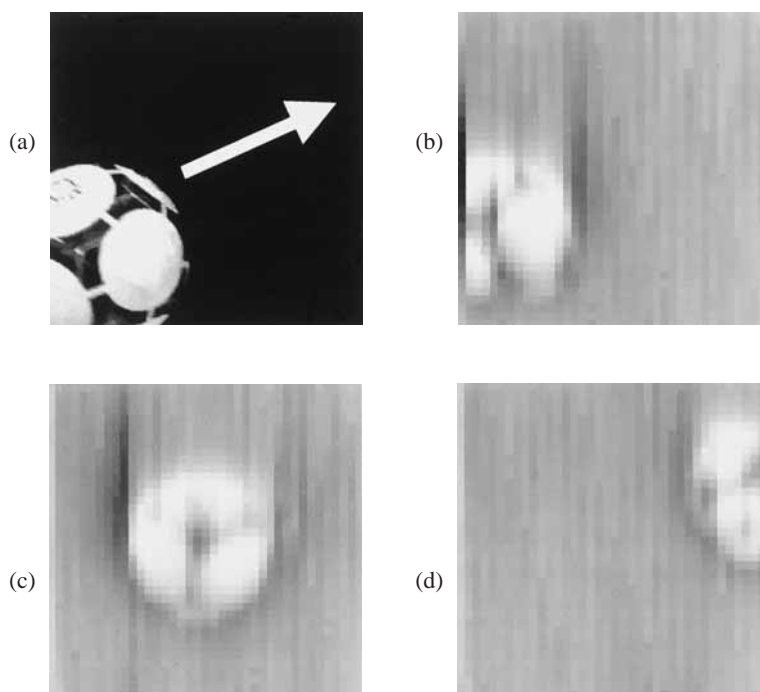

Fig. 6.   Measurement results of edge detection in moving object (a): Input image at t=0 s. A white arrow shows the direction of the moving object. (b), (c) and (d): Output images at t=0, 0.3 and 0.7 s, respectively.

6. Conclusion

An analog circuit for edge detection was proposed based on vertebrate outer retinas. In order to realize a wide dynamic range of light intensity, a simple logarithmic compression photocircuit based on a photoreceptor in the retina was utilized at the first stage of a unit circuit. A function for digitizing an output current was inserted at the last stage to solve the problem of incorrect operation caused by noise and device mismatches. The measured results of the chip fabricated with a 0.35 μm CMOS process and the simulation results with SPICE showed that edge positions could be detected correctly with a dynamic range of 6 decades in the constant condition. In addition, an edge pattern of a moving object was detected at 100 frames/s and the capability for massively parallel processing was confirmed.

Acknowledgement

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