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Wafer Level Lateral Bonding Scheme with LEGO-Like Structure

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A wafer level lateral bonding scheme is presented as an alternative to MEMS packaging applications. The proof-of-concept structure is fabricated and evaluated to confirm the feasibility of the new scheme. The most distinct difference between this new scheme and conventional ones is that wafers are laterally bonded by solder reflow with a new apparatus. This lateral bonding scheme has merits in that it is morphologically insensitive and enables not only hermetic sealing but also electrical via-interconnection. Bonding strength is evaluated under shear and the hermeticity of encapsulation is examined using the pressurized helium leak detection method based on MIL-STD 883E. Results show that the new scheme is feasible as an alternative method for high-yield wafer level packaging.

1. Introduction

Recently, there has been a strong demand for high-yield wafer level packaging (WLP) for MEMS applications. WLP is a major challenge in the commercialization of MEMS and thus, has become a bottleneck for the success of MEMS industry.[(1,2)] As the application of MEMS devices is now extending over diverse fields, various MEMS packaging methods have been studied by many researchers.

Generally, glass-silicon anodic bonding,[(3)] Si fusion bonding,[(4)] eutectic bonding[(5)] and adhesive (glass-frit,[(6)] solder,[(7,8)] polymer [(9)] and so forth) bonding are widely used for the hermetic sealing method, and these techniques are mainly classified into two categories in terms of the bonding interface as described in Table 1. (1) The "surface" bond schemes, such as the anodic, fusion and eutectic bondings, require a flat surface for the intimate contact making it difficult to make feed-through out of hermetic encapsulation. Also, the Si fusion bonding is normally achieved at high temperatures (> 800°C), which may be harmful to the MEMS device. Thus, many researchers have suggested the localized heating techniques to solve such a thermal budget in a high-temperature bonding pro-

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Table 1
Comaprisons of wafer bonding techniques.

Techniques		Advantages	Drawbacks
"Surface" Bond		hermetic, vacuum	flat surface required
surface	anodic	strong bond	high V (~1kV)
	fusion(direct)	strong bond	high temp.(>800°C)
	surface-activated	varies	varies
"Interlayer" Bond		hermetic, nonflat OK	specific material
metallic	eutectic (Au/Si)	hermetic, vacuum, strong bond	flat surface required
	solder	self-aligning	solder flow
	Thermo-compression	nonflat OK	high force, crack
insulating	glass-frit	hermetic, vacuum, strong bond	large area, med. high temp
	adhesive	versatile	outgassing
	photoadhesive	narrow pattern	outgassing

cess.[7,10] On the other hand, (2) the "interlayer" bond schemes such as the solder, glass-frit and adhesive bondings, have advantage over the nonflat surface, but they also have certain drawback such as outgassing of interlayer.

In this paper, we present a new wafer level bonding scheme that is less sensitive to both the wafer flatness and wafer warpage.

2. Concept and Design

Wafer bonding is one of the key technologies in MEMS and its processing yield fundamentally depends on its bonding principle. As illustrated in Table 1, in the case of rough surface morphology, the interlayer bonding techniques are more useful than the other techniques due to their morphological insensitivity.[6–9] However an additional pressure is usually applied to obtain wafers with warpage intimate contact because the

wafer warpage is inevitably accompanied by the fabrication process. This pressure can make the interlayer wider, which has been a hurdle in size reduction.

This study begins with the solder reflow as shown in Fig. 1(a). When the solder materials melt, they have the tendency to minimize the surface energy, resulting in the ball formation on the circular wetting layer, because the ball shape has a minimal surface area per unit volume. This principle of surface energy minimization is also the key to the self-alignment mechanism in flip-chip technology.[11,12]

In this paper, we present a scheme for resolving the drawback caused by the "face-to-face" bonding principle. A major difference between this new scheme and conventional ones is that wafers could be laterally bonded by solder reflow (see the right side of Fig. 1(b)). The solder, when it melts, reflows along the wetting layer of the Under Bump Metallurgy (UBM) and, when it meets that on the other wafer, lateral bonding will begin. Thus, this bonding apparatus gives more advantages in grated topology, and furthermore, can avoid the notching problem in electrical via-interconnection because it is possible to bond together without intimate contact.

The schematic of the proof-of-concept structure is shown in Fig. 2. The peripheral solderline for encapsulation is defined by trench and solder lines. Also, it is a key to the concept that the solder must be surrounded by the wetting layers and trench wall.

The design parameters are determined as shown in Table 2, where S_{TS} is the spacing between the trench and the solder, S_{US} is the spacing between the wetting layer of the UBM and the solder, H_T is the trench height, H_S is the solder height, W_T is the trench width, W_S is the solder width and W_U is the UBM width. S_{TS} and S_{US} are the allowances of alignment, and in this study; they were fixed at 3 µm and 8 µm, respectively.

It must be noted that lateral bonding can be inevitably completed by the solder reflow only if wafers are assembled in a LEGO-like formation and heated, which makes it possible to achieve a high processing yield.

3. Results and Discussion

The proposed scheme basically comprises three processes: (1) the capping wafer fabrication process, (2) bottom wafer fabrication process and (3) bonding process with a LEGO-like assembly. The seal line for encapsulation is defined by Si deep RIE and a thick tin (Sn) solder as an adhesive is electroplated. Finally, the capping and bottom wafers are laterally bonded by solder reflow with a LEGO-like assembly. Pure tin is chosen as a solder material because it has a simple composition and can easily realize the feasibility of the scheme.

3.1 *Capping wafer fabrication process*

The capping wafer of fabrication the proof-of-concept structure was fabricated using micromachining technology as described in Fig. 3. The process started with 300-µm-thick double-side-polished silicon. The silicon substrate was etched by deep RIE for cavity encapsulation (Fig. 3(a)). An AZ 9260 photoresist was spray-coated and patterned after 1.2-µm-thick oxide was deposited (Fig. 3(b)). The peripheral seal line for encapsulation was defined by the Si deep RIE (Fig. 3(c)). The oxide layer was laterally etched to create

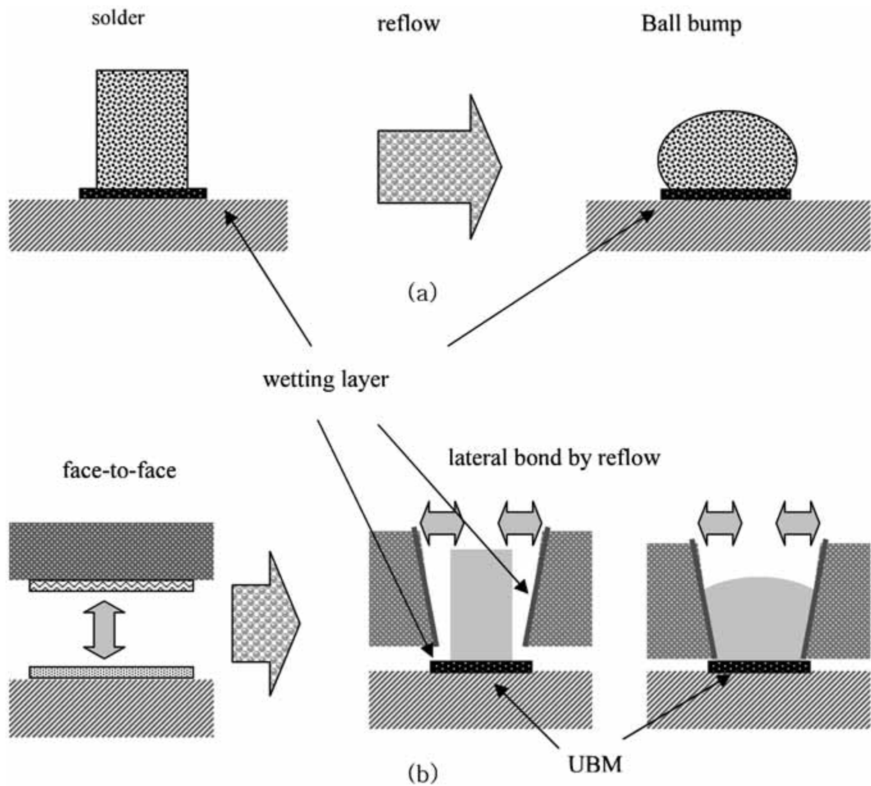
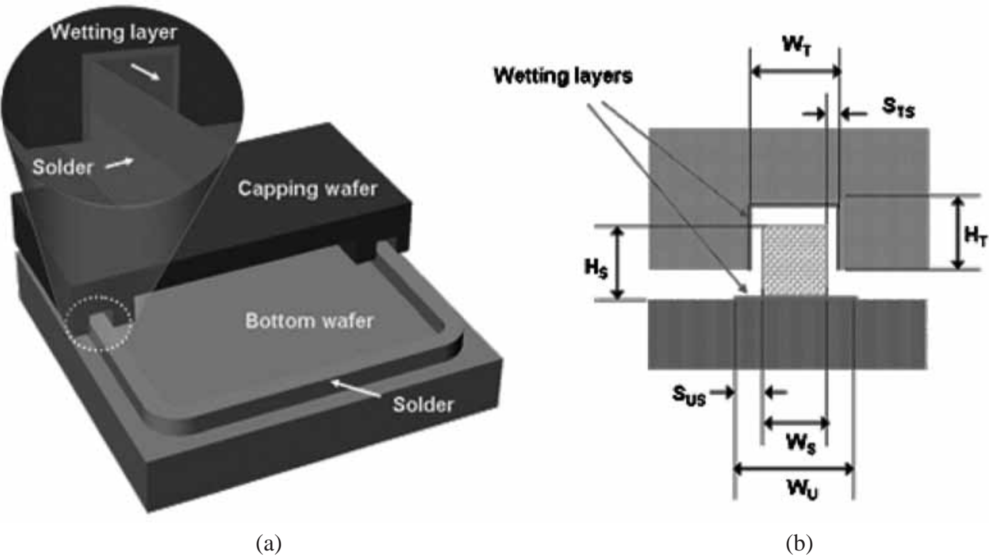


Fig. 1. Principles of the new scheme: (a) solder reflow and (b) conventional "face-to-face" bonding (left) and lateral bonding (right).

a shadowing effect on the edge (Fig. 3(d)). A Cr(400 Å)/Au(4000 Å) wetting metal was sputtered to improve the step coverage for the trenchwall (Fig. 3(e)). Finally, the lift-off process was completed for the wetting metal to cover the trench wall by the shadowing effect (Fig. 3(f)).

3.2 *Bottom wafer fabrication and bonding processes*

The bottom wafer of the proof-of-concept structure was fabricated on Pyrex glass using electroplating technology as described in Fig. 4. The process started with 300-μm-thick double-side-polished glass wafers (Pyrex 7740). Then the UBM wetting layer of Cr(400 Å)/Au(4000 Å) was first defined (Fig. 4(a)). A thin AZ 1512 photoresist was developed for the solder region (Fig. 4(b)), followed by the deposition of a thin Au(1000 Å) seed layer (Fig. 4(c)). A THB 151N negative photo-resist (manufactured by JSR Corporation) was molded for the solder. Plasma O_2 ashing was carried out for 2.5 min at a power of 100 W to remove the residue on the bottom surface (Fig. 4(d)). The pure tin (Sn) was electroplated (Fig. 4(e)). Finally, the THB 151N PR mold, Au seed layer and AZ photoresist were



(a) (b)

Fig. 2. (a) Schematic of proof-of-concept structure and (b) design parameters to be considered.

Table 2
Design parameters and design values.

	Cap. wafer		Bottom wafer			Alignment	
Fabrication design	(100) Silicon wafer Deep RIE Cr/Ar wetting Sputtering & lift-off		Cr/Au UBM JSR 151N thick PR Pure tin(Sn) plating Seed lift -off process				
Parameters	W_T	H_T	W_S	W_U	H_S	S_{TS}	S_{US}
Design values (μm)	50		44	60			
	100	<100	94	110	~80	3	8
	150		144	160			

removed one by one (Fig. 4(f)).

The fabricated wafers of both the capping and a bottom wafer fabrication processes were bonded together by lateral solder reflow. The wafer level aligned assembly was found to be similar to the way in which children assemble the blocks of the well-known toy brand “LEGO”. The wafers were aligned with special vacuum jigs and assembled in a LEGO-like formation. The assembled pairs were put in the reflow oven to be heated under N_2 gas atmosphere. There are two instances where bonding occurred: The “ Bond A” pair was achieved at 250°C for 0.5 min and the “Bond B” pair at 250°C for 3.0 min.

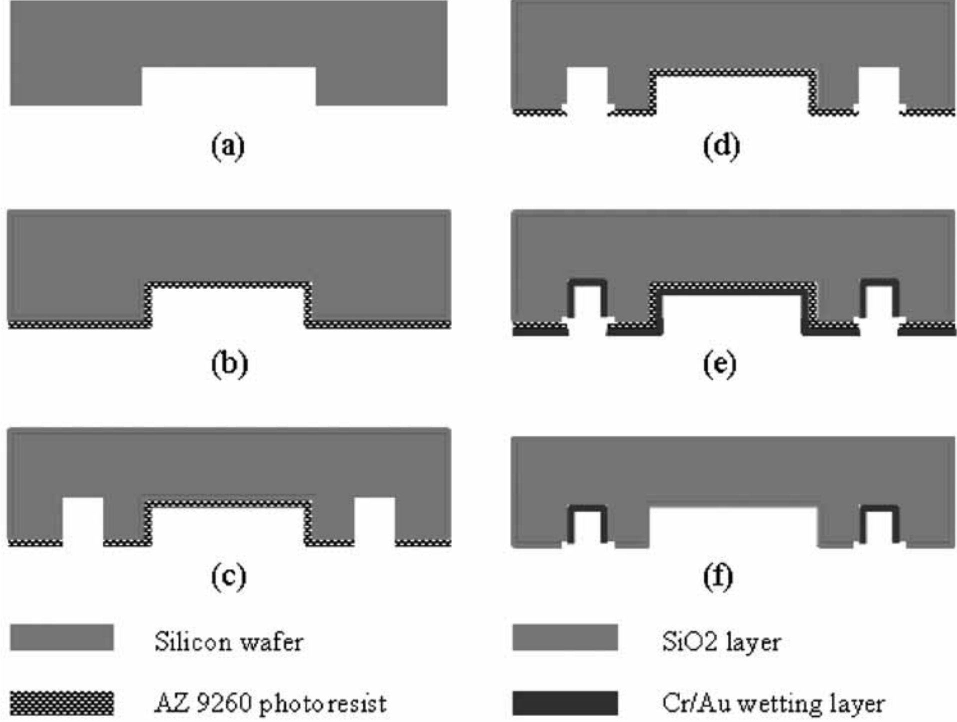


Fig. 3. Process flow of capping wafer fabrication.

3.3 *Evaluations and discussion*

3.3.1 *Strength test under shear*

The strength under shear was evaluated with a ROYCE Instruments System 552 100K bond tester. The cells were fixed on the platform and the shear force was applied parallel to the bonding interface. The bonding strength under shear was around a few tens of *MPa,* as shown in Fig. 5. The strength of the “Bond A” pair (250°C, 0.5 min) was higher than that of the “Bond B” pair (250°C, 3.0 min). It can be understood that the decrease in the strength of the “Bond B” case resulted from the degradation of adhesion by the time-dependent diffusion of seed Au metal into the solder. SEM photographs of the fracture surfaces are shown in Fig. 6. The solder was found to have flowed even into the upper wetting region of the seal trench, which proves that Au depletion occurred in the bonding interface that is assumed to decrease the bonding strength.

3.3.2 *Hermeticity test*

The pressurized He leak test is normally used to evaluate the hermeticity with a high sensitivity because He is an inert gas that only composes 0.0005% the air and also very small to be allowed to easily penetrate the wall. The pressure change per unit dwell time in the cavity is approximately given by $\Delta p(t)/\Delta t \approx R/V$, where $\Delta p(t)$ is the differential pressure between the inside and outside of the cavity, as a function of time t, V is the

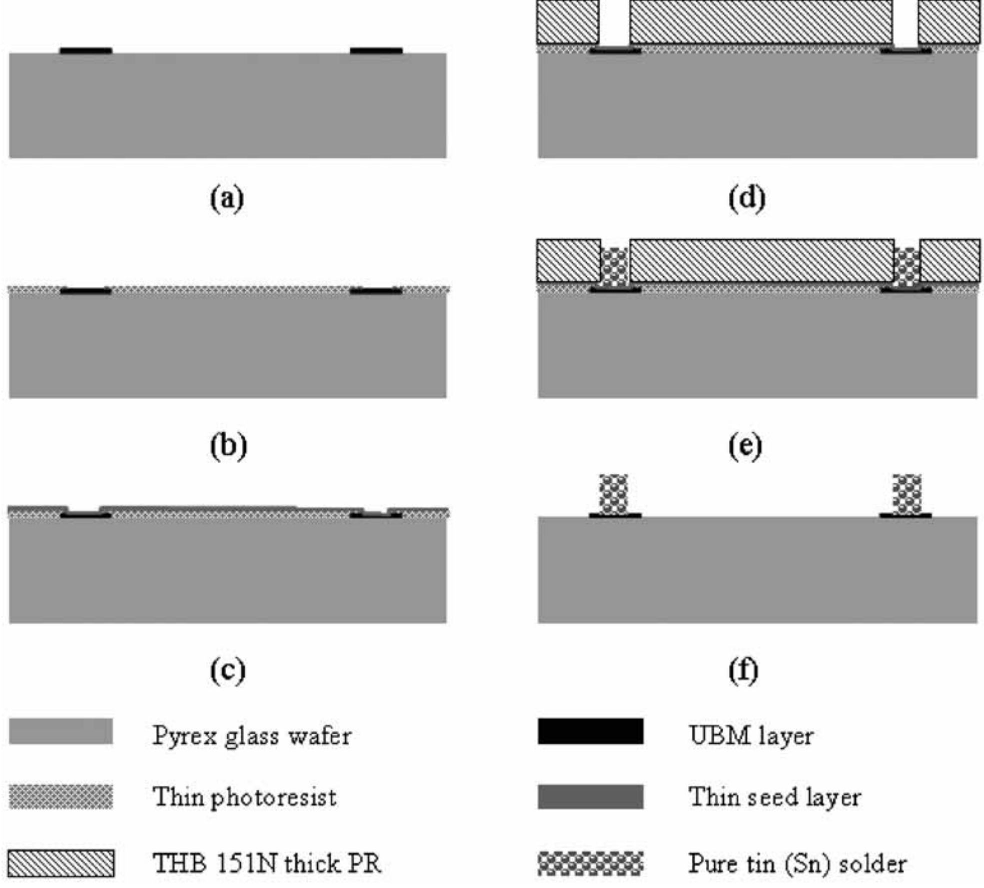


Fig. 4. Process flow of bottom wafer fabrication. The inside of the package can be investigated through a Pyrex substrate without a fracture using an optical microscope.

volume of the cavity, Δt is the dwell time, and R is the leak rate.

According to the test condition "A2" of the MIL-STD 883E standard, the criterion for hermetic failure is that the value must exceed 5.0 10^{-8} mbar-l /s of equivalent leak rate in air (L) at a volume below 0.01 cc.[13] The relationship between R and L is shown in eq. (1), where P_E is the pressure of exposure in atmosphere absolute, P_O is the atmospheric pressure in atmosphere absolute (1 atm), M_A is the molecular weight of air in gram (28.7), M is the molecular weight of He in gram (4), T_E is the time of exposure to P_E in seconds, T_{dwell} is the dwell time between the release of pressure and leak detection in seconds and V is the internal volume of the cavity in cubic centimeters.

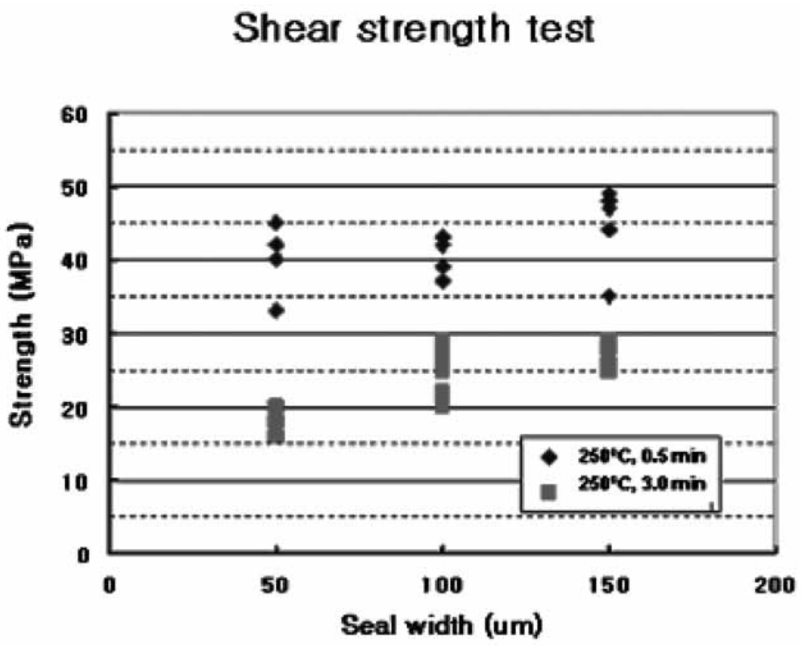


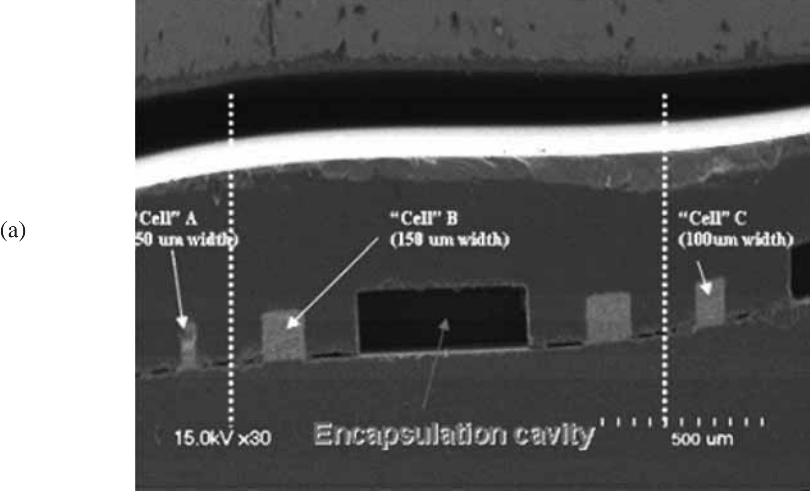
Fig. 5. Strength evaluation under shear. The force should be put in parallel with the bond surface.

$$R = \frac{LP_E}{P_O}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - \exp\left(-\frac{LT_E}{VP_O}\left(\frac{M_A}{M}\right)^{1/2}\right)\right\}\exp\left(-\frac{LT_{dwell}}{VP_O}\left(\frac{M_A}{M}\right)^{1/2}\right) \quad (1)$$

In this work, one hundred cells with no gross leak were tested at once using an ALCATEL DGC 1001 He leak detector. First, the gross leak detection was carried out before the He fine leak test by the optical observation of the inner cavity through a Pyrex substrate because, if there is a gross leak, the detection also shows a very low leak rate. The cells were dipped in IPA for tens of minutes. A dew drop in the cavity was evidence of gross leak.

The He mass spectrometer indicated a typical value of 2.0 10^{-9} mbar-l/s in He (R) independent of seal width, which is equal to 2.93 10^{-9} mbar-l /s of L calculated from eq. (1), where P_E is 6.9 atm, is 18,000 s, T_{dwell} is 300 s and V is 0.00375 cc for one hundred cells. The experimental result shows that the encapsulation using this scheme is sufficiently hermetic.

(a)



(b)

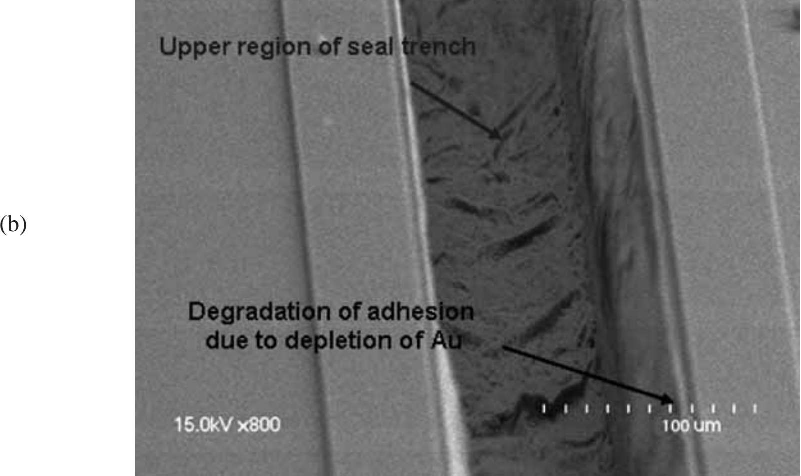


Fig. 6. SEM photographs of (a) cross-sectional view of bonded cell and (b) tilting view of fractured surface.

4. Conclusion

In this work, a wafer level lateral bonding scheme with a new apparatus is proposed. This scheme is very useful for WLP with a nonplanar surface due to the lateral bonding principle accompanied with the LEGO-like assembly. Furthermore, it can avoid the notching problem that occurs in electrical via-interconnection due to its being less sensitive

to the topology. The bonding strength under shear was a few tens of MPa and the equivalent leak rate was 2.93 10^{-9} mbar-l /s in air (L) based on the test condition "A2" of MIL-STD 883E. The experimental results proved that the new scheme is feasible and thus is a good alternative method for high-yield wafer level packaging.

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