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Fabrication of Surface Micromachined Microstructures Using SOI Structures with Buried Cavities and DRIE

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This paper describes the fabrication of Si-on-insulator (SOI) structures with buried cavities using Si-wafer direct bonding (SDB) and electrochemical etch-stop, and their application to surface micromachined microstructures by deep reactive ion etching (DRIE), which is suitable for thick membranes, cantilevers, and three-dimensional microstructures with good thickness, uniformity, flatness and single-crystal Si. After a feed-through hole for supplied voltage and buried cavitives formed on the handle of a p-type Si wafer, the handle wafer was bonded to active Si wafers consisting of a p-type substate with an n-type epilayer corresponding to membrane thickness. The bonded pair was then thinned until electrochemical etch-stop occurred at the pn junction during electrochemical etchback. By using the SDB SOI structure with buried cavities, surface micromachined microstructures were fabricated by DRIE. This single-crystal Si surface micromachining process is a powerful and versatile technology for new microelectromechanical systems (MEMS) applications.

1. Introduction

Recently, much work on microelectromechanical systems (MEMS) integrated with devices in identical substrates is actively in progress as a result of microstructures being fabricated more easily using Si micromachining technology. In genenal, Si micromachining technology is divided into bulk and surface micromachining.[1,2]

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MEMS devices fabricated by bulk micromachining are large and relatively high-cost. Being fabricated by anisotropic wet etching in KOH, EDP or TMAH solutions, structural shapes are restricted by limitations of the Si crystal face. On the other hand, because surface micromachining technology uses growing multilayers or the deposition of thin-films on Si wafers by chemical vapor depostion (CVD), the vertical dimensions of the microstructures are defined by the thickness of the deposit or the thin-film, which is currently limited to less than 10 to 20 μm. Even with careful processing, residual stresses and stress gradients in the thin-film place limitations on the lateral dimensions.

In particular, a Si-on-insulator (SOI) structure has been used as a very effective substrate in various MEMS fields in recent years. In case of surface micromaching, the fabrication of a SOI wafer with free-standing Si membranes was previously reported by Graff and Schubert.(3) This SOI structure was formed by the chemical vapor deposition (CVD) method, which produces a polysilicon active layer with a 1.5 μm thickness. However, the polysilicon membranes have some unsolved problems, such as residual stress and a weak bond strength with the Si substrates.(4)

On the other hand, the SOI wafers fabricated by Si-wafer direct bonding (SDB) technology have several advantages, such as high-aspect-ratio structures, relatively simple process steps and precise control of the geometry of microstructures. In addition, one can accurately fabrucate thick or thin Si membranes, cantilevers, and bridges which has the excellent mechanical properties of single crystal Si, such as low residual stress, great fatigue resistance and high yield strength.(5) Especially, this technolgy enable simple fabrication of thick SOI layers for Si bulk micromachining with buried cavities or surface micromachined microstructures. It is most important for thinning and for accurate thickness control of SOI active layers to use the SDB SOI technology in MEMS. The chemical mechanical polishing (CMP) process is not effective to maintain a mirror surface of the SOI layer and frequently causes damge to the SOI layer due to difficulty of griding the independent SOI layer with buried cavites. The other release technique, the epitaxial layer transfer (ELTRAN) can accurately control the SOI layer thickness, but the bonding technology with buried cavites has not yet been analyzed.(6) In this work, we used the electrochemical etch-stop method, which is based on the anodic passivation characteristics of the Si with a reverse-bias pn junction. In comparison with these existing technologies, the electrochemical etch-stop is the safest of the thickness control technologies. It can control dozens of Å of the final surface roughness and thickness within 0.2 μm.(7)

In this study, we fabricated SDB SOI structures with buried cavities and investigated the flatness of the etch-stopped surfaces and the SOI layers, applying electrochemical etch-stop as the thinning the SDB SOI substrate. In addition, we fabricated the surface micromachined microstructures for Si bulk micromachining by deep reactive ion etching (DRIE). Finally, these fabricated independent membrane structures were analyzed by atomic force microscopy (AFM) and scanning electron microscopy (SEM).

2. Experimental

In this work, we used two boron doped Si wafers which are <100> oriented 4-inches and 3.0×3.0 cm^2 with a resistivity of 12.23 Ω·cm and a thickness of 505 μm. The handle

wafer was p-type, and the active wafer consisted of a 15-μm-thick n-type epilayer grown on a p-type substrate. The oxide layer was thermally grown to be 5000 Å.

The fabrication process sequences of surface micromachined microstructures using SDB SOI structures with buried cavities and DRIE are shown in Fig. 1. The Si substrates used in the process were passed through a standard semiconductor cleaning process to remove organic/inorganic particles on the Si surfaces. We carried out anisotropic etching on the back surface of the p-type handle wafer to define an array of vias to serve as contact holes for the electrochemical etch-stop before SDB processing. A completely etched sample and an n-epi wafer were processed for pre-bonding after pre-treatment in the dilute HF (2.0%) for 1 min using a point-of-contact method, which forms a strong bond between the two samples from the cavity towards the side creating a 1×10^{-6} mTorr vacuum condition after pre-treatment.[8] The bonded Si wafer with buried cavities has an SOI layer with thickness controlled by electrochemical etch-stop after annealing to 1000°C for 60 min.[9,10] Completely bonded samples with buried cavities are used in the fabrication of SDB SOI structures by bulk micromachining.

Figure 2 shows a configuration for the electrochemical etch-stop for the fabrication of SDB SOI structures with buried cavities. A temperature bath at 80°C of 20 wt.% TMAH

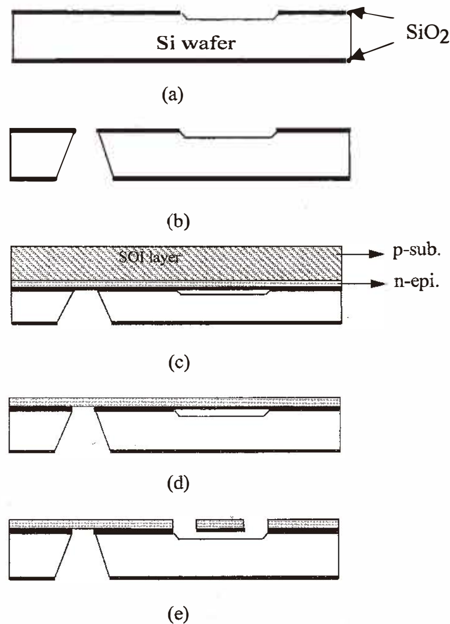
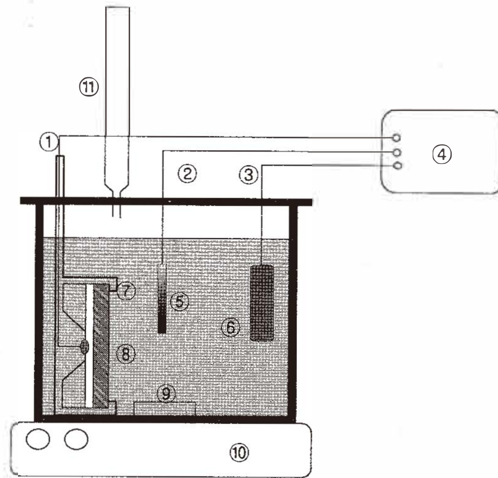


Fig. 1. Fabrication process sequences for surface micromachined microstructures using SDB SOI structures with buried cavities and DRIE: (a) fabrication of buried cavity, (b) formation of feed-through hole, (c) SDB process, (d) fabrication of SDB SOI, and (e) implementation of surface micromachined structures.



1. Working Electrode
2. Reference Electrode
3. Counter Electrode
4. Potentiostat
5. Ag/AgCl
6. Pt mesh
7. Teflon holder
8. Sample
9. Magnetic stir-bar
10. Hot plate
11. Reflux condenser

Fig. 2. Configuration for electrochemical etch-stop.

solution was chosen for all the experiments, and was controlled during the process to within ± 1°C. During wafer etching, a constant voltage was supplied between a working electrode and a reference electrode using a scanning potentiostat. A magnetic stirrer was used to maintain a uniform concentration of the 20 wt.% TMAH solution throughout the beaker. In this manner, an SDB SOI structure with a single-crystal Si active layer and buried cavities was completely fabricated.

Finally, to fabricate the surface micromachined microstructures, a thick photoresist layer was used as a mask and, after patterning for DRIE through the top Si wafer into the buried cavity, the microstructures were formed using an SF_6:O_2 gas mixture as shown in Table. 1.

3. Results and Discussion

To prevent premature etch-stop during the Si membrane fabrication process, we compared the curves for leakage current-voltage characteristics between the p-type and n-epi layer grown p-type Si wafers. Figure 3 shows the leakage current-voltage characteristic

Table 1
DRIE conditions for 3D microstructure fabrication.

Condition \ Level	Deposit	Etch 1	Etch 2
C_4F_8 (cc)	100	0	0
SF_6 (cc)	0	70	100
Ar (cc)	40	40	40
Time	6 s	3 s	5 s
RF power	1 W	9 W	9W
ICP power		825 W	
Vaccum		20 mmTorr	

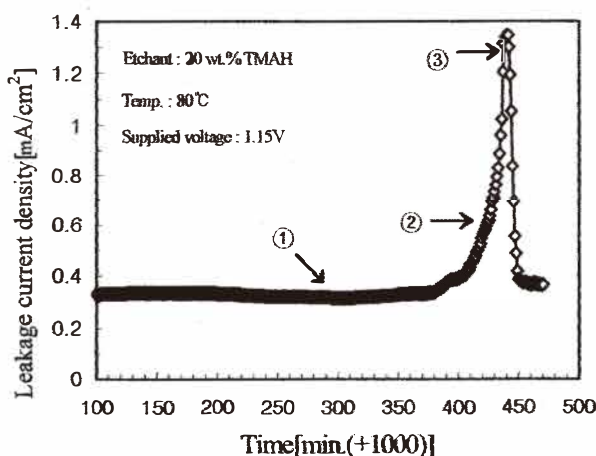
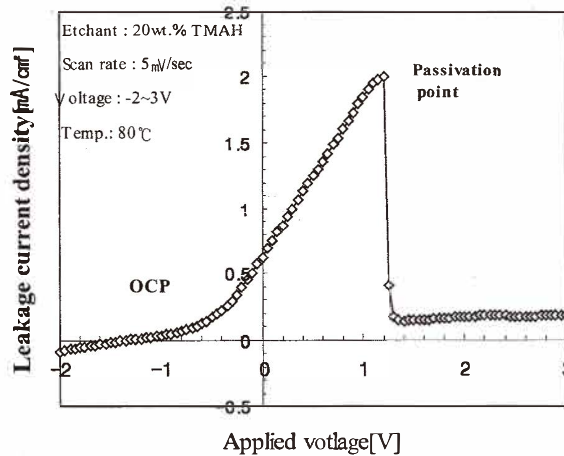


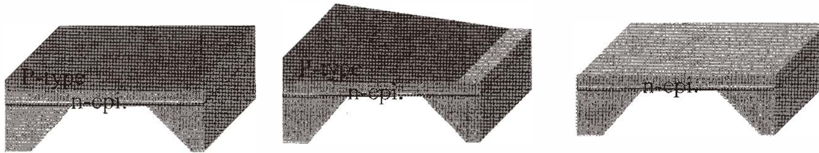
Fig. 3. Leakage current-voltage characteristic curve of p-type Si wafer.

curve of a p-type wafer in a 20 wt.% TMAH solution at 80°C. The concentration of boron used as a dopant in the p-type substrate was $10^{14} \sim 10^{15}$ cm^{-3}, the scan rate was 5 mV/s, and the supplied voltage was –2 V ~ 2 V. Because the open curcuit potential (OCP) point was –1.4 V, the leakage current was constantly increased until the passivation point (PP) was attained. At a passivation point of 1.2 V, the leakage current which has been increased incrementally was suddenly decreased on the Si wafer. The highest current density measured was about 1.35 mA/cm^2, and the leakage current density remained between 0.035 mA/cm^2 and 0.046 mA/cm^2 after the etch-stop.

The leakage current-time characteristic curve at the point of electrochemical etch-stop is shown in Fig. 4(a). Using the reference electrode (Ag/AgCl) in a three-electrode system, the leakage current was maintained steadily during the Si etching time. After the p-type Si had been etched, the leakage current was suddenly increased when n-epi Si appeared in the



(a)



(b)

Fig. 4. (a) Leakage current-time characteristic curve and (b) etch-stop step at electro-chemical etch-stop.

etching solutions. When the n-epi Si had been exposed completely, the etching was stopped by passivation of the chemical reaction with etched solutions. Figure 4(b) shows the etch-steps: (1) is the situation in which the p-type Si appeared by restoration of an oxidizing environment in the etched solutions. (2) shows that the surface of p-type Si surface was partly removed in the TMAH solutions, at which point the leakage current of the pn junction was rapidly increased up to 2 mA/cm^2 at a voltage of 1.2 V. (3) indicates that the p-type Si has been completely etched and the etching has been stopped by passivation in the n-epi Si layer.

Figures 5(a) and 5(b) show AFM images of an n-epi layer grown p-sub (100) mirror surface and SDB SOI substrates with buried cavities etch-stopped electrochemically in a 20 wt.% TMAH solution. The average roughnesses of the n epi layer and the etch-stopped SOI layer is 5.12 nm and 5.4 nm, respectively. In the case of SDB SOI structures fabricated by electrochemical etch-stop, the flatness of the etch-stopped SOI substates is much better than those in the case of other methods such as lapping and chemical mechanical polishing (CMP), and corresponds to that of Si mirror surfaces.[11]

The SEM cross-sectional views of the SDB SOI structure with buried cavities are

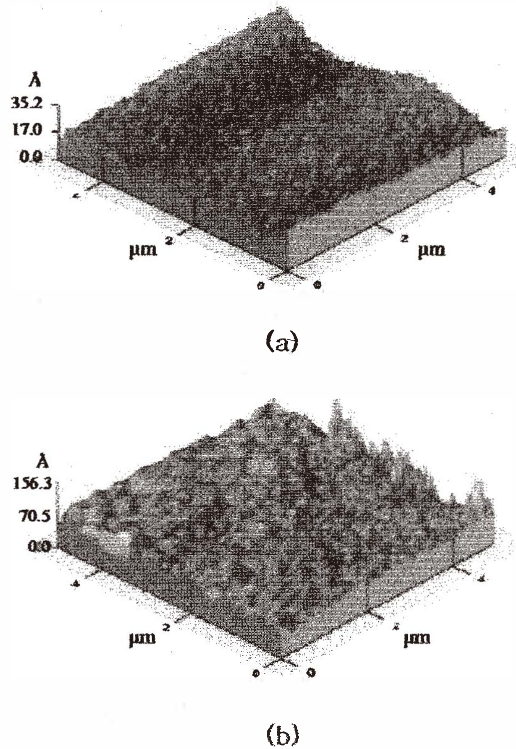
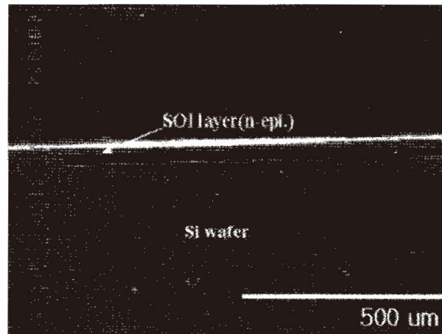


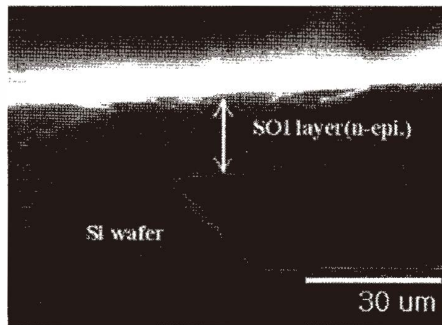
Fig. 5. AFM images of (a) Si polished surface and (b) SDB SOI substrates with buried cavities etch-stopped electrochemically in TMAH (20 wt.%) solution.

shown in Figs. 6(a) and 6(b). This experiment successfully achieved SDB SOI structures and electrochemical etch-stop processes using the Si wafer (p-type) and the p-sub./n-epi.(15 μm) wafer. The thickness of the active layer over the etch-stopped cavity is 15 μm, the depth and the width are 18,900 μm, respectively. A membrane with a dimension of 900×900 μm^2 over the buried cavity is maintained in an independent state without any damage to the active layer. Thus, it is confirmed that 3D microstructures with a high aspect ratio can be achieved using SDB SOI fabrication techniques and electrochemical etch-stop, and that the properties of these are appropriate for MEMS applications.

Figure 7 shows an surface microphotograph of the micromachined structures on single-crystal Si showing the SDB SOI structures with buried cavities and DRIE. A diaphragm with a demension of 300×300 μm^2 onto a buried cavity is maintained independently without any damage to the active layer. Because of the high aspect ratio possible with these processes, the micromachined structures on the surfaces can be very tall, yet narrow and compliant for MEMS applications.



(a)



(b)

Fig. 6. (a) X100 and (b) X1000 SEM images of the SOI structures with buried cavities fabricated SDB and electrochemical etch-stop.

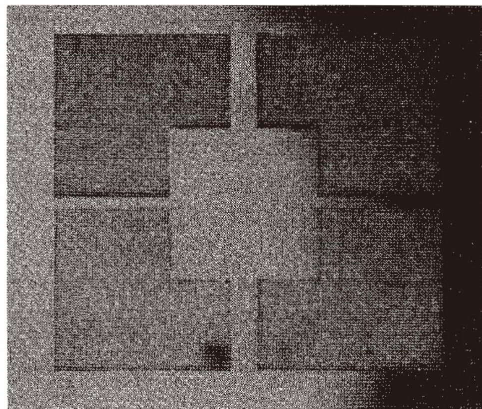


Fig. 7. A surface microphotograph of the micromachined structures on single-crystal Si implemented through the SDB SOI structure with buried cavities and DRIE.

4. Conclusions

Applying electrochemical etch-stop to the methods for thinning of SDB SOI substrates, we have fabricated SOI structures with buried cavities and have investigated the flatness of the etch-stopped surface and the variations in SOI thickness. The surface micromachined structures have been achieved by DRIE. After forming buried cavities, the SDB SOI structure with buried cavities has been fabricated using electrochemical etch-stop. Finally, after fabricating the SDB SOI substrate with buried cavities, the micromachined strutures on the surface achieved using DRIE have been shown to have very good electrical and mechanical qualities. The combination of these two powerful micromaching techniques forms a versatile new technology for the fabrication of MEMS devies.

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