

Integration of LIGA Structures with CMOS Circuitry

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Successful direct integration of a mechanical structure fabricated by LIGA on a Si chip containing CMOS circuitry has been achieved in this work. A one-dimensional cantilever accelerometer is chosen as a vehicle to demonstrate this integration process. The capacitive sensor element employs one electrode formed in the Si substrate during integrated circuit (IC) fabrication. The other electrode is fabricated using the LIGA technique along with sacrificial layer etching. Details of a post-IC fabrication process to achieve this integration are given. Need for careful control of stress in the deposited layers on both the chip and the X-ray mask is delineated. Achieving a high contrast in the X-ray mask is necessary. The process developed here can also be utilized for integrating high-aspect-ratio structures obtained with a thick UV resist such as SU-8 with circuitry on the same chip.

1. Introduction

Significant research progress has been made in recent years in developing microsensors and microactuators for a variety of applications for defense, commercial, medical, environmental, analytical and other purposes.^(1–6) Microdevices comprising microsensors and microactuators need to be integrated with measurement and control circuitry to increase the applicability of these devices. Frequently, the measured signal or signal-to-noise ratio can be small and thus requires amplification at the point of detection. On occasions, the signal must be processed at the point of detection in order to extract useful data. An example would be an array of neural probes that would require data amplification and multiplexing

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at the detection point prior to sending the signal outside.⁽⁷⁾ This calls for the integration of circuits with detectors. Remote sensing and monitoring in many applications including biomedical applications require the integration of sensors and actuators with circuitry. There are two approaches to integration. In the monolithic approach, microstructures and circuits are present on the same chip. In the hybrid approach, circuits and microdevices are built on separate substrates and then assembled together on a common carrier such as a ceramic substrate. In some cases, system integration may involve both monolithic and hybrid approaches. The nature of the system application along with its cost and performance criteria dictate the preferred approach to integration. Hybrid integration permits the fabrication of sensors and circuits separately and hence allows for the optimization of individual fabrication processes. This is desirable and has been utilized extensively.⁽⁸⁾ On the other hand, monolithic integration is conducive to wafer-level batch processing, making it as easy to integrate one micropart as one hundred or more microparts. Moreover, it allows for a more compact system and provides improved reliability and performance, particularly when the measured signals are small or need immediate amplification or processing.

There are three ways to achieve the monolithic integration of integrated circuit (IC) technology with microdevices or MEM structures to fabricate intelligent microsystems. In the pre-IC fabrication approach, microdevices are fabricated first on a chip followed by IC fabrication. This approach exposes the fabricated microdevices to high processing temperatures and the harsh chemical and radiation ambient inherent in an IC fabrication process. This may not be desirable in many applications. However, it has been employed in some cases.⁽⁹⁾ The second approach is to integrate microdevice fabrication steps with IC fabrication steps as far as possible. This is referred to as the co-IC fabrication approach. This approach has the advantage of economy as the total number of steps is reduced, but it inevitably calls for performance compromises, as the processing steps that optimize the microdevice performance do not necessarily optimize circuit performance. This approach is also impractical, as each new microstructure design may call for a different processing sequence that can be time-consuming and costly to implement. We had adopted this approach in our earlier work with limited success.⁽¹⁰⁾ The third approach is to fabricate the circuit first and then fabricate the microstructures. This is the post-IC fabrication approach. The fabrication steps for microstructures must now be restricted to a low temperature (typically below 450°C) so as not to degrade the performance of aluminum metal layers on the CMOS chip. The microdevice fabrication process must also present a benign chemical and radiation ambient to the fabricated circuits so that the performance of the latter is not degraded. In spite of these limitations, post-IC fabrication is an approach of choice for the integration of many microsystems. One can also combine these approaches, for example, utilizing some common fabrication steps used in co-IC fabrication with post-IC fabrication.⁽¹¹⁾

There are three broad approaches utilized in fabricating microstructures on a chip.⁽¹²⁾ These are bulk micromachining, surface micromachining and LIGA⁽¹³⁾ processing. Baltes *et al.*⁽¹⁴⁾ and Baltes and Brand⁽¹⁵⁾ have summarized the approaches to integrating IC technology with microdevices utilizing bulk and surface micromachining technologies. Integration of CMOS circuitry with electroformed metal structures using UV exposure has been reported.⁽¹⁶⁻¹⁸⁾ In this paper, we present a fabrication technique for integrating LIGA

or LIGA-like structures with standard CMOS circuitry. The LIGA process employing X-ray exposure permits the formation of high-aspect ratio structures with near vertical sidewalls.⁽¹⁹⁾ Fabrication of 1000 μm or higher structure with vertical sidewalls is possible. This is in contrast to the surface micromachining technique where a typical polysilicon layer is less than 15 μm in height. In many applications, a high aspect ratio results in improved performance and/or sensitivity. For example, in a comb-drive structure the electrostatic force increases linearly with structure height.⁽²⁰⁾

There are two approaches to monolithically integrating LIGA structures with circuitry. In the case of aligned molding by Both,⁽²¹⁾ the LIGA structure is obtained by a post-IC fabrication process below 200°C utilizing press molding of polymethylmethacrylate (PMMA). The aligned molding technique requires specialized equipment for alignment and pressing. The force on the molding tool must be controlled to prevent damage to the silicon wafer. The above mechanical printing process suffers from lateral dimension changes as the molding tool presses into PMMA and essentially pushes it away. Dimensional changes also arise from the differences in the thermal coefficient of expansions of the various materials involved. Some of these dimensional changes can be compensated for during design. Typically an alignment accuracy of $\pm 8 \mu\text{m}$ is achieved.

In the approach presented here, LIGA or LIGA-like structures are monolithically integrated with CMOS circuitry through a post-IC fabrication process utilizing direct optical printing rather than mechanical printing. The approach uses X-ray exposure of a thick resist such as PMMA and can also be applied for the integration of high aspect ratio structures fabricated by optical UV or X-ray exposure of a thick resist such as SU-8. CMOS technology is chosen for fabricating circuitry, as it is the most common IC technology in use today.

2. Method

A one-dimensional cantilever accelerometer is chosen as a test vehicle to demonstrate the integration process developed here. The accelerometer is a capacitive sensor formed between a suspended electrode and a fixed electrode. Acceleration is indicated by a change in capacitance value due to motion of the suspended electrode. The detailed design of the movable electrode and the required sensing circuitry has been carried out.⁽²²⁾ The circuit is then fabricated by a commercial IC foundry utilizing 2- μm -linewidth n-well CMOS technology. The fabricated chip with CMOS circuitry is shown in Fig. 1. The circuits include a readout circuit for capacitance measurement, a sample-and-hold circuit and two amplifiers. Details of the readout circuit design are given elsewhere.^(10,23) The large central open area in Fig. 1 is for fabrication of a movable mechanical LIGA part by a post-IC fabrication process developed in our laboratory, to achieve direct integration of LIGA-like structures with CMOS technology.

A simplified overview of the post-IC fabrication sequence developed here is depicted in Fig. 2. After receiving the chip containing the CMOS circuitry from the foundry, the overglass and all other dielectric and metal layers nominally present after CMOS circuit fabrication are first removed from the open area shown in Fig. 1. The resultant cross-sectional view is shown in Fig. 2a). In this design, we have utilized the p⁺-layer available in CMOS technology to make a connection with the sensing mechanical part. We have also

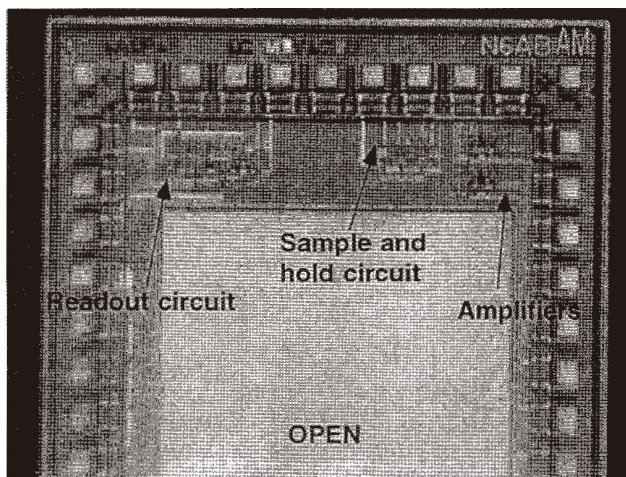


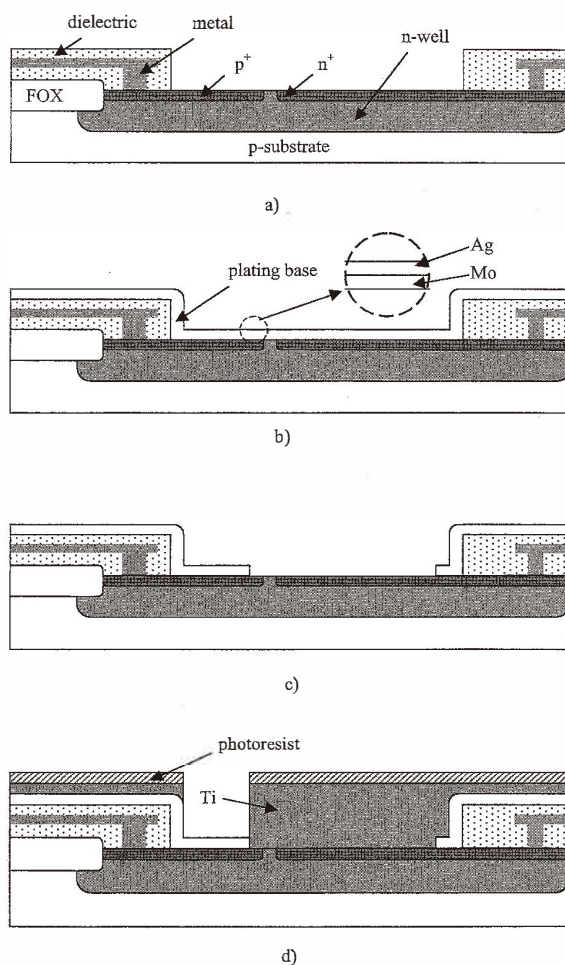
Fig. 1. IC chip after CMOS circuit fabrication.

utilized the n^+ -layer available in the CMOS fabrication process to form a part of the mechanical sensor. The n^+ -layer forms the fixed bottom plate of the capacitor used for sensing acceleration. These are examples of co-IC fabrication steps that are incorporated in our sensor design. The other plate of the capacitor will be a movable LIGA beam structure to be fabricated by a post-IC LIGA technique.

In order to achieve a successful merging of LIGA and CMOS IC technologies, the fabrication sequence is broken down into smaller steps. Problems in the individual steps are solved until an acceptable solution is obtained. Finally, these steps are combined to obtain an integrated monolithic structure.

2.1 *Plating base*

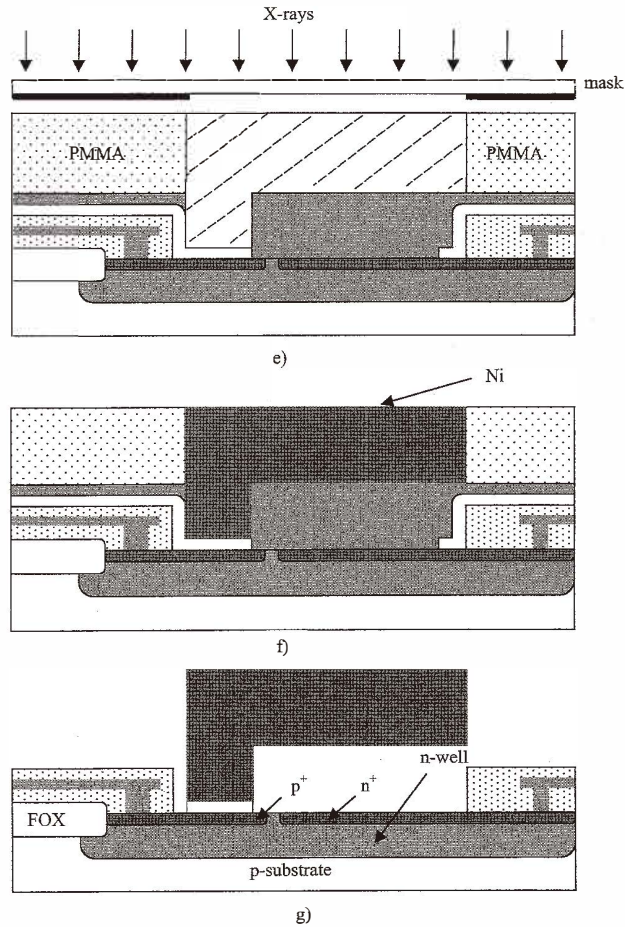
A plating base is needed for providing an electrical contact during electrodeposition. The plating base should also adhere well to the silicon substrate. In this work, a sandwich layer consisting of 20-nm-thick Mo followed by 60-nm-thick Ag is employed as the plating base. Molybdenum provides adhesion to the substrate while Ag serves as the plating base layer. Both metals must also protect the underlying areas from attack by the 10% HF solution used for sacrificial layer etching for releasing the LIGA structure as described later. Both metals are deposited by rf sputtering. Control of stress during film deposition is crucial in providing protection of the underlying areas from attack by the sacrificial layer etchant and for reducing defects in the electrodeposited material. Hence, the film deposition process is first characterized. The conditions for stress-free deposition of Mo are given elsewhere.⁽²⁴⁾ From the d-spacing values obtained from X-ray diffraction measurements as a function of sputtering pressure, Mo films deposited at a rf sputter power of 400 W, argon flow rate of 45 sccm and pressure of 8 mtorr were found to be under the least strain.⁽¹¹⁾ The same pressure was used for the Ag deposition as well since the sputtered Ag films at this



Figs. 2a)–2d). Process sequence for monolithic integration of LIGA with CMOS IC by a post-IC fabrication technique. Figures depict cross section in the area labeled OPEN in Fig. 1. a) After removal of dielectric and other layers from the OPEN area. b) After plating base deposition. c) After patterning of the plating base. d) After sputter deposition and patterning of Ti sacrificial layer.

pressure were found to be of good quality. No separate strain measurements were carried out for the Ag layer deposition.

The cross section after plating base deposition is shown in Fig. 2b). The plating base layer is now patterned using a standard lithographic technique. The Mo/Ag plating base layers are retained wherever the underlying substrate needs to be protected during the sacrificial layer etch. Figure 2c) shows the cross section after patterning of the plating base layers.



Figs. 2e)–2g). Process sequence for monolithic integration of LIGA with CMOS IC by a post-IC fabrication technique. Figures depict cross section in the area labeled OPEN in Fig. 1. e) X-ray exposure after spin-coating PMMA. f) After electroplating of Ni. g) After PMMA removal, sacrificial and protective layer etching.

2.2 Sacrificial layer

Titanium is used as a sacrificial layer in this work. As stated previously, it is extremely important to obtain a stress-free deposition. X-ray diffraction data indicated 8 mtorr rf sputtering pressure at 200 W sputter power and an argon flow rate of 45 sccm to be optimal for this purpose, giving Ti films with very small built-in strain.⁽¹¹⁾ A sacrificial layer thickness of 3 μm or smaller is used in this work. Figure 2d) shows the cross section after selective patterning of the sacrificial Ti layer to provide access to the electroplating base.

2.3 X-ray lithography

2.3.1 Resist coating

Application of a thick resist poses new challenges. Photoresist layers used in the IC industry are thin, being typically less than 5 μm in thickness. High-aspect-ratio structures possible with LIGA require a thick photoresist coating. For X-ray lithography, PMMA is frequently used as a positive resist material. One approach to applying thick PMMA layers on a substrate is by a casting process using a press.⁽²⁵⁾ This approach is always accompanied by high stress in the resist and at the resist/substrate interface. Another approach is through bonding of a PMMA sheet to a Si substrate.⁽²⁶⁾ A third approach is spin-coating.⁽²⁷⁾ Spin-coating PMMA in multiple layers is used in this work to apply the resist to the substrate. In order to produce a resist thickness of 15 μm and higher, a PMMA solution with high viscosity is prepared by mixing PMMA powder with chlorobenzene (25% PMMA with 75% chlorobenzene by weight). This is the highest concentration of PMMA dissolvable in chlorobenzene.⁽²⁷⁾ A commercial spinner is used for spin-coating with a spin cycle of 500 RPM for 20 s initially, which is increased to 1000 RPM for 5 s and decreased again to 500 RPM for 125 s. A resist thickness of approximately 15 μm is obtained with this coating cycle. For multiple coatings, no baking of the previous layers is found to be necessary before applying the next layer. The same thickness is obtained for each subsequent coating during a multiple layer coating cycle. After application of multiple coatings and upon obtaining the desired resist height, the resist is baked in a nitrogen atmosphere at 110°C for 2 h. The cooling cycle sequence is critical in this baking procedure. During the cooling cycle, the oven was turned off after 2 h of baking and left to cool with an approximate cooling rate of 0.5°C/min. Figure 2e) shows the cross section after PMMA thick resist coating.

2.3.2 X-ray mask fabrication

For exposure to X-rays, a novel inexpensive X-ray mask technology has been developed in our laboratory for the fabrication of LIGA microdevices.⁽²⁸⁾ A simple mask employing a microscope cover glass as a substrate is fabricated in our laboratory to delineate transparent and absorbing areas. The initial cover glass thickness of 175 μm is first thinned to approximately 25 μm in a buffered HF solution. The etch time is about 3 h. This acts as a transparent membrane on which a Au absorber layer is deposited. Control of stress in the mask membrane is crucial. The glass membrane is mounted on a circular silicon ring formed from a silicon wafer by bulk micromachining the center portion. Silicone rubber glue is evenly spread on the top of the silicon ring and the glass membrane is placed on the ring. The glue retains elasticity upon curing, reducing stress in the membrane arising due to thermal coefficient mismatch during X-ray exposures.

A plating base comprising 10-nm-thick Cr is first sputtered on the glass membrane followed by a 40-nm-thick Ag layer. The Cr layer provides adhesion to the substrate while the Ag layer provides the seed layer for Au electrodeposition. A 5- μm -thick spin-coated photoresist (Shiply STR 1045) is used to delineate the absorber pattern through optical lithography. After developing, the resist is baked at 120°C for 90 min to make the resist sufficiently durable to withstand the electroplating solution, which has a high pH value and

otherwise has a tendency to attack the positive photoresist. A noncyanide Au complex in electrolyte with a pH value of 10–11 (Technic TG 25) is used as an electroplating solution. The Au plating is carried out in a constant temperature magnetically stirred bath at 35°C at a constant current with 1" electrode spacing and a platinized Ti mesh as the counter electrode. With this technique, stress can be controlled in the Au membrane for thicknesses up to 3 μm . Stress is critical as it can distort the pattern or can cause catastrophic failure under X-ray exposure, due to additional thermally induced stress. After 3 μm Au deposition, the resist is stripped and the Ag layer underneath the resist is etched in a ferric nitrate solution.⁽²⁹⁾ The 10 nm Cr layer is not etched as it has high optical and X-ray transparency. The completed mask is used for delineating LIGA structures on the Si wafer.

2.3.3 X-ray exposure

The exposures were carried out at the Center for Advanced Microstructure and Devices (CAMD) synchrotron electron storage ring. Exposure calculations are performed with the CXrL toolset.⁽³⁰⁾ Details of the contrast requirement and for obtaining a thicker absorber layer by utilizing a thick optical resist SU-8 are given elsewhere.^(28,31) Nominal conditions for synchrotron radiation exposure are: 1.3 GeV electron beam energy, 100 mA beam current, 25 μm glass membrane thickness, 125 μm Be window thickness and 20 torr He ambient. The exposure dose at the bottom is set to 2000 J/cm^3 to ensure complete exposure at the resist since the sensitivity of the PMMA resist used was 1600 J/cm^3 . Using the mask described in section 2.3.2, exposure on the resist under the Au absorber results in a dose of less than 200 J/cm^3 .

Excellent straight-line features are obtained in the 300- μm -thick test PMMA resist on a Si wafer using the X-ray mask technology described above. For this test case, the exposure dose is 9700 mAmin with 1" beam scan. A 17- μm -thick glass mask membrane is used, resulting in a top to bottom resist dose ratio of 4.2 under the transparent area of the glass membrane. Following the X-ray exposure, the resist is developed in a standard GG (Ghia & Glashauser) LIGA developer consisting of 60% (2-butoxyethoxy) ethanol, 20% morpholine, 5% 2-aminoethanol and 15% water (by volume) at 35°C. A post-rinse in 80% (2-butoxyethoxy) ethanol and 20% water is required to terminate the developing process and a final rinse in DI water is followed by drying in a nitrogen jet.

Unlike optical masks, X-ray masks often lack suitable contrast as no absorber is perfectly opaque and no membrane is perfectly transparent to X-rays. As a consequence, the protected area under the mask absorber layer will suffer some radiation during the X-ray exposure. In order to determine the effect of this residual exposure on the fabricated CMOS circuitry, the circuits on the chip are subjected to X-ray radiation in a controlled setup. The circuit output is proportional to the capacitance change due to acceleration. The fabricated circuits were tested prior to exposure and were found to function satisfactorily.⁽³²⁾ For this test, the measurement is performed with an initial capacitance value of 133 pF with incremental steps of 5 pF. Figure 3 shows the results. The chip is exposed to a dose such that 50 μm PMMA on the substrate would have received 2000 J/cm^3 at the bottom of the resist after passing through a 25- μm -thick glass membrane. The circuits received the same level of radiation but after passing through 3.5 μm of electrodeposited Au absorber.

After receiving this X-ray radiation dose, the circuits completely failed to work. In CMOS circuits, preventing radiation damage under the gate area is crucial. The electron-

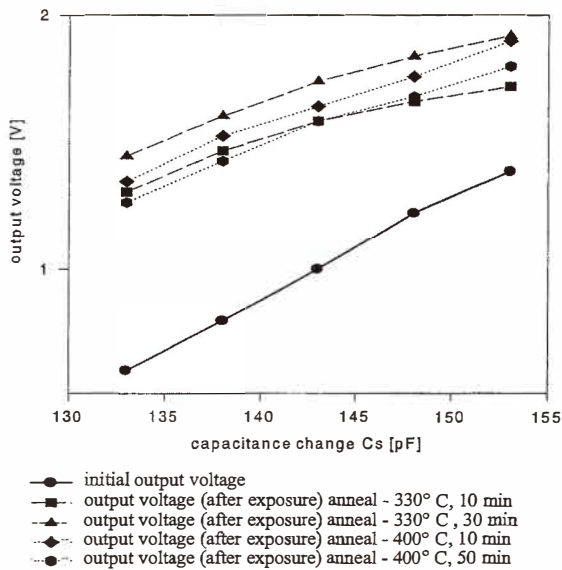


Fig. 3. Effect of X-ray exposure and subsequent annealing on the CMOS circuit performance.

hole pairs generated in the oxide due to radiation result in trapped charges in the oxide that shift the device threshold voltage. Generally, the electrons with higher mobility values are swept faster than the holes, which become trapped in the oxide bulk. Ionizing radiation also causes the creation of hole traps in the oxide by breaking the strained bonds typically found near the interface with silicon and also in the oxide bulk. The increased trap charges are observed to disappear at room temperature over periods ranging from 10^{-3} s to over 10^7 s.⁽³³⁾ Annealing the device speeds up this recovery process. Since the circuit uses an aluminum metal layer, the annealing temperature in this work must be restricted to a temperature of 450°C or lower. Figure 3 shows the results after a 330°C 10 min annealing of the exposed circuits. All annealings were carried out in N_2 ambient. The circuit recovered sufficiently to be functional but with a shift in the circuit response. A further 20 min annealing at this temperature seemed to shift the output response curve even further. Additional annealing at this temperature did not seem to affect the response further. The chip was then subjected to a 400°C annealing for 10 min. The higher temperature was expected to clear traps having higher activation energies. There was a slight improvement with this annealing as the output response curves recovered slightly as seen from Fig. 3. A further annealing for 40 min at 400°C provided very little additional improvement. Increasing the annealing temperature would be advisable, but was not carried out because of the aluminum interconnects present on the chip. Annealing temperatures in the $300\text{--}350^{\circ}\text{C}$ range provide significant but not complete recovery of the electrical output for this exposure test.

The $3.5\text{-}\mu\text{m}$ -thick Au absorber thickness used here does not provide sufficient exposure contrast. We have developed technology for fabricating a thicker Au absorber mask with

a higher exposure contrast.⁽³¹⁾ A higher contrast mask with a thicker Au layer along with post-exposure annealing is recommended for a more complete recovery from X-ray exposure damage.

2.4 Ni electroplating

Upon X-ray exposure and the development of the exposed PMMA, the resist structures are filled with metal through an electroforming process. Nickel is commonly used for LIGA microstructures because of its good plating characteristics and well-known properties and is the metal of choice in this work. The integration sequence developed here is general in nature and can be suitably tailored if a material other than nickel is utilized for the electroforming process. The electroplating technique for microstructure formation with Ni has been reported in detail in the literature.⁽³⁴⁾ The properties of electroformed Ni depend upon the temperature, pH value and current density used in the plating process. Low stress in the electroformed Ni is essential for the functionality of the movable structures, otherwise the freestanding part can buckle after its release from the substrate. The effect of the 10% HF solution used for the sacrificial layer etching on the electroplated Ni is not reported in the literature, but our experiments indicate that immersion of Ni in dilute HF degrades its adhesion to the plating base. Hence, a carefully optimized plating process that can withstand this harsh processing environment is imperative.

As stated earlier, a 20-nm-thick Mo layer was first sputtered on the silicon substrate for adhesion followed by a 60-nm-thick Ag layer as the plating base. A nickel sulfate electrolyte consisting of 200 g NiSO₄·6H₂O, 5 g NiCl₂·6H₂O, 25 g H₃BO₃, 3 g saccharine and 1 g lauryl sulfate dissolved in 1000 cc of water is used as the plating bath. The plating solution is kept at a constant temperature in a water bath. A nickel electrode, 2"×3" in size, is used as the anode and is kept at a distance of 1" from the substrate. The plating is achieved by connecting the plating base to the cathode and passing current through the electrolyte. A magnetic stirrer is used to continuously mix the solution. The plating rate can be estimated analytically.⁽³⁴⁾

Harsch⁽³⁴⁾ has reported that the minimum stress in Ni microstructures in a nickel sulfamate electrolyte occurs in the pH range of 3.5 – 4.5, the bath temperature of 50°C and the current density of 20 mA/cm². Hence, plating experiments in this work are performed at 50°C, pH of 3.5 and current density in the range of 5 – 20 mA/cm². Figure 4 shows plating rates as a function of current density. The plating rate is higher for smaller feature plating areas, perhaps due to peripheral effects. Figure 5 shows as-deposited Ni lattice spacing from the observed (111) diffraction peaks obtained from X-ray diffraction measurements as a function of the plating current density. The dotted line indicates the lattice spacing value expected from a stress-free layer. We selected 14 mA/cm² as the current density for Ni electro-deposition as it indicates a minimum amount of stress in the as-deposited layer. At smaller current densities, the lattice spacing is smaller, while for higher current densities it is higher, in either case implying increased stress.

Figure 2f) shows the cross section after Ni electroplating. For some samples, a second layer of PMMA is spin-coated directly on the first layer and the same process is repeated to yield an electroplated seismic mass at the end of the beam to increase the sensitivity of the sensor. The unexposed PMMA mold is then dissolved in acetone.

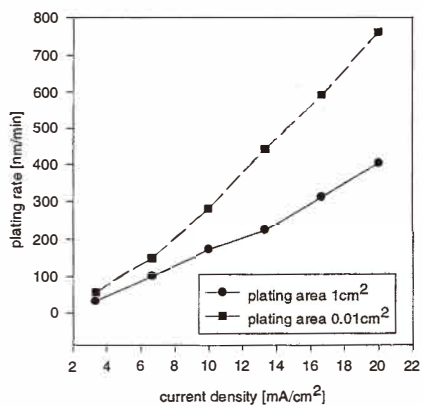


Fig. 4. Nickel plating rate as a function of current density.

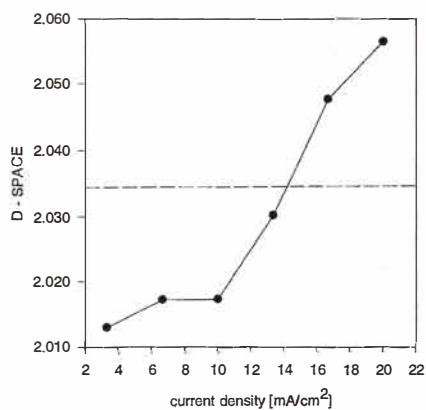


Fig. 5. Spacing (d-space) between (111) planes for electroformed Ni as a function of plating current density.

2.5 Release of microstructures

The next step is to remove the Ti sacrificial layer to free the electroplated Ni electrode from the bottom. Sacrificial layer etching involves considerably longer times than the standard etching steps carried out in IC technology. A 10% HF solution, that attacks Ti without attacking Ni and the plating base, is used as a selective etchant for this purpose.

In order to arrive at an appropriate etching time, square Ni test structures are electroplated on sputtered Ti layers of different thicknesses to determine the etching rate of Ti under Ni. The structures were etched for different times in a 10% HF solution. Each top Ni structure was then mechanically removed and the width of the unetched Ti layer remaining underneath is compared to the original square width to determine the etch rate of the

underlying sacrificial layer. Figure 6 shows the experimental results. The results indicate the etch rate to be almost independent of the Ti layer thickness for Ti thicknesses greater than $1\ \mu\text{m}$. The etch rate increases significantly when the etching apparatus is placed in an ultrasonic bath. Hence, this measure was employed for the beam release process in this work. Use of a higher concentration HF solution also increases the etch rate, but after some etch time it causes the plating base layer to crack. Hence, the concentration of HF in the etching solution is limited to 10% in this work.

Since a wet etch process is used to release the cantilever beams from the substrate, post-etch rinsing and drying procedures are critical because freestanding beams will often adhere to the substrate. High surface tension forces resulting from the rinse liquid trapped between the cantilever beams and the substrate can initiate this stiction. One means of reducing stiction is to use post-release rinse solvents with reduced surface tension, preferably at elevated temperatures, to reduce adhesion.⁽³⁵⁾

A plating base test structure shown in Fig. 7 is designed in order to investigate the release process and to determine the maximum freestanding cantilever beam length. This structure of isolated islands is defined on a Si wafer covered with silicon nitride and a Mo/Ag plating base layer. A $3\text{-}\mu\text{m}$ -thick Ti layer is sputtered and an opening for the anchor region of the cantilever beam is defined and etched. After coating the wafer with PMMA and exposing it to synchrotron radiation, the developed beam structures in PMMA were filled with $5\ \mu\text{m}$ of Ni by an electroplating process. The cantilever beams were then released through sacrificial layer etching and in the absence of stiction, each released beam formed a capacitance with another isolated part of the plating base. The presence of stiction shorted the beam by connecting it to the central electrode. Hence, by simply checking for the resistance between the beam and the central electrode, one can determine whether a beam is freestanding or not. For this experiment, beams in the range of 200–800

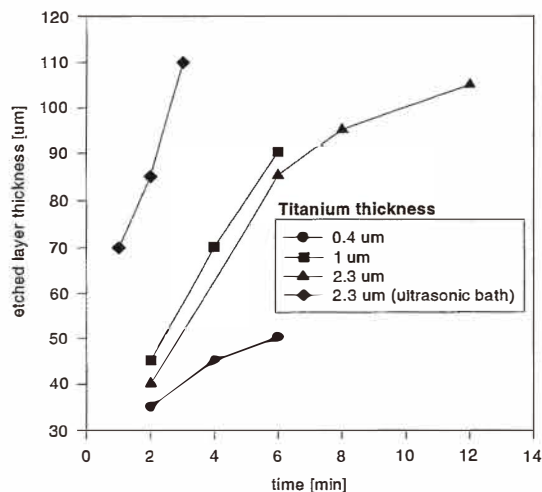


Fig. 6. Ti etch length underneath Ni in 10% HF solution as a function of etch time.

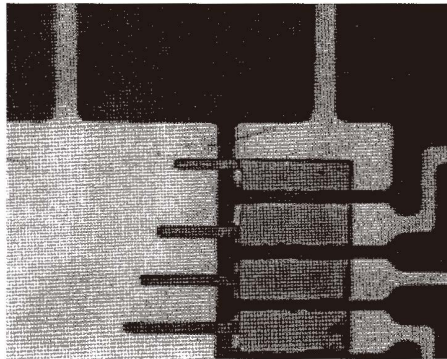


Fig. 7. Part of a test structure to examine the release of beams. The smallest beam shown here is 350 μm long.

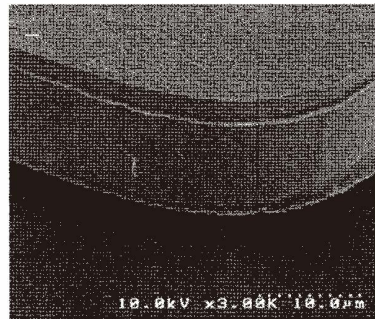
μm in length are designed. The sacrificial Ti layer is etched in a 10% HF solution and the sample is then rinsed in DI water. This is followed by a post-rinse in boiling methanol at 65°C, which has a lower surface tension than water. The samples are air-dried. The beams are electrically probed with microneedles to measure their resistance. The maximum freestanding cantilever beam length is found to be 200 μm . Rapid thermal annealing has been used to reduce stiction possibly due to the instability of the trapped liquid under tension.⁽³⁵⁾ In this work, the samples were slid into a furnace heated to 400°C for 10 s after the methanol rinse. The length of the freestanding beam structures now increased to 350 μm . In order to further increase the length of the freestanding beams, a rinse in a hydrophobic solution⁽³⁵⁾ is carried out following the methanol rinse and prior to the furnace annealing. A commonly used substance in photolithography, hexamethyldisilazane, is used as the hydrophobic agent. The freestanding beam length is now increased to 450 μm .

The maximum freestanding length is also a function of beam thickness. In this work, the Ni beam thickness could not be increased without significantly decreasing the sensitivity of the accelerometer. Our calculations indicate that a beam thickness of 10 μm results in a sensor output sensitivity of 0.1% or less with a Ni seismic mass plated at the beam tip.⁽³²⁾ Hence, the beam thickness in our design was restricted to 10 μm or less. With the process developed here, we are able to free 5- μm -thick cantilever beam structures of at least 450 μm length with a 3 μm Ti sacrificial layer.

The Mo/Ag plating base layers are now etched off from the unwanted areas on the chip. Figure 2g) shows the cross section of the released structure after sacrificial layer etching. Figure 8a) shows a micrograph of Ni LIGA beams fabricated in our laboratory after sacrificial layer etching. Figure 8b) indicates that the beam has been completely released from the underlying substrate. The current density can be varied with deposition time to change lattice d-spacing of the electrodeposited layer as seen from Fig. 5. The resulting stress gradient in the electroplated layer will cause the beam to buckle slightly upwards, away from the substrate. This is desirable to increase the fabrication yield of the freestanding beams.



a)



b)

Fig. 8. Released LIGA beams on a silicon chip. a) General view. b) Close-up view showing the release of beam from the substrate.

2.6 Annealing

The chip is now annealed at 350°C for 15 min in N₂ ambient to remove the effects of any radiation damage incurred during X-ray exposure. Figure 9 shows a micrograph of the fabricated circuit. The microsystem is now ready for packaging and testing.

3. Discussions and Summary

We have achieved the direct integration of a MEM structure fabricated by the LIGA technique with CMOS circuitry on the same chip by a post-IC fabrication process. A standard IC process is used to fabricate the CMOS circuits. A one-dimensional accelerometer is used as a vehicle to demonstrate this direct merging of LIGA technology with CMOS technology. The presence of the fabricated circuit restricts the processing of MEM structures to temperatures below 450°C. X-ray lithography is used to delineate the mechanical structure. The mask contrast ratio is crucial in preserving the performance of the fabricated circuit after radiation. The 3.5- μm -thick Au absorber used in this work is not

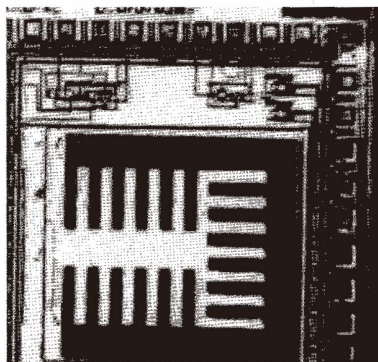


Fig. 9. View of the IC chip after fabrication of the LIGA structure.

sufficient to prevent the circuit from malfunctioning. The circuits became functional after annealing the samples up to 400°C but the effects of radiation damage could not be completely reversed. Future work will need to use higher contrast X-ray masks. The control of stress in all deposited layers is crucial in ensuring protection during long etching and X-ray exposure times. The latter can be significant for high aspect ratio MEM structures. Care is needed to deposit a conformal Mo layer without stress or pinholes for protection during the sacrificial layer etch. If a LIGA structure that requires a high operating voltage is used for electrostatic actuation, additional care will be required in design to route the higher voltage supply line away from the CMOS circuitry and in the choice of the thickness of the insulator beneath or around the supply line. The process sequence developed here can be also employed with a thick UV resist such as SU-8 which does not require X-ray exposure.

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