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Investigation of MEMS Packaging Using Multichip Module Foundries

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An investigation of the feasibility of packaging micro-electromechanical systems (MEMS) using advanced multichip module (MCM) foundry processes has been conducted. MCM packaging provides an efficient solution for the integration of MEMS with other microelectronic technologies. The MCM foundries investigated for MEMS packaging were the General Electric high-density interconnect (HDI) and chip-on-flex (COF) as well as the Micro Module Systems (MMS) MCM-D process. Bulk and surface micromachined test dies were packaged with CMOS electronics using these MCM foundries. Procedures were developed to successfully release and assemble the MEMS devices without degrading the MCM package or other die in the module. The use of MCM foundries enables the cost-effective development of microsystems in situations where monolithic integration of MEMS and microelectronics is not suitable.

1. Introduction

Multichip modules (MCMs) achieve many of the benefits of monolithic integration by combining a number of different integrated circuit dies, usually from different wafers and process technologies, on a common host substrate.[1] Hence, MCMs offer an attractive approach to integrating and packaging micro-electromechanical systems (MEMS) because of their ability to support MEMS and microelectronics on a common substrate without requiring changes in or compromises to the native fabrication processes.

MCM technology has significantly improved over the last decade in response to

requirements for better packaging and performance in microelectronics.[1] MCMs can assume many different appearances depending on factors such as the kind of substrate and the method of interconnection between dies. Commonly used substrate materials include ceramics, silicon, and laminates used in printed wiring boards (PWB). MCMs can generally be classified as having either patterned substrate, patterned overlay, or a combination of both. The majority of MCMs in use today are patterned substrate. In a patterned substrate MCM, the dies are located above the host substrate and the interconnection between dies is made through wiring on the substrate. Patterned overlay is an alternate approach to MCM packaging in that the dies are embedded in the substrate and the interconnects between dies are made via an overlay fabricated on top of the dies.

Interconnection between dies can be made using a variety of methods such as wirebonding, flip-chip solder bumps, or direct metallization. Beside the obvious size and weight benefits of MCM packaging, the close proximity of the dies allows for improved system performance by providing low-noise wiring and, in some cases, eliminating unnecessary interconnections.

The primary goal of our research is to investigate and develop methods of using foundry MCM technology for MEMS packaging. Custom MCM technologies designed for MEMS applications have been proposed[2,3] but have not yet become available as foundry services and may be costly. Successfully adapting existing MCM foundry technologies will provide a means for near-term and low-cost development of microsystems since these products will make a transition from research to manufacturing. The deposited thin-film multichip module (MCM-D), high-density interconnect (HDI), and chip-on-flex (COF) processes were chosen because they are available as foundries and represent high-performance packaging solutions.

Key considerations for MCM packaging of MEMS include whether to release the micromachined devices before or after packaging and the compatibility of the package materials with the MEMS release procedures. Most MEMS devices require a 'release' etch prior to operational use. The release process involves removing selected materials to create three-dimensional structures and, in some cases, to allow physical movement. Released MEMS devices are typically very fragile and require special handling. Consequently, it is desirable to release the devices after packaging especially when using foundries. However, many of the release etchants commonly used for MEMS are harmful to microelectronics and microelectronic packaging. Our results successfully demonstrate the feasibility of releasing MEMS devices after foundry MCM packaging without affecting the module or other microelectronic dies in the module.

2. MEMS Packaging Test Die

Sandia National Laboratory developed a concept of using specially designed chips for evaluating the impact of assembly and packaging on microelectronics,[4] and we have adopted this approach for evaluating MEMS packaging. Our MEMS packaging test dies incorporate a variety of devices and test structures designed to assess the impact of foundry MCM packaging on MEMS. Surface and bulk micromachined test dies were developed to

represent two of the prevalent MEMS fabrication technologies.

The surface micromachined MEMS packaging test dies were fabricated through the Multi-User MEMS Processes (MUMPs) and the Sandia Ultraplanar Multilevel MEMS Technology (SUMMiT) process. MUMPs is a three-layer polysilicon surface micromachining technology sponsored by the Defense Advanced Research Projects Agency (DARPA).[5] Silicon dioxide is the sacrificial material in this MEMS process and is removed with a wet etch in hydrofluoric acid (HF). Among the test structures on the MUMPs die are breakage detectors to monitor excess force and polysilicon resistors to monitor excess heating. Other devices on the die are representative of MEMS structures that might be used in an actual application. Table 1 lists general categories of devices on the MUMPs surface micromachined test die.

The SUMMiT process is a unique surface micromachining foundry offered by Sandia National Laboratories. This process has recently been extended to include five layers (four releasable) of structural polysilicon.[6] The polysilicon layers are separated by sacrificial layers of oxide that are etched away in HF or HF/HCl. The SUMMiT dies used in this research are not designed specifically for packaging but contain useful test structures and are used to provide a view of another surface micromachining process.

The bulk micromachined test die was fabricated through the Metal Oxide Semiconductor Implementation Service (MOSIS) using the Orbit CMOS MEMS process. The CMOS MEMS process is based on a standard 2 μm CMOS technology and has two metal and two polysilicon layers. Provisions are made to specify cuts in the overglass to expose the silicon substrate for bulk micromachining. In addition, regions of boron doping can be specified to form etch stops for anisotropic silicon etchants such as ethylene diamine pyrocatechol (EDP) and potassium hydroxide (KOH). These tools allow for bulk micromachining to be accomplished in the standard CMOS process.[7] Table 1 lists some of the device categories represented on our bulk micromachined test die. A sampling of integrated circuits such as ring oscillators for testing package interconnects is also included on the test die.

Table 1
MEMS device categories on test die.

Device category	Surface	Bulk
Electrostatic piston mirrors	√	
Electrostatic resonators	√	
Hinged/rotating devices	√	
Thermal actuators	√	
Variable capacitors	√	
Breakage detectors	√	√
Cantilevers	√	√
Polysilicon resistors	√	√
Suspended structures		√
Thermal bimorphs		√

3. MCM-D/MEMS Packaging

The first foundry MCM process we used for MEMS packaging was the Micro Module Systems (MMS) MCM-D process. MEMS packaging test chips were sent to the DARPA-sponsored MIDAS Foundry Access Service for MCM-D packaging. MIDAS provides access to low-cost, prototype quantities of MCMs by acting as a brokerage for MCM foundries.[8] Our MCM-D/MEMS packaging experiment was a pure foundry transaction in that our fabrication was treated as a routine work order with no special handling requirements. MIDAS handled the entire transaction, and there was no interface between the authors and MMS. Table 2 lists the characteristics of the MMS MCM-D package, and Fig. 1 shows a photograph of one of the MCM-D/MEMS modules.

Table 2
Characteristics of MCM-D package.[8]

Property	MMS MCM-D
Substrate material	Aluminum
Signal/power wiring layers	3/2
Dielectric material	Polyimide
Conductor metallization	Copper
Die attach adhesive	Ablebond 789-3
Die interconnect method	Wirebond
Die edge-to-edge spacing	> 500 μm
Max. operating frequency	100 – 400 MHz

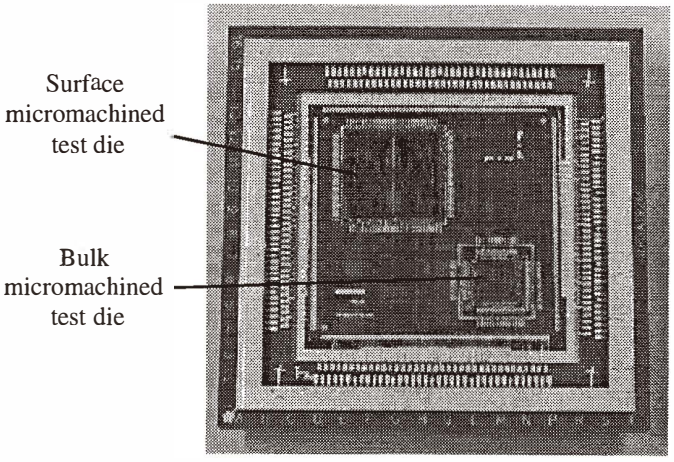

Fig. 1. MCM-D/MEMS package.

The MMS MCM-D is a patterned substrate MCM and represents the conventional packaging approach where the interconnect layers are deposited on the substrate and the dies are mounted above the interconnect layers. The interconnect between the die and the substrate is made through wirebonding. The MMS MCM-D is one of three foundry processes offered by MIDAS.[8] We chose the MMS process because its substrate and wiring materials are most compatible with the release procedure for the surface micromachined test die as explained in the next section.

3.1 *Postprocessing of bulk micromachined die in MCM-D package*

After packaging, the modules were returned to the Air Force Institute of Technology (AFIT) for postprocessing and release. We typically use a wet etch procedure for releasing unpackaged bulk micromachined test die (Table 3). However, the wet etch procedure was incompatible with the packaging materials used in the MCM-D process. The MCM-D module was not able to withstand the extended EDP or KOH etch. The polyimide dielectric used in the MCM substrate tended to crack and delaminate. Tetramethyl ammonium hydroxide (TMAH) was also used as a substitute etchant for EDP, but cracks and delamination still occurred. The cracks were large enough to allow etchant to penetrate the surface and delaminate the polyimide.[9]

Consequently, we investigated the feasibility of using xenon difluoride (XeF_2), which is an isotropic dry (gas phase) etchant for silicon. One of the desirable attributes of XeF_2 is that it appears to have near infinite selectivity to many materials such as silicon dioxide, silicon nitride, photoresist, and aluminum, which are commonly used in microelectronics and packaging.[10] Hence, XeF_2 can be easily masked by materials such as photoresist and silicon oxide.[10] The combination of high selectivity with ease of masking made XeF_2 an excellent choice for our MEMS/MCM experiments.

MCM-D packaging samples and MEMS test dies were sent to the University of California at Los Angeles (UCLA) to validate their compatibility with XeF_2. At UCLA, etching is conducted in a computer-controlled multichambered system that provides precisely metered pulses of XeF_2 gas.[10] This system has been demonstrated to provide consistent and reliable etching of bulk silicon.

The bulk micromachined test dies were designed for release by an anisotropic etchant such as EDP which is easily controlled through the use of P-doping to form etch stops or the natural stopping mechanism at the convergence of crystal planes.[7] XeF_2 is an isotropic

Table 3
Wet etch release procedure for bulk micromachined test die.

1.	Dip in 10% HF for 10 s
2.	Soak in deionized water for 5 min
3.	Etch in EDP at 95°C for 45 – 60 min
4.	Soak in deionized water for 5 min
5.	Soak in 2-propanol for 5 min
6.	Dry on hot plate at 50°C

etchant, and there are no etch stops to control etch progress. However, we found that the MEMS structures could be safely and reliably released with XeF_2 by periodically monitoring etch progress. Furthermore, the package samples subjected to the XeF_2 release procedure showed no sign of being impacted by exposure to the gas. This was not a surprise as many of the materials in the MCM-D package had been previously verified in XeF_2.[10]

After the compatibility of the test dies and the package samples was established, a populated MCM-D/MEMS package was etched in the XeF_2 chamber. The surface micromachined die was masked with tape to protect it from the XeF_2 etch. The module was etched to an approximate depth of 70 μm. Figure 2 shows some of the released bulk micromachined microstructures on the MCM-D/MEMS packaged test die.

3.2 *Postprocessing of surface micromachined die in MCM-D package*

The surface micromachined die in the MCM-D/MEMS package was released after XeF_2 etching of the bulk micromachined die. The MCM-D package was able to withstand the wet etch procedure for the surface micromachined test die (Table 4). Consequently, the main issue was protection of the silicon dioxide on the released bulk micromachined die. Testing of various encapsulants and photoresists demonstrated that the positive photoresist is an effective mask against HF etch if the masked region is not immersed in the acid bath.[9] Even when not immersed in the acid bath, HF vapor is still capable of etching silicon dioxide. If the entire module must be immersed, a negative photoresist can be used as a mask. However, negative photoresists were found to be more difficult to remove after soft baking than positive resists that require only an acetone bath. This is particularly important when working with released microstructures.

The bulk micromachined die was carefully coated with the positive photoresist, and the module was soft baked for 20 min at 60°C. The procedure in Table 4 was then used to

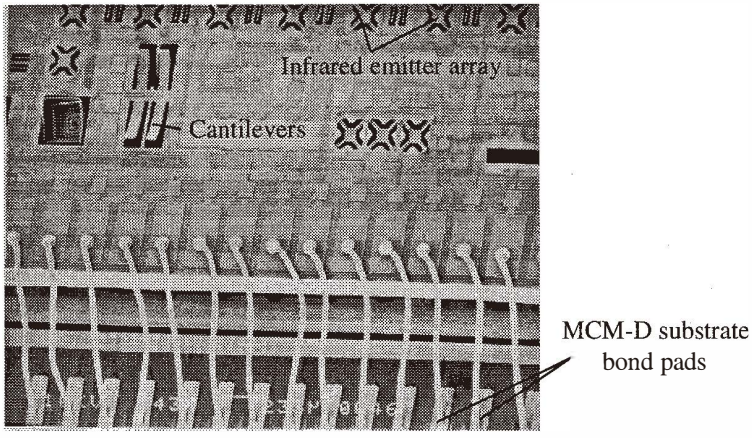

Fig. 2. Released bulk micromachined test die on the MCM-D/MEMS module.

Table 4
Wet etch release procedure for surface micromachined test die.

1.	Soak in 2-propanol for 5 min
2.	Dry on hot plate at 50°C
3.	Etch:
	MUMPs: 49% HF for 2 min 30 s
	SUMMiT: 49% HF for 20 min or 50/50 HF/HCL for 30 min
4.	Dip in deionized water for 5 s
5.	Soak in 2-propanol for 10 min
6.	Dry on hot plate at 50°C

successfully release the devices on the MCM-D packaged surface micromachined test die. The bulk micromachined die was not submerged in the HF acid bath. After the surface micromachined die was released, the entire module was soaked in acetone to remove the protective photoresist coating on the bulk micromachined test die. Figure 3 shows devices on the surface micromachined die. Subsequent analysis of the module showed no impact on the bulk micromachined test die or MCM-D wiring. The micromachined devices on both MEMS test dies operated as designed, and the CMOS electronics on the bulk micromachined test die performed as expected.

4. High-Density Interconnect (HDI) and Chip-On-Flex (COF)/MEMS Packaging

HDI and COF processes are similar in that they are both patterned overlay MCMs. Both of these MCM foundry processes have several attractive features for MEMS and electronics packaging. The die interconnects have very low parasitic capacitance and inductance due to the use of direct metallization. HDI/COF packaged systems can operate at well over 1 GHz.[11] Other benefits include three-dimensional packaging, the ability to locate bond pads virtually anywhere on the die, and MCM reparability.[12] Table 5 lists HDI and COF package characteristics.

COF is an extension of the HDI technology developed in the late 1980's. The HDI "chips first" process consists of embedding bare dies in cavities milled into a ceramic substrate and then fabricating a layered thin-film interconnect structure on top of the components. Each layer in the HDI interconnect overlay is constructed by bonding a dielectric film on the substrate and forming via holes through laser ablation. Metallization is created through sputtering, electroplating, and photolithography.[12]

COF was created to provide low-cost multichip packaging. Its performance approaches that of other high-performance MCMs such as HDI.[13] COF processing retains the interconnect overlay used in HDI, but molded plastic is used in place of the ceramic substrate. Figure 4 shows the COF process flow. Unlike HDI, the interconnect overlay is prefabricated before chip attachment. The bottom layer of the overlay is usually Kapton.

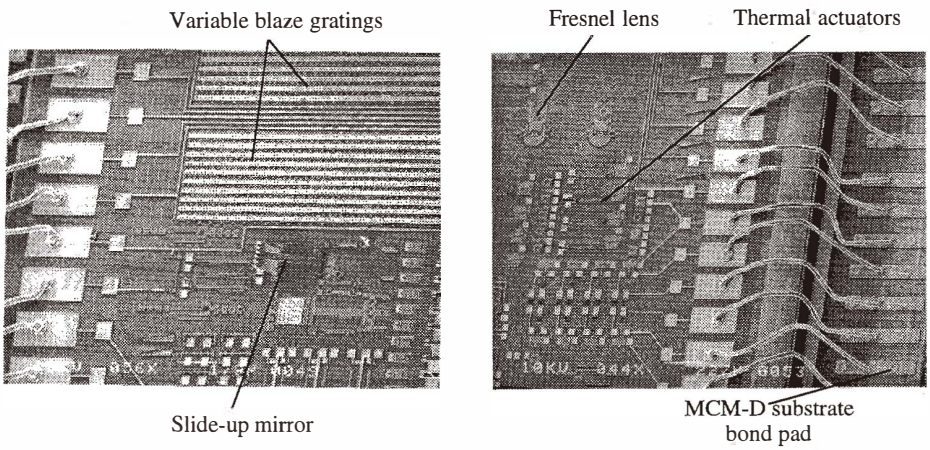

Fig. 3. Released surface micromachined test die (MUMPs) on MCM-D/MEMS module.

Table 5
Characteristics of HDI and COF packages.

Property	HDI	COF
Substrate material	Alumina	Molded plastic
Signal/power wiring layers	9 (1 layer used in this research)	3 (1 layer used in this research)
Overlay dielectric material	Kapton	Kapton/Ultradel
Conductor metallization	Ti/Cu/Ti	Ti/Cu/Ti/TiW/Au/TiW
Die attach adhesive	Ultem	Ultem
Die interconnect method	Direct metallization	Direct metallization
Die edge-to-edge spacing	> 375 μm	> 800 μm
Max. operating frequency[12]	> 1 GHz	> 1 GHz

The top layer of the overlay can also be Kapton; however, a spin-on or spray-on polyimide such as Ultradel can be substituted. Copper is used for metallizing the prefabricated overlay.

The chip(s) are attached face down on the COF overlay using a thermoset adhesive. After the chip(s) have been bonded to the overlay, a substrate is formed around the components using a plastic mold forming process such as transfer, compression, or injection molding. The module temperature does not exceed 210°C during substrate molding. The next step in the process is to electrically connect the die to the overlay. This is accomplished by laser drilling vias through the overlay to the component bond pads. Next, sputtered Ti/Cu followed by additional electroplated Cu is applied to the module

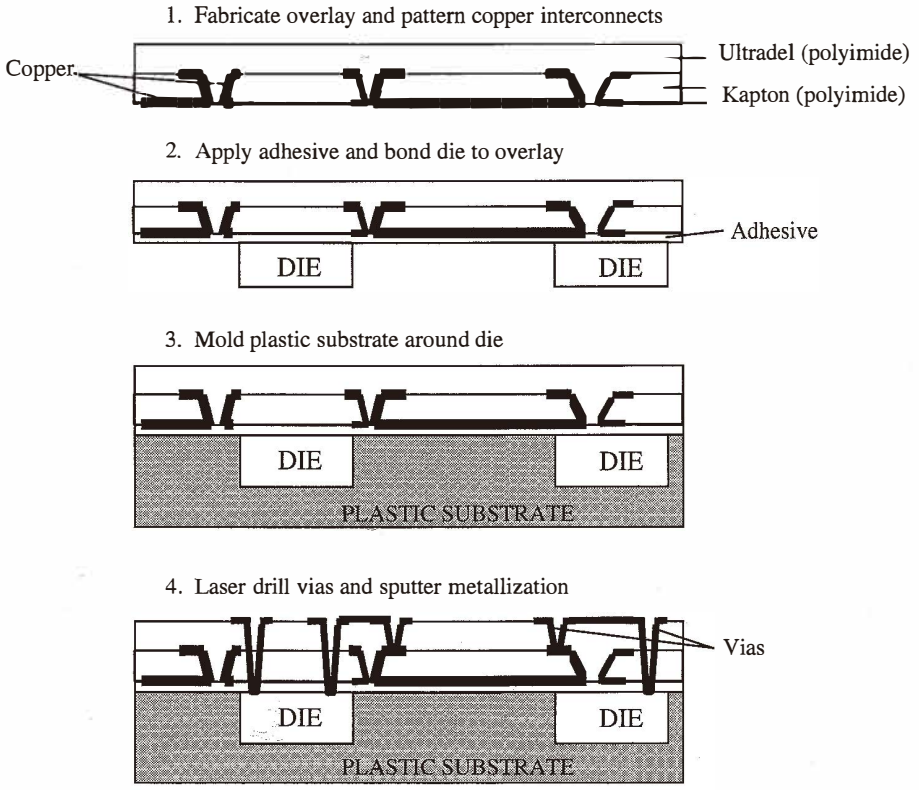

Fig. 4. Chip-on-flex process flow (after Fillion *et al.*[13]).

surface. This metallization is then patterned to form electrical interconnects. Different kinds of top layer metallizations can be used depending on the target application.

Unlike the MMS MCM-D, the HDI and COF foundry processes require additional processing for MEMS packaging since the dies are embedded in the overlay with no access to the microdevices. Therefore, General Electric, the developer of the HDI process, was contacted for assistance in creating a low-impact method of adapting the HDI foundry process for MEMS packaging. Our approach for packaging MEMS die in the HDI and COF processes is to add an additional laser ablation step to allow physical access to the MEMS devices as shown in Fig. 5. Additional plasma etching is also performed to minimize the amount of ablated dielectric residue that can accumulate in the exposed windows.

The surface and bulk micromachined test dies were packaged at the General Electric Corporate Research and Development Center using the HDI and COF procedures. The test dies were packaged in modules containing a generic CMOS electronics die and ablation

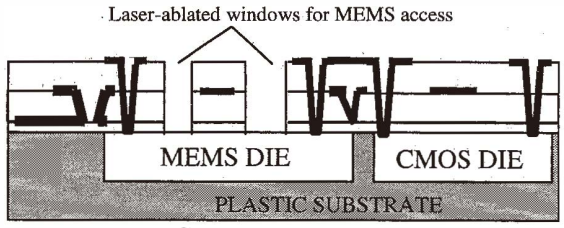

Fig. 5. Large-area ablation for MEMS access in chip-on-flex package.

test cells. After passivation, windows in the dielectric overlay above the MEMS die were selectively opened using laser ablation. The ablation was accomplished with a continuous argon ion laser (350 nm wavelength). The laser spot was circular with a nominal diameter of 9 μm. The initial laser power was approximately 1.6 W and the scan rate was 360 μm/s for the first fabrication lot. For subsequent lots, the ablation power was varied to reduce the risk of damage to the MEMS die.

4.1 *Postprocessing of surface micromachined die in HDI and COF packages*

The HDI and COF/MEMS samples containing the MUMPs surface micromachined test die were released using the procedure shown in Table 4. Material compatibility tests conducted prior to packaging indicated that the Kapton dielectric, adhesives, and substrates used in the HDI and COF packages should survive the release procedure. Examination of the modules after release showed no evidence of deterioration of either package for the short MUMPs release etch.

The MEMS devices on the packaged MUMPs test die performed electrically and mechanically in the same manner as devices on unpackaged control die. Rotating, hinged and flip-up devices moved freely and operated as designed. In addition, devices were operated through the package pads which demonstrated good continuity through the overlay and onto the MEMS die. Finally, the overlay protected embedded CMOS electronics die from the release etch as expected. Figure 6 shows a HDI/MEMS module with a MUMPs and CMOS electronics die, and Fig. 7 shows released MEMS devices in several of the ablated windows in a COF/MEMS module.

SUMMiT surface micromachined dies were also packaged using HDI and COF/MEMS processes. SUMMiT die require a much longer HF release etch than MUMPs due to the existence of more oxide layers and the slower etch rate of oxide in the SUMMiT process. HDI and COF/MEMS modules were released using both a 20-min HF etch and a 30-min HF/HCl etch. Figure 8 shows released devices on a SUMMiT die in a COF/MEMS package.

The ceramic HDI substrate and the overlay were not affected by either the long HF or HF/HCl release etch for SUMMiT die. The molded plastic COF substrate was largely unaffected after the long etches but did show a slight loss of grains from the matrix on exposed surfaces. The loss of grains was determined to be limited to the surface, and the

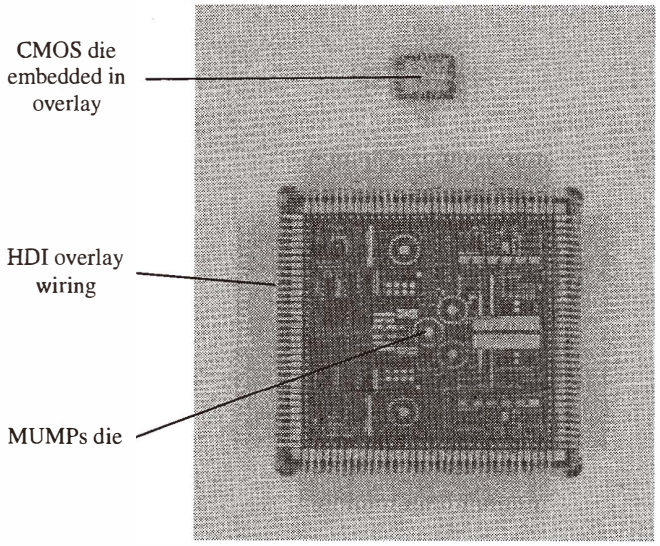

Fig. 6. MUMPs surface micromachined test die in HDI/MEMS module.

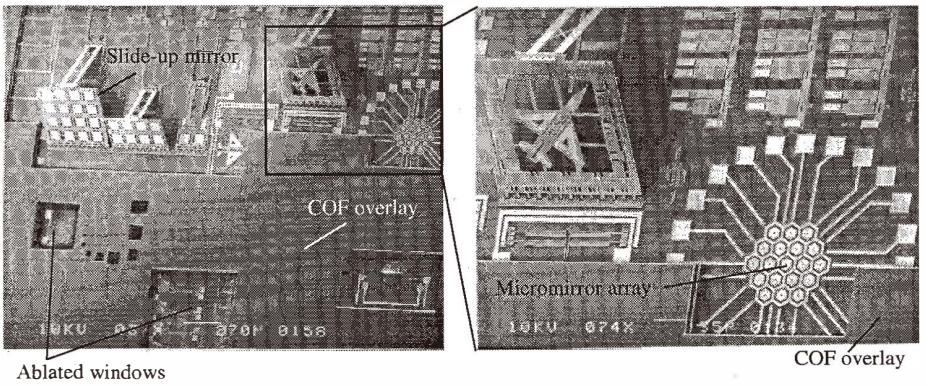

Fig. 7. Released MUMPs surface micromachined devices in COF/MEMS module. The large slide-up mirror has a height of 650 μm when fully elevated. The airplane has a length of 500 μm.

COF/MEMS modules were still serviceable with no discernible impact on the overlay or any embedded CMOS die. Some of the modules etched longer than 30 min showed slight delamination of the overlay at the periphery of the package, but no delamination was observed in the windows ablated for MEMS access.

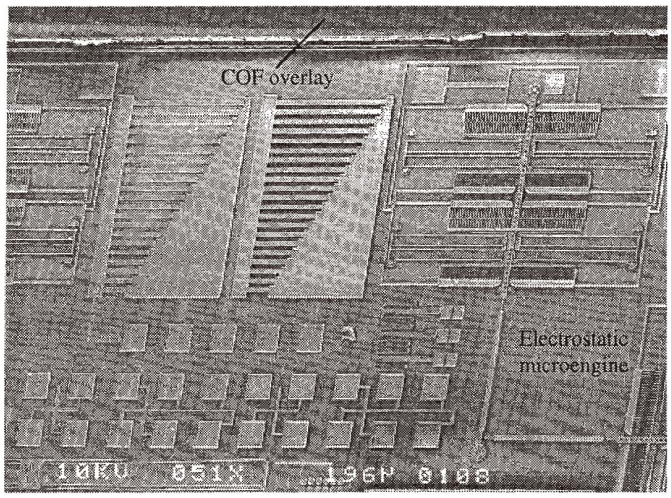

Fig. 8. SUMMiT surface micromachined die in COF/MEMS package. The microengine and other devices on the die were designed and fabricated at Sandia National Laboratory.[6]

4.2 *Reducing heat-induced damage from laser ablation*

The most serious problem discovered during postpackaging analysis of the surface micromachined test die was the potential for MEMS device warping or failure due to excessive heating from laser ablation. Devices most susceptible to overheating were long, thin structures with poor heat loss paths to the substrate. Polysilicon resistors in areas that received high laser ablation power also showed resistance drops of 10–15%, which is consistent with the change in resistance encountered during polysilicon resistor trimming.[14] Moreover, devices in smaller ablated windows were also more likely to show thermal damage from laser ablation.

4.2.1 *Sources of heat damage from HDI/COF ablation*

The properties of materials used in MEMS fabrication are pertinent to efforts of minimizing the potential for damage during laser ablation of the dielectric overlay. The ablation of HDI/COF is accomplished with a continuous argon ion laser at 350 nm. This wavelength is particularly conducive to damaging polysilicon devices in the MUMPs process because polysilicon absorbs virtually all of the incident laser energy at 350 nm.[15] The top polysilicon layer (*Poly 2*) in MUMPs is particularly vulnerable to heat damage because it is uncovered and directly exposed to the laser beam during ablation. The underlying polysilicon layers can also receive a high fraction of the incident laser power when they are only covered by sacrificial layers of silicon dioxide since the optical transmittance of silicon dioxide is approximately 90 percent at 350 nm.[16]

Another contributor to heat damage is the nature of the ablation process. The ablation in the HDI and COF/MEMS process is primarily a photothermal phenomenon. The "pulse

width" of the laser used in the COF/MEMS process can be defined as the amount of time that the half power beam width (HPBW) of the beam covers a point on the surface.[17] By this definition, the pulse widths of bulk ablation and ablation polish steps are 6.67 ms and 1.67 ms, respectively. Ultraviolet laser ablation of polyimides using pulse widths greater than one millisecond has been shown to be primarily a photothermal reaction.[17–20]

The temperature threshold for the photothermal ablation of Kapton at 350 nm was reported as a minimum of 850°C.[18,20] The optimum photothermal ablation of Kapton was also theorized to occur at temperatures ranging from 1,100–1,500°C.[19] As a result, any material in close proximity to the Kapton ablation, such as an embedded MEMS die, may be subjected to a heat source of at least 850°C and potentially as high as 1,500°C. Temperatures of this magnitude can easily cause failure in polysilicon structures.

4.2.2 *Development of optimized overlay ablation procedure*

One obvious method to reduce the potential for heat damage was to find the minimum power and time required for ablating through the overlay. This was accomplished by conducting a detailed study and analysis of the HDI/COF laser ablation process. During the study, the ablation of the Kapton overlay was measured while varying laser power and scan rate. The HPBW of the laser is nominally 9 μm. For each pass, the laser is scanned laterally across the surface of the module for a distance of 6–12 mm. After the scan is completed, the laser is stepped vertically 3 μm and reverses its course. A shutter is used to control laser beam impact on the surface of the module. The scan rates of the laser are 150 Hz in the bulk ablation mode and 600 Hz for the ablation polish used for cleaning up residual material.

Several COF package samples were tested to characterize the progress of laser ablation by measuring the depth of ablation as a function of power level. COF package samples with two layers of Kapton were used for these experiments. The overlay was approximately 60 μm thick since each layer of Kapton has a nominal thickness of 25 μm and the two adhesive layers are each 5–10 μm thick. Windows were ablated in the test sample overlay while varying laser power from 1–4 W for bulk ablation and 1–5 W for the ablation polish. Following each pass at a particular power level, the depth of the overlay ablation was measured with a profilometer. Figure 9 shows the results of this investigation.

After the laser ablation process had been characterized, an optimal ablation protocol was developed. The first HDI/MEMS module that showed MEMS device damage was ablated with a power of 1.6 W. However, power was not reduced until the laser was within a few microns of the embedded die. We subsequently developed and implemented a new procedure that uses a series of ablation steps that gradually reduce the effective ablation power as the overlay is removed. In addition, alternative methods of overlay removal such as plasma cleaning and high-pressure water scrubs are also employed. The steps of this optimized procedure are shown in Table 6.

The first ablation step is designed to rapidly remove a large portion of the overlay. This bulk ablation step is accomplished with 3 passes at 2 W and removes the first layer of Kapton and the interlayer adhesives (~ 30 μm). The second ablation step uses a lower power and consists of 5–7 passes at 1 W. This step ablates the bottom Kapton layer (~25 μm) and leaves only the lower adhesive layer to be removed by the ablation polish. The

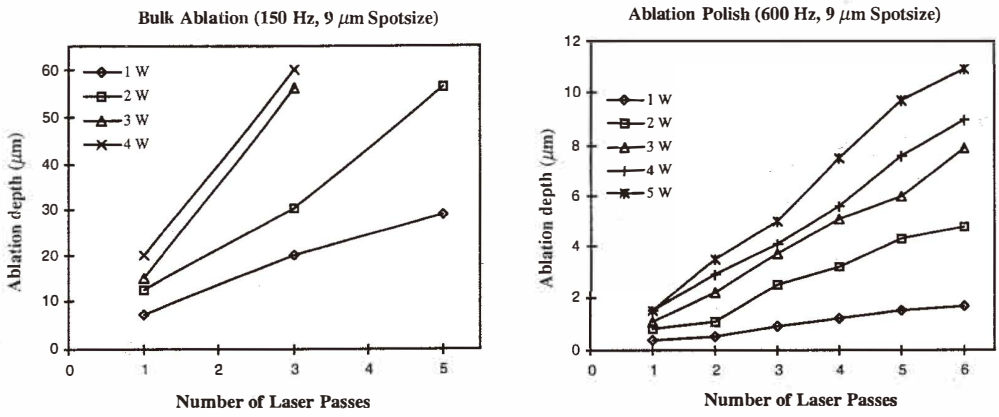

Fig. 9. Ablation depth versus power level for laser ablation of HDI/COF overlay.

Table 6
Optimized ablation protocol for HDI and COF/MEMS overlay.

Process step	Power (W)	Scan rate (Hz)	Passes over entire module	Duration (min)
1. High-power bulk ablation	2	150	3	N/A
2. Low-power bulk ablation	1	150	5–7	N/A
3. Ablation polish	3	600	6	N/A
4. Plasma etch (O_2 @ 1 Torr)	300	N/A	N/A	60–90

Note: A high-pressure (500 psi) water scrub is performed after each step
Laser characteristics: continuous argon laser (350 nm)
9 μm HPBW
3 μm center-to-center spacing between adjacent laser scans

ablation polish (6 passes, 3 W, 600 Hz) cleans up most of the residual dielectric and adhesives. Although a higher continuous power is used for the polish step, the faster scan rate lowers the effective power for ablation. A high-pressure water scrub is also used after each ablation step to minimize residue accumulation.

A plasma etch is used after the ablation is completed. An oxygen (O_2) plasma etch (< 90 min) was found to be very effective in removing residue left behind after the ablation polish. The use of high pressure (~ 1 Torr) and a cold chamber (< 100°C) minimizes etching of oxides or nitrides on the packaged die. The final step is a high-pressure water scrub to remove any silica residue that may remain on the surface of the MEMS die.

The use of the optimized ablation protocol was very successful. The result of the

optimized process is a very clean ablation with little residue in the ablated cavity. The use of the optimized ablation protocol in conjunction with plasma cleaning significantly reduced the occurrences of laser-induced damage on the test die. Figure 10 shows a small, ablated window containing two scanning micromirror systems[21] that were successfully packaged and released with no evidence of warping or heat-induced damage. The window in the overlay was ablated using the procedure in Table 6. The scanning mirrors were damaged or destroyed when the window was ablated using higher ablation power. These devices have the same resistance and deflection characteristics as similar devices on an unpackaged control die, which indicates no change in performance as a result of packaging, ablation, and release.

4.2.3 *Thermal insulation using protective layers*

Another method of reducing heat damage is to apply a protective layer on the surface of the MEMS die to provide thermal isolation from the heat generated during laser ablation. We initially investigated the usefulness of applying oxide layers over the MEMS die as a means of minimizing residue accumulation on exposed microdevices.[22] One of the additional benefits of the protective oxide coating was that it reduced the vulnerability of the MEMS devices to laser ablation.

MEMS devices in areas with oxide coating show noticeably less evidence of laser heating damage even when the ablation was done at 1.6 W. The thermal conductivity of silicon dioxide is 1.0–1.4 $W K^{-1}m^{-1}$[23] which is much lower than that of silicon (156 $WK^{-1}m^{-1}$)[24] or polysilicon (30 $WK^{-1}m^{-1}$).[24] The presence of a sputtered oxide or spin-on-glass protective layer is particularly effective in reducing the occurrence of heat damage in MUMPs *Poly 2*

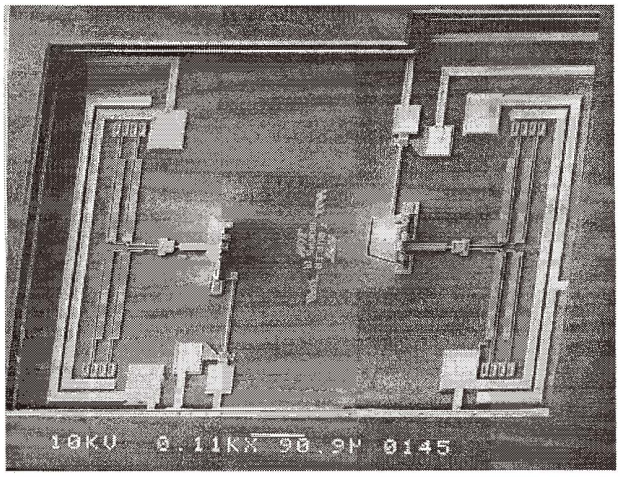

Fig. 10. Scanning micromirrors packaged and assembled in COF/MEMS module without laser heating damage. The optimized ablation procedure and a 300 nm protective oxide coating were used.

structures. *Poly 2* devices are exposed on the surface of the die and have no isolation from the thermal effects of ablation.

4.3 *Postprocessing of bulk micromachined die in HDI and COF packages*

Similar to the MCM-D/MEMS experiment, HDI and COF package materials were not able to withstand the wet etch procedure for bulk micromachined test die;[9] thus, XeF_2 was investigated as an alternative etchant. COF and HDI package samples were sent to UCLA for compatibility testing in their XeF_2 etch chamber. The samples were etched in XeF_2 along with two of the bulk micromachined test dies. The etching continued until an etch depth of approximately 70 μm was achieved on the test dies. The package samples subjected to the XeF_2 release procedure appeared unaffected by exposure to the gas. Inspection of the package samples after etching revealed no impact to either COF or HDI substrates or overlay after the 15–20 min exposure to XeF_2.

A populated COF/MEMS package was etched in the XeF_2 chamber after the compatibility of the test die and the package samples was established. The module was etched to an approximate depth of 50 μm. Figure 11 illustrates that a wide variety of bulk micromachined devices can be COF packaged and released using XeF_2. The cantilevers are composed of metal and polysilicon which are encased in oxide. Each cantilever is 250 μm long and 70 μm wide. Fragile structures such as the spiral shown in Fig. 11 were also successfully packaged and released. The width of the spiral arm is only 12 μm wide and is formed from polysilicon and metal encased in silicon dioxide. Perhaps the best endorsement of the success of the packaging experiment was that all of the bulk micromachined devices were released without affecting the functionality of the package or the CMOS microelectronics on the test die.

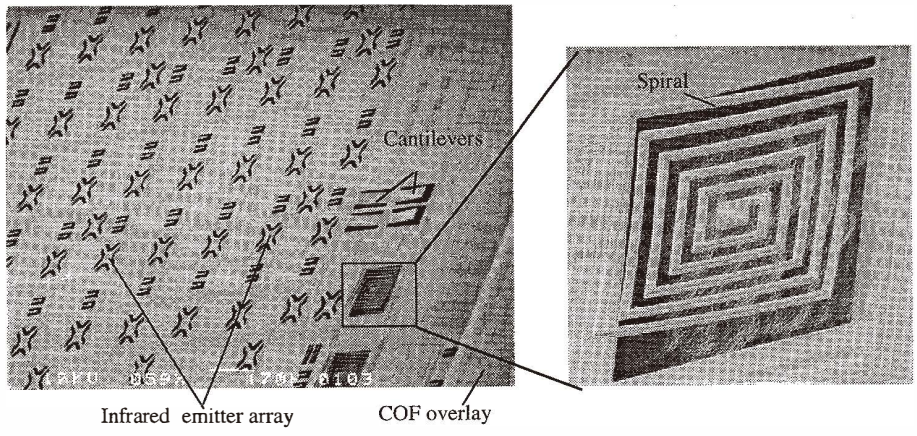

Fig. 11. Structures on released bulk micromachined test die in COF/MEMS module.

5. Discussion

The feasibility of packaging of bulk and surface micromachined MEMS using foundry MCM processes has been demonstrated. Bulk and surface micromachined test dies were packaged using the MMS MCM-D and the General Electric high-density interconnect and COF MCM foundries. Procedures were developed and implemented for successfully releasing the MEMS die after packaging. Xenon difluoride (XeF_2) was found to be an excellent postpackaging etchant for MCM packaged bulk micromachined MEMS die. For surface micromachining, HF can be used for the release of MEMS after MCM packaging.

Methodologies to reduce the potential for MEMS device damage due to laser ablation and accumulation of residue were also implemented. Ablation-induced damage can be mitigated through lowering of ablation power, use of protective coatings, and prudent use of plasma etching. Furthermore, the importance of test die and structures dedicated to the effects of packaging and assembly was affirmed. Failure modes of MEMS devices can differ significantly from macroscale devices and microelectronics.

Finally, all of the MCM packages, MEMS dies, and CMOS microelectronics used in this research were foundry fabricated. In addition, we made a concerted effort to use and develop simple postprocessing procedures for release and handling of the MEMS/MCM packages. The increasing availability of affordable, high-performance foundry processes combined with the postprocessing techniques presented in this paper should allow a wide range of developers to implement robust and cost-effective microsystems.

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