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Hydrogen-Induced Interface Traps in a Palladium/Very Thin Oxide/Silicon Structure

Kentaro Ito

Department of Electrical and Electronic Engineering, Faculty of Engineering,
Shinshu University, 500 Wakasato, Nagano 380, Japan

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Hydrogen sensitivity of the palladium/very thin oxide/silicon structure was investigated by using capacitance and conductance methods. A decrease in the palladium work function and a buildup of trap levels at the oxide-silicon interface on exposure to hydrogen, both of which contribute to the hydrogen sensitivity, were estimated separately. Peaks in the incremental interface trap density were observed at 0.6 eV and 0.4–0.5 eV above the silicon valence band edge. Origins of the interface traps were discussed in terms of chemical bonds which were modified by absorbed hydrogen.

1. Introduction

A Pd MOS diode consisting of a thin Pd film, very thin (< 5 nm) silicon oxide and n-type silicon is an interesting device that is sensitive to a small amount of hydrogen existing in the ambient.[1] This solid-state chemical sensor can be integrated with silicon microelectronic circuitry because it operates sensitively at room temperature.[2] So far, hydrogen sensitivity has been explained in two ways. Some authors attributed reversible changes in the device characteristics to a decrease in the work function of the Pd film on exposure to hydrogen,[1–3] while others attributed them to hydrogen-induced trapping states at the interface between the oxide and the silicon.[4,5]

The hydrogen sensor studied in this paper is based on the characteristics peculiar to two thin films: the first one is a vacuum-evaporated Pd film, 20 nm thick; the second one is a very thin silicon oxide which is formed on single crystal silicon by heating in a dry oxygen

atmosphere. The Pd thin film is used because hydrogen molecules adsorbed on its top surface are dissociated into hydrogen atoms which in turn easily diffuse toward the silicon oxide even at room temperature. It is well known that the presence of silicon oxide formed on a silicon surface is able to drastically eliminate high-density dangling bonds and also high-density surface states as a consequence which would exist on a bare silicon surface. Since the oxide employed in our device is so thin that electrons or holes can tunnel through it, the current-voltage characteristics as well as capacitance-voltage characteristics of the device are similar to those of Schottky diodes. It is also possible that the gas species adsorbed at the interface of Pd and silicon oxide penetrate the extremely thin oxide to interact with the silicon surface.

By assuming two hydrogen-induced interface states, Keramati and Zemel showed for the first time that the measured admittance of the Pd MOS diodes can be explained on the basis of a theoretical model.[4] Petty also showed the existence of two electron traps at the interface using deep-level transient spectroscopy.[5] However, in these two reports the trap energy levels were located at different energy positions in the silicon band gap.

In this paper, we investigate hydrogen-induced changes in the interface trap density and the built-in potential of both Pd/SiO_2/n-Si and Pd/SiO_2/p-Si diodes using low-frequency and high-frequency capacitance methods, respectively. We have revealed that independent of the silicon conductivity type used, the interface trap distribution has a main peak near midgap and a subpeak below midgap. The former peak has also been detected using the conductance method. The ambient used is room air to which this sensor would be most frequently applied to detect hydrogen.

2. Methods

Monocrystalline n-type, 7 Ω cm and p-type, 3 Ω cm silicon wafers with (111) crystal orientation were used as substrates. The Pd MOS diodes were prepared by the same methods as described in a previous paper.[6] The diode was inserted into a vessel and kept at room temperature in the dark. The ambient gases used were ordinary room air, desiccated (dry) air and room air containing 2,000 ppm H_2. The small-signal ac capacitance and conductance of the diode were measured under various dc bias voltages over a frequency range from 10 Hz to 1 MHz using an impedance analyzer (YHP 4192A).

We estimated the interface trap density D_{it} from the low-frequency capacitance method as follows.[7]

$$D_{it} = \frac{1}{Aq}\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \frac{C_s}{q}, \tag{1}$$

Here, q is the electronic charge, A is the area of the gate metal (Pd film), C_{LF} is the low-frequency (10 Hz) capacitance which is the average of twenty measurements, C_{ox} is the oxide capacitance obtained from the diode capacitance at large forward bias, and C_s is the

silicon surface capacitance per unit area which can be theoretically determined from silicon band bending. The value for Ψ_s was calculated using the relation

$$\Psi_s = \Psi_{s0} + \int_0^V \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV, \tag{2}$$

where Ψ_{s0} is band bending at the applied voltage $V = 0$ and equal to the built-in potential of the diode. We estimated this from high-frequency (1 MHz) capacitance-voltage characteristics at reverse bias. The value of D_{it} calculated from eq. (1) is the interface trap density at the energy position E which is expressed by the following equation and is located opposite the majority carrier Fermi level of the bulk silicon. In the silicon band gap E_g, energy E is given by

$$E - E_v = E_g - kT \ln\left(\frac{N_c}{N_D}\right) + q\Psi_s, \tag{3}$$

where E_v is the energy of the valence band edge, k is the Boltzmann constant, T is the absolute temperature, N_c is the effective density of states in the conduction band, and N_D is the bulk doping level.

The conduction method is known to have advantages over the above capacitance method.[7] For instance, by using the former method one can not only measure the interface trap density with high accuracy but also determine the cross section of the traps. The interface trap density was estimated from the small-signal parallel conductance of the diode G_p as

$$D_{it} = \frac{\left(G_p/\omega\right)_p}{qAf_D}, \tag{4}$$

where $(G_p/\omega)_p$ is the peak value of a G_p/ω versus frequency f curve, ω is the angular frequency and f_D is the factor that is determined by statistical fluctuation of band bending and can be measured from the width of the peak. The values of G_p/ω were calculated from the diode conductance and capacitance as

$$\frac{G_p}{\omega} = \omega C_{ox}^2 \left(G_m - G_{dc}\right) \Big/ \left[\left(G_m - G_{dc}\right)^2 + \omega^2 \left(C_{ox} - C_m\right)^2\right], \tag{5}$$

where G_{dc} is the conductance deduced from the dc current-voltage characteristics of the diode and G_m (C_m) is the conductance (capacitance) measured at an angular frequency of ω.

3. Experimental Results

Figure 1 shows the capacitance-voltage (C-V) curves for the Pd/SiO_2/n-Si diode in room ambient and also in that containing 2,000 ppm H_2. The frequency-dependent capacitance of the diode indicates the existence of interface traps. The increase in capacitance on exposure to hydrogen is due partly to a decrease in the built-in potential of the diode, i.e., silicon band bending at zero bias, and to an increase in trap density as described before. The oxide capacitance C_{ox} was determined to be 95 nF from the low-frequency capacitance at large forward bias (3V). Therefore, the thickness of an oxide layer is estimated to be 2.6 nm from C_{ox} using the dielectric constant of 3.9 for the oxide.

Figure 2 shows $1/C^2$-V curves at 1 MHz for the same diode as above. Both curves measured in room air and hydrogen-containing air can be approximated by straight lines that are parallel to each other at the reverse bias. The donor concentration in the n-type silicon, which is calculated from the slope of the lines, is 8.8×10^{14} cm^{-3}, in fair agreement with the value of 7.1×10^{14} cm^{-3} obtained from resistivity measurement. Extrapolation of the straight portion of the curves to the voltage axis gives us the built-in potential of the diode, i.e., 0.59 V in room air and 0.37 V in hydrogen-containing air.

Figure 3 shows G_p/ω-f curves for the diode with bias as a parameter. The peaks of the curves are always broader than those due to single-level traps.[7] This broadening of the peaks indicates a distribution of band bending fluctuation originating from localized interface charges. Moreover, the peak for the diode exposed to hydrogen-containing air is

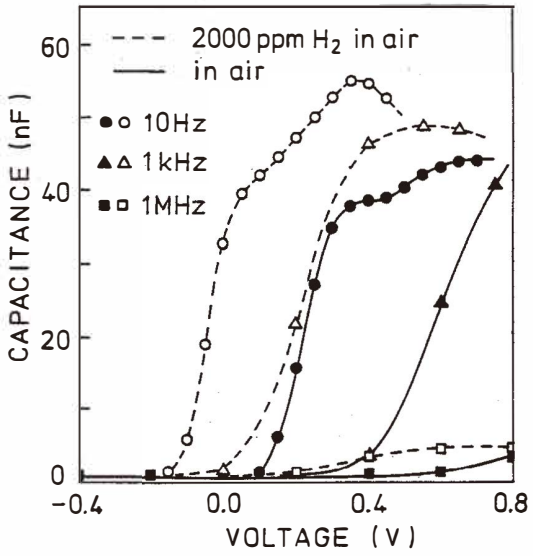

Fig. 1. C-V curves for the Pd/SiO_2/n-Si diode.

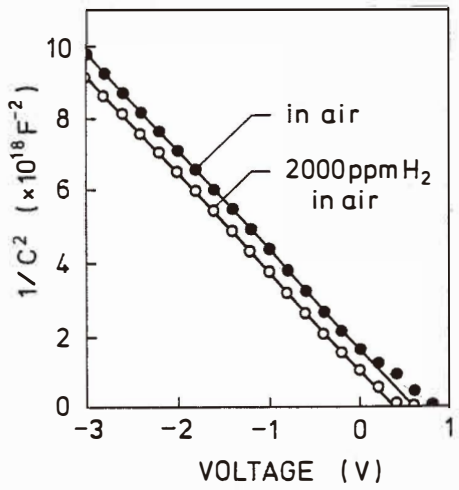

Fig. 2. $1/C^2$-V curves for the Pd/SiO_2/n-Si diode measured at 1 MHz.

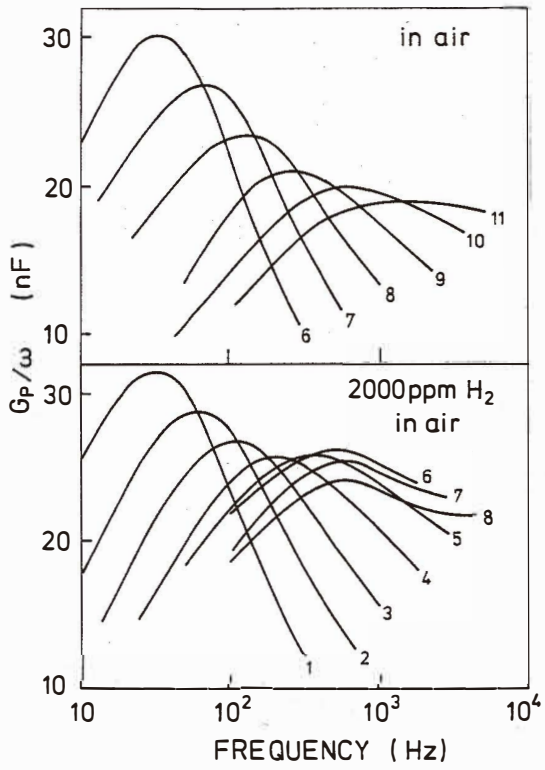

Fig. 3. G_p/ω-f curves. The number n designated in the figure shows that the Pd/SiO_2/n-Si diode is under forward bias of $0.05(n+1)$ [V].

broader than for the diode exposed to room air if the two peaks are compared under the same band bending: hydrogen absorption causes additional charge fluctuation.

Figure 4 shows an interface trap density distribution throughout the silicon band gap, which is obtained from the *C-V* curve at 10 Hz shown in Fig. 1. The energy position of the Fermi level at the interface under flat-band condition is designated by "F.B." in the figure. There is an obvious increase ΔD_{it} in the interface trap density due to hydrogen absorption. The values of ΔD_{it} thus obtained and those estimated from the G_p/ω -f curve are plotted in Fig. 5. Both capacitance and conductance methods give us the same hydrogen-induced trap interface density peak of 5×10^{12} $cm^{-2}eV^{-1}$ located at 0.63 eV above the valence band edge of silicon. Other diode samples showed trap distribution peaking at $E = 0.58 - 0.64$ eV. This scattering of the energy position is likely due to error in band bending measurement. A trap density peak was observed at $E = 0.45$ eV using the capacitance method. However, this subpeak was not detected using the conductance method: an effect of minority carriers on the conductance makes it difficult to extract D_{it} below midgap.[7] The calculated electron capture cross section of the trap located at $E = 0.63$ eV is 3×10^{-12} cm^2, using the G_p/ω -f curve shown in Fig. 3 and the mean value of the thermal velocity of electrons (1×10^7 cm/s).

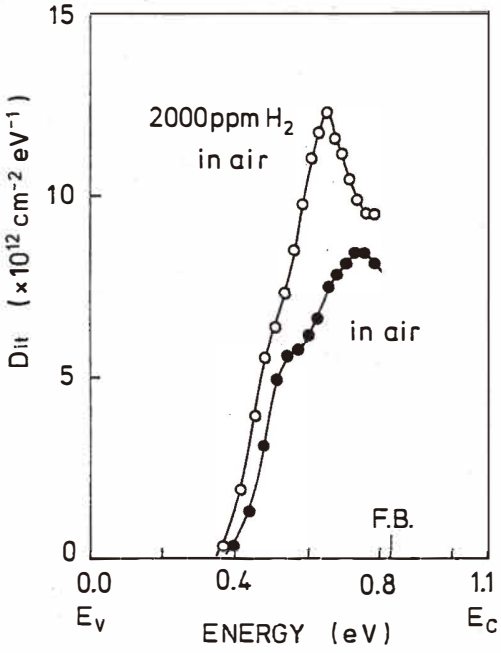

Fig. 4. Interface trap density estimated from the low-frequency (10 Hz) capacitance which is shown in Fig. 1.

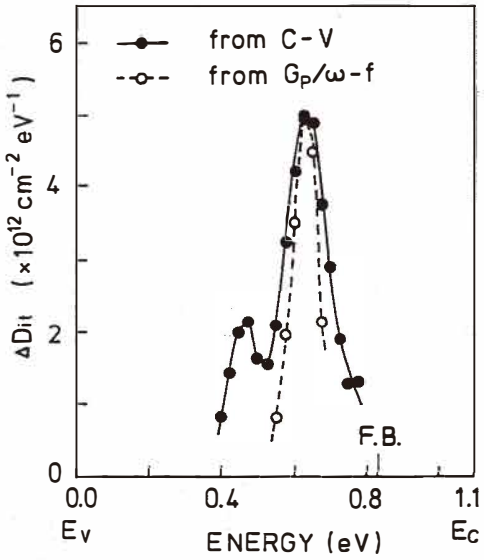

Fig. 5. Increment of the interface trap density in the Pd/SiO_2/n-Si diode on exposure to hydrogen-containing air.

Figure 6 shows the *C-V* curve for the Pd MOS diode prepared on p-type silicon. The capacitance decreases on exposure to hydrogen containing air: this is due to an increase of 0.25 V in silicon band bending which is deduced from the $1/C^2$-*V* curves measured at 1 MHz. Figure 7 shows the hydrogen-induced interface trap density ΔD_{it} estimated from the 10 Hz *C-V* curves. A trap distribution which exhibits a peak at $E = 0.60$ eV corresponds to the previous one at $E = 0.63$ eV (see Fig. 5). On the other hand, a shoulder observed at $E = 0.4 - 0.5$ eV in the curve of Fig. 7 corresponds to the previous subpeak.

Figure 8 shows D_{it} measured in dry air and room air at 65% relative humidity. The measured value of D_{it} is lower in dry air than in room air. The maximum increment of the trap density observed at $E = 0.70$ eV in room air is therefore considered to be due to water vapor.

4. Discussion

Keramati and Zemel showed that hydrogen-induced donor-type interface traps are located at 0.45 and 0.7 eV above the valence band edge E_v.[4] Petty observed hydrogen-induced electron traps 0.6 and 0.94 above E_v with capture cross sections of 10^{-15} cm^2 and 10^{-19} cm^2, respectively.[5] The interface trap density distribution which has a peak at $E = 0.63$ eV as shown in Fig. 5, is most likely assigned to the first electron traps observed by Petty, while that at $E = 0.45$ eV is most likely assigned to the first traps observed by

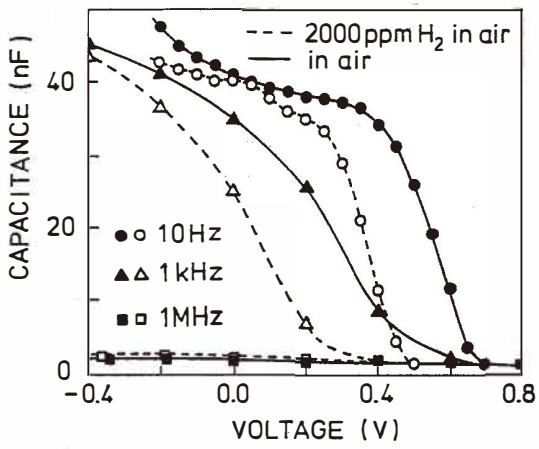

Fig. 6. *C-V* curves for the Pd/SiO_2/p-Si diode.

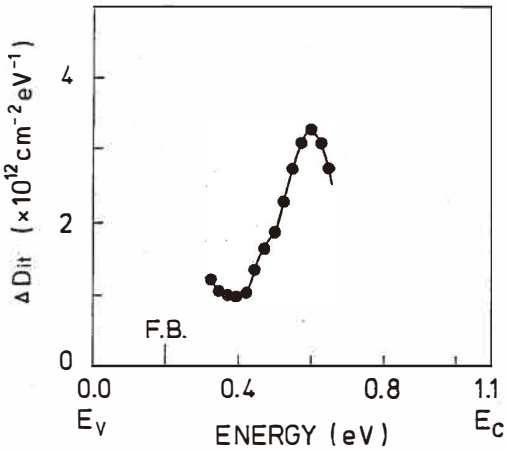

Fig. 7. Increment of the interface trap density in the Pd/SiO_2/p-Si diode on exposure to hydrogen-containing air.

Keramati and Zemel. The disagreement between the hydrogen-induced trap energy levels reported by the authors is probably due to differences in oxide growth methods.

The change of about 0.2 V in the built-in potential can be attributed to a decrease in the Pd work function as follows. We have fabricated a Pd MOS capacitor in which the oxide is too thick for hydrogen to penetrate. The shift of the *C-V* curve for this capacitor on exposure to air containing 2,000 ppm H_2 was 0.25 V, corresponding to the above value.

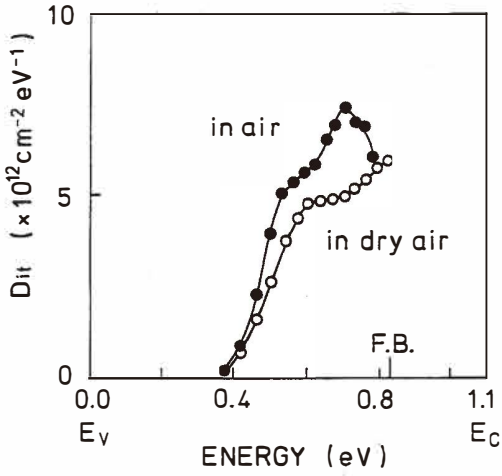

Fig. 8. Interface trap density measured in dry air and in room air at 65% relative humidity.

Nylander *et al.*[8] ascribed the shift of 0.2 – 0.3 V to a decrease in the Pd work function.

The origin of the observed hydrogen-induced traps can be explained in terms of the following chemical reaction at the SiO_2-Si interface.

$$\equiv Si - O - Si \equiv + H \rightarrow \equiv Si\bullet + HO - Si \equiv \quad (6)$$

Chemically active hydrogen atoms formed in the Pd can penetrate the very thin oxide and reach the interface to reduce the weakly bonded Si–O. The interface traps probably originate in the SiOH groups and the silicon dangling bonds ≡Si• thus formed. When hydrogen is removed from the ambient, the reverse reaction of eq. (6) occurs, causing a reversible decrease in the interface trap density. Laughlin *et al.*[9] together with Sakurai and Sugano[10] theoretically showed that the interface states due to silicon dangling bonds can be energetically located near the midgap of silicon.

The effect of water vapor on the interface trap density can be explained by water-related traps that were found in MOS capacitors by Nicollian *et al.*[11] Water is probably able to penetrate the very thin oxide layer and form SiOH groups at the interface even at room temperature.

In summary, hydrogen sensitivity in room ambient of the Pd MOS diode, which consists of a very thin interfacial oxide, was investigated using capacitance and conductance methods. The change in the built-in potential of the diode was about 0.2 V on exposure to room air containing 2000 ppm H_2. This value could be attributed to a decrease in the Pd work function. Simultaneously, an increase in the interface trap density was observed at 0.6 eV and 0.4 – 0.5 eV above the silicon valence band edge. Water vapor also had an effect of increasing the interface state density. Origins of the interface traps were

discussed in terms of chemical bonds modified by the dissociatively adsorbed gases at the SiO_2-Si interface.

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