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Micromachined Hot Plate Test Structures to Measure the Heat Capacity of CMOS IC Thin Films

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We report on new microstructures to measure the heat capacity of complementary metal oxide semiconductor (CMOS) integrated circuit (IC) thin films and layer sandwiches. The test structures were fabricated using a commercial single-poly, double-metal 1 μm CMOS process followed by silicon bulk micromachining. They consist of laterally supported plates composed of CMOS dielectrics and metal layers. The structures contain an integrated gate polysilicon resistor used simultaneously as a heater and a thermistor. Time constants of structures with different layer compositions were determined. From these, average heat capacities of various CMOS layer sandwiches and individual CMOS thin films were extracted. At 300 K, average volumetric heat capacities of 2.55 ± 0.30 MJ m^{-3} K^{-1} and 2.45 ± 0.19 MJ m^{-3} K^{-1} were found for lower and upper CMOS metals, respectively. The sandwich of CMOS oxides, including the resistor, and the silicon oxynitride passivation have respective heat capacities of 1.72 ± 0.21 MJ m^{-3} K^{-1} and 2.62 ± 0.23 MJ m^{-3} K^{-1}.

1. Introduction

The heat capacity (HC) of CMOS thin films determines the response of thermal microtransducers and thermomechanical stresses in IC devices. The low-frequency cutoff of thermal converters[1] and the high-frequency cutoff of CMOS infrared detectors[2] depend on the HC of sandwiches of CMOS dielectrics and integrated polysilicon/metal thermopiles. The efficiency of thermally excited IC-process based microresonators[3] and the sensitivity of resonant CMOS vacuum microgauges and chemical sensors are affected

by thin film HCs.

Although the number of reports on thermal conductivities of IC layers has been increasing,[4–6] very few data are available on their HCs. The reason, no doubt, lies in the difficulty in determining this property. Delicate calorimetric measurements are required before reliable HC data are obtained. If a thin film is deposited on a bulk substrate, thermal effects due to its HC are easily obscured by the bulk response. With thin film samples, on the other hand, the task is complicated by the importance of radiative energy losses caused by the large surface-to-volume ratio. Quantification of these radiative terms is delicate.

Silicon bulk micromachining has provided ways to acquire HC values of thin films using thermal microstructures. The thermal diffusivities of polysilicon and silicon-rich silicon nitride films were determined using microbridges.[7] The HC of a silicon nitride/ silicon oxide membrane was measured.[8] A calorimeter that measures the HC of thin films down to 1.5 K is based on an amorphous silicon nitride membrane.[9] Three methods for the measurement of the HC of standard CMOS IC materials were recently reported.[10–12] The first is based on uniformly heated microbridges, similar to the structures in ref. 7. The other two use cantilever beams made of CMOS dielectrics with integrated CMOS gate polysilicon heaters and resistive[11] or thermoelectric[12] temperature measurements. However, none of these microcalorimeters provided reliable data for CMOS metallizations.

In addition to the HCs of sandwiches of dielectric CMOS layers, the new micro test structures reported here allow the acquisition of such data for CMOS metal layers with higher accuracy than achieved previously. Thanks to their uncomplicated geometry, they can be described by a simple thermal model. This enables a straightforward extraction of HCs. The calorimetric measurements rely on the well-established 3ω method.[13]

In this paper, heat capacity refers to the volumetric HC in units of J m^{-3} K^{-1}. This must be distinguished from the specific heat of a material (sometimes termed heat capacity in the literature), in units of J kg^{-1} K^{-1}, which yields the present volumetric HC upon multiplication with the density. A volume-referred definition of HC is preferred since the densities of IC thin films depend on the fabrication process and are usually not known with sufficient accuracy.

2. Fabrication and Measurement Principle

A top view and cross section of the new microcalorimeters are schematically shown in Figs. 1(a) and 1(b), respectively. An SEM micrograph of a device is shown in Fig. 2. The devices were fabricated using the standard single-poly, double-metal 1 μm medium voltage ASIC CMOS process of EM Microelectronic-Marin SA (EM), Marin, Switzerland. They consist of a laterally supported 102-μm-wide and 172-μm-long rectangular plate composed of the sandwich of dielectric CMOS layers including the field, contact, and via oxides, and the passivation. Components made of the conducting IC thin films are integrated in between. These are the degenerately n-doped polysilicon and the two metal layers. Table 1 lists layer thicknesses determined by SEM analysis of device cross sections. The plate is supported by two 11-μm-wide arms of length $L = 92$ μm, consisting of the dielectric sandwich. A polysilicon resistor with a sheet resistance of 31.5 ± 0.4 Ω

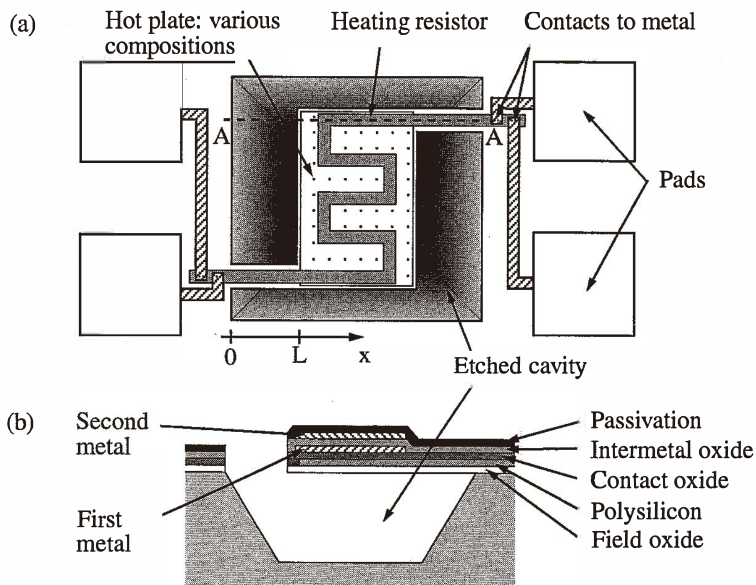

Fig. 1. Schematic (a) top view of the microcalorimeters and (b) cross section along line A-A.

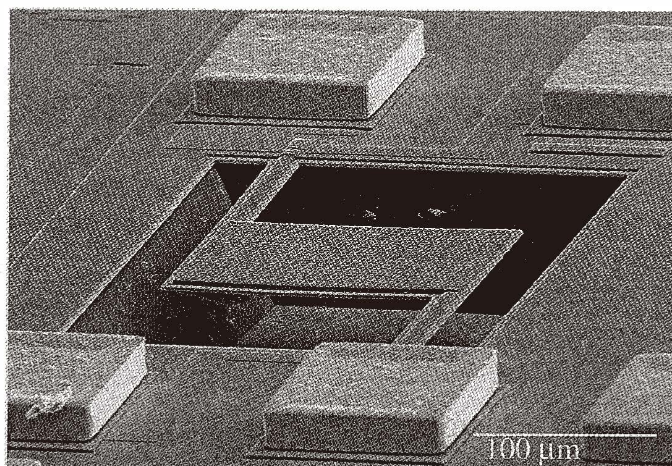

Fig. 2. SEM micrograph of a hot plate microcalorimeter (type 1).

Table 1
Thin film materials of the microcalorimeter hot plates, layer thicknesses, composition of different structures, and respective thin film volumes in the plates.

Material	Thickness [μm]	Structure type					Volume [10^3 μm^3]
		1	2	3	4	5	
Polysilicon	0.367 ± 0.012	×	×	×	×	×	3.52 ± 0.12
First metal	0.728 ± 0.023					×	4.37 ± 0.14
				×	×		11.0 ± 0.3
Second metal	1.23 ± 0.039	×	×				18.4 ± 0.6
					×		17.1 ± 0.5
Passivation	1.50 ± 0.11	×		×	×	×	16.7 ± 1.2
Silicon oxides	1.89 ± 0.10	×	×	×	×	×	43.0 ± 1.9

meanders through the arms and the plate. A fraction, 3.4%, of the resistance is located in each arm (resistance R_{a0} at 300 K), while the remaining 93.2% is integrated into the plate (resistance R_{p0} at 300 K). The overall resistance $R_0 = 2R_{a0} + R_{p0}$ of the polysilicon resistor at 300 K is about 21 kΩ. The resistor has two functions: it heats the structure and simultaneously enables monitoring of the thermal response. It is contacted in a four-point probe configuration, enabling accurate determination of resistance changes and, thus, temperature variations.

The devices were designed using the CADENCE design framework II and fabricated through the wafer service of EM. The microstructures were obtained after completion of the CMOS process by anisotropic silicon micromachining. To prevent etching of the sample back surfaces, 170 nm of SiO_2 were deposited on the rear surface of the wafers by PECVD. After a BOE dip, samples were etched in an S-type EDP solution[14] at 95°C for 2 h. This maskless post-processing was made possible by appropriate openings in all dielectrics, defined by the superposition of corresponding mask layers. Such mask superposition has no equivalent in IC design and violates several CMOS design rules. However, the violations do not jeopardize the CMOS process and integrated circuits fabricated concurrently operate as expected. Finally, the dice were attached and wire-bonded to DIL-28 substrates.

Five structures with different plate compositions were fabricated. Comparison of pairs of such devices differing by a single layer allows the extraction of the HCs of individual layers. Table 1 shows the various plate compositions. In the structures of types 1 to 4, rectangles of the first and/or second CMOS metal, with respective sizes of 92 μm by 162 μm and 88 μm by 158 μm, were integrated into the plate. The structures of type 5 contains a lower metal rectangle (92 μm by 162 μm) with two 30-μm-wide and 138-μm-long

openings. In type 2 structures, the passivation was removed over a 88 μm by 158 μm wide area. All structures have at least one partial metallization for temperature homogenization over the plate. Material volumes as determined from SEM cross sections and layout dimensions, including uncertainty estimates, are listed in Table 1. The composition of the arms is the same for all structures. They consist of the complete dielectric sandwich and the polysilicon resistor.

Thermal properties at 300 K were extracted from the thermal responses of the devices to static and dynamic heat dissipation. In the static case, a dc current I_{dc} dissipates a power $P_{dc} = R_0 I_{dc}^2$ in the structure. The device then undergoes an average temperature increase $\overline{T_{dc}} \sim I_{dc}^2$ along the polysilicon meander. To the first order in $\overline{T_{dc}}$, the resistance of the heater varies as

$$R(\overline{T_{dc}}) = R_0 \cdot (1 + \beta \overline{T_{dc}}), \quad (1)$$

where $\beta = R^{-1} dR/dT$ denotes its linear temperature coefficient of resistance at 300 K. Strictly speaking, the temperature increase of the resistor leads to a second contribution to P_{dc} proportional to I^4. However, under the experimental conditions described in section 5, this term is smaller than 1% and will be neglected. In view of the temperature dependence of the polysilicon resistance, the voltage drop U_{dc} (I_{dc}) over the resistor is of the form

$$U_{dc}(I_{dc}) = R_0 I_{dc} + U_{dc3}(I_{dc}). \quad (2)$$

The first term on the right-hand side is the ohmic term $R_0 I_{dc}$, while U_{dc3} results from the temperature increase of the structure under I_{dc}. This contribution is proportional to I_{dc}^3 and depends on the thermal loss mechanisms of the device. In consequence, these mechanisms can be characterized by dc electrical measurements.

In the dynamic case, an ac current $I_{ac}\cos(\omega t)$ with amplitude I_{ac} and angular frequency ω is applied to the polysilicon resistor. The power $P_{ac}(t) = R_0 I_{ac}^2 (1 + \cos(2\omega t)) / 2$ dissipated in the structure consists of a static term and a dynamic component at the second harmonic frequency. Likewise, the resulting average temperature increase $\overline{T_{ac}}(t)$ along the resistor contains a static and a dynamic component, viz.,

$$\overline{T_{ac}}(t) = \overline{T_{ac0}} + \overline{T_{ac2}}(\omega) \cos(2\omega t - \phi(\omega)). \quad (3)$$

The 2ω component has a frequency-dependent amplitude $\overline{T_{ac2}}(\omega)$ and phase $\phi(\omega)$. Both depend on the heat loss mechanisms and the average HC of the plate. To the first order in $\overline{T_{ac}}(t)$, the heater resistance varies as

$$R(t) = R_0 \{1 + \beta \overline{T_{ac}}(t)\}. \quad (4)$$

Therefore, similarly to the static case, the temperature-dependence of R leads to a second 2ω contribution to $P_{ac}(t)$, which, however, is again smaller than 1%. In consequence, the time-dependent voltage $U(t) = R(t)I_{ac}\cos(\omega t)$ over the resistor contains the third harmonic component

$$U_{ac3}(t) = \frac{1}{2} R_0 I_{ac} \beta \overline{T_{ac2}}(\omega) \cos(3\omega t - \phi(\omega)). \tag{5}$$

The average HC of the plate is extracted from the ω-dependent amplitude of $U_{ac3}(t)$, using the model developed in the next section. A similar method has been used to determine the thermal conductivity of amorphous solids.[13]

3. Thermal Model

The supporting arms are characterized by the thermal conductance $K = \sum \kappa_i a_i$, where the summation includes all component layers of the arms, and κ_i and a_i denote the thermal conductivities and cross-sectional areas, respectively, of the individual layers. Considering the small volumes and surface areas of the arms compared with those of the plates, the HC and radiative heat loss of the arms are neglected. The time-dependent temperature on the arms, $T_a(x,t)$, is assumed to depend on the coordinate x (defined in Fig. 1(a)) only and to be constant on cross sections perpendicular to the arms. With these simplifications, $T_a(x,t)$ solves the heat conduction equation

$$K \frac{\partial^2}{\partial x^2} T_a(x,t) = -\frac{P_a(t)}{L}, \tag{6}$$

where P_a denotes the power dissipated in the arms.

In view of the homogenizing metal layers, the temperature $T_p(t)$ on a plate is assumed to be constant over the plate. The heat capacitance C of the plate is defined as $C = \sum c_k v_k$, where c_k and v_k denote the volumetric heat capacities and volumes of the component materials, respectively. With the total plate volume $V = \sum v_k$, the volume-averaged HC of the plate is $c = C/V$. Heat is dissipated in the plate at a rate $P_p(t)$ and is eliminated by heat conduction through the arms and by thermal radiation. Energy conservation therefore implies that

$$C \frac{\partial}{\partial t} T_p(t) = P_p(t) - 2K \frac{\partial}{\partial x} T_a(x,t) \bigg|_{x=L} - \frac{K_{rad}}{L} T_p(t). \tag{7}$$

The final term on the right-hand side summarizes thermal radiation losses, using the phenomenological thermal parameter K_{rad}. Conductive heat losses through the surrounding

gas are minimized by performing measurements in vacuo. Boundary conditions (BCs) to be fulfilled by T_a and T_p are $T_a(L,t) = T_p(t)$ and $T_a(0,t) = 0$.

3.1 *Static case*

Heating powers dissipated in each arm and in the plate are $P_a = R_{a0}I_{dc}^2$ and $P_p = R_{p0}I_{dc}^2$, respectively. Small contributions to P_a and P_p due to the temperature-dependence of the resistances R_a and R_p are neglected here, being smaller than 1% under typical experimental conditions. The temperature profile along the polysilicon resistor is obtained by solving eqs. (6) and (7) under the appropriate BCs. Averaging over the length of the resistor provides the mean temperature

$$\overline{T_{dc}} = \frac{(R_0')^2(1+\varepsilon)L}{R_0(2K+K_{rad})} I_{dc}^2, \tag{8}$$

where $R_0' = R_{a0} + R_{p0}$ denotes the thermally relevant resistance and

$$\varepsilon = \frac{R_{a0}^2(2K + K_{rad})}{6R_0^2K}. \tag{9}$$

The parameter ε is of the order of 10^{-4} and is thus neglected. In consequence, the voltage U_{dc} over the resistor is well approximated by

$$U_{dc}(I_{dc}) = R_0I_{dc} + \frac{(R_0')^2 L\beta}{2K + K_{rad}} I_{dc}^3. \tag{10}$$

Thus, by (i) measuring the overall resistance R_0, (ii) deducing R_0' from this result using the design dimensions ($R_0' = 0.966R_0$), (iii) measuring β, and (iv) measuring the dependence $U_{dc}(I_{dc})$, the relevant thermal conductance $2K + K_{rad}$ of the device can be extracted.

3.2 *Dynamic case*

The 2ω components of the power dissipated in the arms and the plate are $P_a(t) = R_{a0}I^2\cos(2\omega t)/2$ and $P_p(t) = R_{p0}I^2\cos(2\omega t)/2$, respectively. Again, by solving eqs. (6) and (7), temperatures $T_a(x,t)$ and $T_p(t)$, amplitude $\overline{T_{ac2}}(\omega)$ and phase $\phi(\omega)$ are obtained. These are

$$\overline{T_{ac2}}(\omega) = \frac{1}{2}\frac{(R_0')^2 L}{R_0(2K+K_{rad})}\sqrt{\varepsilon^2 + \frac{1+2\varepsilon}{1+(\omega\tau)^2}} I_{ac}^2 \tag{11}$$

and

$$\phi(\omega) = \mathrm{atan}\left(\frac{\omega\tau}{1+\varepsilon(1+(\omega\tau)^2)}\right) \quad (12)$$

with the thermal time constant

$$\tau = \frac{2CL}{2K + K_{rad}}. \quad (13)$$

The influence of the parameter ε on $\overline{T_{ac2}}$ and ϕ is small at low frequencies. However, it increases with increasing ω. Time constants of the plates τ are roughly 0.2 s. At the maximum experimental angular frequency of 38 s^{-1}, therefore, the omission of ε introduces respective errors of 0.03% and 2% in $\overline{T_{ac2}}$ and ϕ.

Neglecting ε, the third harmonic component $U_{ac3}(t)$ of the measured dynamic voltage over the resistor is then well approximated by $A(\omega)\cos(3\omega t - \phi(\omega))$ with amplitude

$$A(\omega) = \frac{U_0}{\sqrt{1+(\tau\omega)^2}}, \quad (14)$$

where U_0 is given by

$$U_0 = \frac{(R_0')^2 L\beta}{4(2K + K_{rad})} I_{ac}^3. \quad (15)$$

From the measured frequency-dependent amplitude and phase of U_{ac3}, therefore, the thermal time constant τ of the structure and the heat capacitance of the plate can be extracted. All other parameters are independently determined. In view of its smaller error upon neglect of ε, $A(\omega)$ is preferred over $\phi(\omega)$ for the extraction of C.

Finally, a pair of structures with heat capacitances C_1 and C_2, differing in plate composition by a single thin film of volume v_{layer} is considered. In view of the additive definition of C, the volumetric HC of this thin film material, c_{layer}, is given by

$$c_{layer} = \frac{C_2 - C_1}{v_{layer}}. \quad (16)$$

The underlying assumptions of the model were checked by static and harmonic[15] thermal finite-element (FE) analysis, using the microsystem simulation package SOLIDIS.[16]

As input parameters for the model we used (i) independently measured thermal conductivities,[4,5] resistivities and temperature coefficients of resistance,[6] (ii) assumed HC values of 1.77 MJ m^{-3} K^{-1}, 1.67 MJ m^{-3} K^{-1}, and 2.37 MJ m^{-3} K^{-1} for the dielectrics, polysilicon, and first metal, respectively, and (iii) dimensions of the layout. The simulations showed that the plate temperatures are highly homogeneous; in the relevant range of angular frequencies from 3.1 to 37.7 s^{-1}, the temperature amplitude and phase typically vary by less than 0.1% and 0.02% over the entire plate. This shows that the metal layers integrated in the test structures are extremely efficient temperature homogenizers. The temperature profile along the suspension arm is highly linear. Effects due to the HC of the arms are small.

A final test of the model was performed as follows. An assumed plate heat capacitance C_{in} was fed into the FE model. The relevant thermal conductance of the structure was obtained numerically under dc heating conditions. Next, the amplitude of the mean ac temperature response along the resistor was simulated as a function of ω; finally, the model expression of eq. (14) was fitted to the simulated response and a heat capacitance value C_{out} was extracted. The extracted value agreed with C_{in} within 1.82%. It is concluded that this is the typical uncertainty of extracted C values resulting from model simplifications.

The influence of thermomechanical effects on the measurements is discussed now. When heated, the micro hot plate deforms due to thermal expansion of the individual layers. This results in a deformation of the temperature-monitoring polysilicon resistor and causes a piezoresistive change in the resistance value. To the first order, this is proportional to the temperature change of the hot plate. Thus, the effective temperature coefficient of resistance β of the resistor is the result of two effects: the intrinsic temperature dependence of the polysilicon resistance and the thermomechanical effect. The second effect is estimated to contribute roughly 10% to β, which is not negligible. However, as explained in Section 5 below, the method with which β is determined enables measurement of the required effective temperature coefficient of resistance, including the thermomechanical contribution.

4. Experimental

The structures were characterized in vacuo. The DIL-28 packages were mounted on a pedestal that can be cooled by liquid nitrogen and heated by a resistor. This allowed stabilization of the chips at preset temperatures. Measurements at these temperatures were used for the determination of β of the polysilicon resistors/thermistors. The chip temperature was controlled with a calibrated silicon diode temperature sensor integrated in the pedestal and an external PID temperature controller. At the cryostat base pressure of 10^{-6} mbar, conductive and convective heat losses through the surrounding gas were negligible.

A set of three different measurements was performed on up to three devices of each type. First, β of the polysilicon resistor of each sample was determined. Next the microcalorimeters were characterized under static heating powers, which provided the effective heat conductance $2K + K_{rad}$. Finally, the structures were characterized under dynamic conditions, which allowed extraction of their heat capacitance C. The experimen-

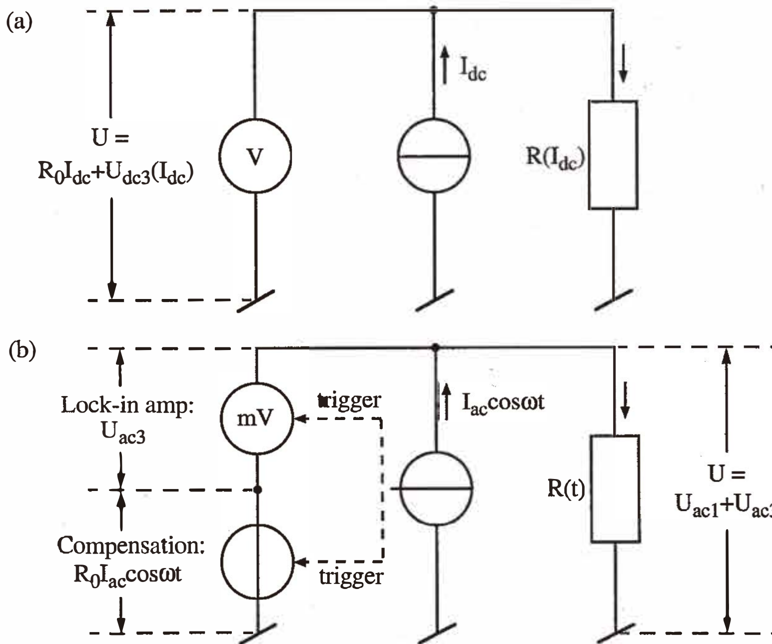

Fig. 3. Schematic experimental setups for (a) dc and (b) ac characterization of hot plate microcalorimeters.

tal setups for static and dynamic measurements are shown in Fig. 3. For dc measurements (Fig. 3(a)), a dc current I_{dc} was applied to the resistors in the samples by a universal source *HP 3245A*, and the voltage drop over the resistors was measured by a multimeter *HP 34401A*. This measurement was performed for a range of currents. For ac measurements (Fig. 3(b)), harmonic currents of various angular frequencies ω were applied to the samples. The voltage drop over the resistor, $U(t) = U_{ac1}(t) + U_{ac3}(t)$, has components U_{ac1} and U_{ac3} at angular frequencies ω and 3ω, respectively. Voltage U_{ac3} was measured with a lock-in amplifier *EG&G PARC 5302*. This was connected in series with the second source channel providing the synchronized voltage $R_0 I_{ac} \cos \omega t$ used to compensate most of U_{ac1}.

5. Results

The coefficient β of each resistor was determined using

$$\beta(T_0) = \frac{R_{20} - R_{-20}}{R_0 \cdot (T_{20} - T_{-20})} \tag{17}$$

by measuring the respective resistance values $R_{-20} = R(T_{-20})$, $R_0 = R(T_0)$, and $R_{20} = R(T_{20})$, with $T_{-20} = 280$ K, $T_0 = 300$ K, and $T_{20} = 320$ K. Experimental β values are listed in Table 2. Their average is 7.36×10^{-4} K^{-1}. Note that the resistance values R_{-20}, R_0, and R_{20} include the intrinsic change of the resistor with temperature and the piezoresistive change due to the temperature-dependent deformation of the hot plate structure. As a consequence, β determined by this method includes both effects required for accurate temperature monitoring on the hot plate.

Static measurements were performed at T_0. The voltage U_{dc} was recorded for $-36\ \mu A \leq I_{dc} \leq 36\ \mu A$. A cubic polynomial, $U_{dc} = R_0 I_{dc} + R_3 I_{dc}^3$, with fitting coefficients R_0 and R_3 was fitted to the experimental results. Examples of such results for different structures with corresponding fits are shown in Fig. 4. Table 2 shows the optimal resistance R_0 for all structures. A variance of 1.3% of all R_0 values is typical of commercial CMOS processes. Finally, the effective thermal conductance $2K + K_{rad}$ of each microcalorimeter was obtained from R_3 using eq. (10), and the results are shown in Table 2. On all structure types except the type 2 structures, the plates are covered by the standard CMOS oxynitride passivation. The effective thermal conductance $2K + K_{rad}$ of structures without passivation is 234 ± 3 pW m K^{-1}. All others have $2K + K_{rad} = 243 \pm 8$ pW m K^{-1}. This difference may be explained by the lower emissivity of the CMOS metallization compared with silicon oxynitride, for thermal radiation at 300 K, at wavelengths between 8 and 20 μm.

Table 2
Linear temperature coefficient of resistance β and resistance R_0 of heating resistors, effective thermal conductance $2K + K_{rad}$, thermal time constant τ, total heat capacitance C, and average volumetric heat capacity c of the plates of all characterized samples.

Structure type	β [10^{-3}K^{-1}]	R_0 [kΩ]	$2K + K_{rad}$ [10^{-10} WmK^{-1}]	τ [s]	C [μJK^{-1}]	c [MJm^{-3}K^{-1}]
1	0.726	21.37	2.414	0.139	0.168	2.054
	0.733	20.59	2.364	0.143	0.170	2.077
2	0.744	21.39	2.361	0.104	0.123	1.895
	0.755	20.64	2.313	0.109	0.127	1.951
3	0.727	20.92	2.410	0.127	0.153	2.061
	0.728	21.05	2.376	0.129	0.153	2.066
	0.725	21.21	2.512	0.124	0.157	2.097
4	0.708	21.20	2.587	0.151	0.196	2.144
5	0.753	20.83	2.378	0.116	0.138	2.036
	0.752	20.94	2.373	0.115	0.136	2.015
	0.749	21.10	2.481	0.111	0.138	2.046

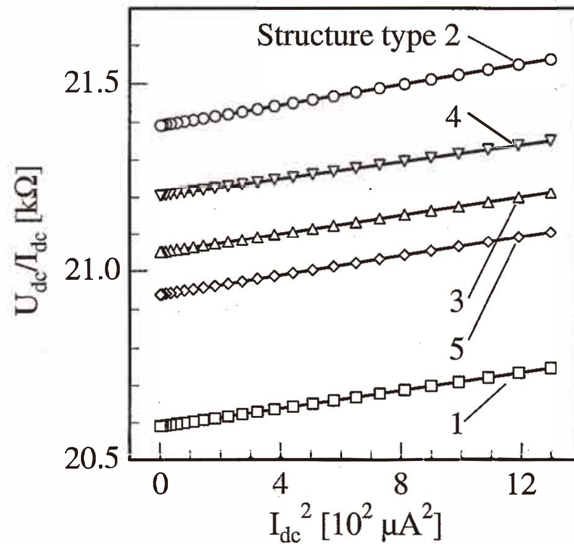

Fig. 4. Apparent resistance U_{dc}/I_{dc} of heating resistor of different types of microcalorimeters as a function of current I_{dc}. Solid lines are optimum fitting curves obtained using eq. (10).

For the dynamical characterization of the structures, ac currents with $I_{ac} = 36$ μA and ω between 0.6 s^{-1} and 37.7 s^{-1} were applied to the resistors. Time-averaged powers of about 13 μW were thus dissipated and temperature increases of the microcalorimeters remained below 10 K. The ω-dependent amplitude of the voltage signal $U_{ac3}(t)$ was roughly 3000 times smaller than the linear resistive voltage component at angular frequency ω. The third harmonic component of the compensation signal $R_0 I_{ac} \cos\omega t$ was smaller than 9 μV, compared with typical amplitudes of 1 mV of $U_{ac3}(t)$. Frequency-dependent measured amplitudes $A(\omega)$ of $U_{ac3}(t)$ of different structures are shown in Fig. 5. Similar data were obtained for all samples and fitted with the model expression of eq. (14). This provided the time constants τ and, using eq. (13), the individual heat capacitances C of the microcalorimeters. Experimental τ values are listed in Table 2 for all samples investigated. Average time constants are 0.141 s, 0.107 s, 0.127 s, 0.151 s, and 0.114 s for the structures of types 1 to 5, respectively. Table 2 also shows extracted C values for all structures. The averages of C for structures of types 1 to 5 are 0.169 μJ K^{-1}, 0.125 μJ K^{-1}, 0.154 μJ K^{-1}, 0.196 μJ K^{-1}, and 0.137 μJ K^{-1}, respectively. The structure of type 4 has the largest C value; it contains all CMOS dielectrics and both metal layers. Division of C data by appropriate plate volumes provided the average volumetric HC c of the plates of all samples, as shown in Table 2. Averages are 2.065 MJ m^{-3} K^{-1}, 1.923 MJ m^{-3} K^{-1}, 2.075 MJ m^{-3} K^{-1}, 2.144 MJ m^{-3} K^{-1}, and 2.032 MJ m^{-3} K^{-1} for the structures of types 1 to 5, respectively.

By subtraction according to eq. (16), the volumetric HCs of both metallizations and the

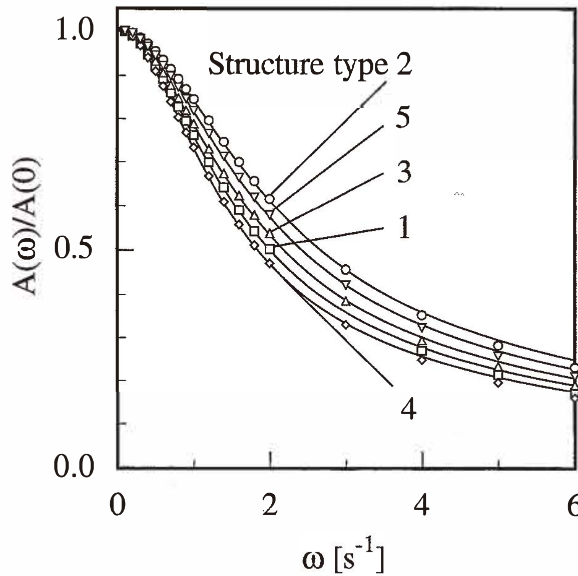

Fig. 5. Normalized amplitude of $U_{ac3}(t)$ versus angular frequency ω for microcalorimeters of different types. Solid lines are optimum fitting curves obtained using eq. (14).

passivation were obtained. Nine combinations of structures of types 3 and 5 provided an HC $c = 2.51 \pm 0.24$ MJ m^{-3} K^{-1} of the lower CMOS metal. For the second metal, using structures of types 3 and 4, a c of 2.44 ± 0.12 MJ m^{-3} K^{-1} was obtained. Using this value, a second heat capacity $c = 2.77 \pm 0.16$ MJ m^{-3} K^{-1} was extracted for the lower CMOS metal with structures of types 1 and 4. From the two independent values for the lower metal, an average $c = 2.56 \pm 0.24$ MJ m^{-3} K^{-1} was obtained for this layer. For the passivation, $c = 2.62 \pm 0.24$ MJ m^{-3} K^{-1} was obtained with structures of types 1 and 2. If the contribution of the second CMOS metal is subtracted from the structures of type 1, an average c value of 1.95 ± 0.12 MJ m^{-3} K^{-1} is deduced for the complete sandwich of CMOS dielectrics including the oxynitride passivation, with an integrated polysilicon resistor. Similarly, $c = 1.72 \pm 0.15$ MJ m^{-3} K^{-1} was obtained for the silicon oxides with integrated resistor, by eliminating the metal contribution from the results of type 2 structures. The uncertainties in the above c values result from the standard deviation of the experimental C values (in Table 2), the uncertainties of the measured layer volumes (in Table 1), and the subtraction procedure. The results and extraction method for component layers and sandwiches are summarized in Table 3.

Within the respective experimental uncertainty ranges, the HCs extracted here for CMOS metals agree with that of bulk aluminum deduced from published data. The specific heat[17] and density[18] of Al at 300 K are 0.2164 cal g^{-1}K^{-1} and 2.7 g cm^{-3}, respectively. These result in a volumetric HC of 2.44 MJ m^{-3}K^{-1}. A HC of 2.41 MJ m^{-3}K^{-1} at

Table 3
Average heat capacities c of CMOS layers and layer sandwiches, and the methods used for their extraction.

Layer	c [MJm^{-3}K^{-1}]	Method
(a) Second metal	2.44 ± 0.12	Subtraction of type 3 from 4
(b) First metal	2.51 ± 0.24	Subtraction of type 5 from 3
(c) First metal	2.77 ± 0.16	Subtraction of type 1 from 4, using (a)
(d) First metal	2.56 ± 0.24	Weighted average of (b) and (c)
(e) Passivation	2.62 ± 0.24	Subtraction of type 2 from 1
(f) All dielectrics with polysilicon resistor	1.95 ± 0.12	Subtraction of (a) from type 1
(g) All Si oxides with polysilicon resistor	1.72 ± 0.15	Subtraction of (a) from type 2

300 K was measured for the first metal with other CMOS-compatible test structures.[19]

The comparison of HC values of amorphous materials is less conclusive, since their properties depend strongly on the fabrication process. The specific heat[17] of SiO_2 is 0.1775 cal g^{-1}K^{-1} at 300 K. With a density[18] of 2.2 g cm^{-3}, this results in a volumetric HC of 1.63 MJ m^{-3}K^{-1}. Within the experimental uncertainty, the HC for the oxide sandwich including polysilicon agrees with this value for bulk silicon dioxide.

The specific heat of bulk silicon nitride[20] (Si_3N_4) is 100.04 J mole^{-1}K^{-1} at 300 K. A volumetric HC of 2.46 MJ m^{-3} K^{-1} is obtained with an atomic mass of 139.94 g mole^{-1} and a density[18] of 3.44 g cm^{-3}. Mastrangelo *et al.*[7] measured a HC of 2.2 MJ m^{-3} K^{-1} for low-residual, silicon-rich, LPCVD Si_3N_4. Völklein[8] determined a HC of 1.68 m^{-3} K^{-1} for a layered SiO_2/Si_3N_4 system at ambient temperature. Ehlert[21] investigated the HC of the oxynitride Si_2N_2O. He extracted a specific heat value of 67.84 J mole^{-1} K^{-1} at 300 K. Previous measurements[19] with other CMOS-compatible test structures provided a HC for a CMOS dielectric sandwich of 1.71 MJ m^{-3} K^{-1} at 300 K.

6. Conclusions

We have reported on a new method to determine the heat capacities of thin film layers in CMOS sandwiches. It relies on the thermal characterization of micro hot plates composed of the investigated CMOS layers. The heat capacities of several sandwiches containing the dielectric layers, the gate polysilicon, and both metal layers of a commercial ASIC CMOS process were determined. These allowed extraction of heat capacities of both

metallizations, the passivation layer, and the oxide sandwich. Test structures such as those reported here can be easily included in other CMOS processes.

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