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CMOS Micro Electro Mechanical Systems

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This introduction to the merging of MEMS and CMOS IC technology includes a summary of current technological approaches to CMOS MEMS, illustrations by selected CMOS MEMS microtransducer prototypes and an outline of the MEMS CAD tools, SOLIDIS and ICMAT.

1. Introduction

The term MEMS (micro electro mechanical systems) originally meant miniaturized electromechanical actuators, but now applies to a broad family of micromachined sensors, actuators and systems with coupled electrical, mechanical, radiant, thermal, magnetic and chemical effects. The acronyms IC MEMS, IMEMS (or iMEMS) and CMOS MEMS refer to silicon integrated MEMS based on integrated circuit (IC) technology combined with micromachining, thin film deposition or electrodeposition.[1–11]

For example, microsensors for thermal, mechanical and chemical measurands can be made by combining established CMOS IC technologies with CMOS-compatible additional processing steps specific to the sensor function. Preferably, such extra etching or deposition steps are performed by post-processing (also called post-CMOS), i.e., after completion of the regular IC process sequence. Pre-processing (pre-CMOS) and intermediate processing (intermediate CMOS) have also been demonstrated. Technological approaches to CMOS MEMS are summarized in section 2. Examples of post-CMOS microtransducer prototypes are demonstrated in section 3, whereas section 4 is dedicated to CMOS MEMS modeling and related materials characterization.

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2. CMOS MEMS Technologies

Here is a preliminary list of CMOS-compatible MEMS technologies:

- Bulk micromachining (wet or dry, isotropic or anisotropic, from wafer front or back).
- Surface micromachining (sacrificial oxide and/or metal or polysilicon).
- Micromachining before completion of IC process (pre-processing, pre-CMOS).
- Micromachining after completion of IC process (post-processing, post-CMOS).
- Micromachining inside or outside the IC foundry.
- Use of IC materials (monocrystalline silicon, polycrystalline silicon, oxide, nitride, metal, or gold bumps) for microstructures with electro-thermo-opto-mechanical functions.
- CMOS-compatible layer deposition, chemical-mechanical polishing, and wafer bonding.

Such techniques are currently being explored by researchers at Analog Devices, UC Berkeley, Carnegie-Mellon University, Cornell University, ETH Zurich, Fraunhofer Institut Dresden, Georgia Institute of Technology, University of Michigan, MIT, NIST, Sandia, Siemens, Stanford University, and several Canadian universities.

A summary of some of these developments is attempted in the following; it mainly draws from presentations at recent meetings such as IEDM, IEEE MEMS, Solid-State Sensor and Actuator Workshop, and IEEE ISCAS. Completeness is not attempted.

2.1 *Post-CMOS micromachining*

Four different ways to combine CMOS IC technology with micromachining are illustrated by the generic microtransducer cross sections shown in Fig. 1; these include two surface (a, b) and two bulk (c, d) micromachining techniques. The CMOS-compatible surface micromachining by sacrificial oxide etching (a) and sacrificial metal etching (b) is summarized as follows.

As indicated in Fig. 1(a), CMOS polysilicon microstructures can be formed by selective removal of the CMOS dielectric layers. This technique was demonstrated recently for a 0.8 μm CMOS IC process of Siemens AG with a standard 0.35-μm-thick gate polysilicon layer serving as the seismic mass for an accelerometer and a 0.6-μm-thick field oxide serving as the sacrificial layer.[12,13] Buffered HF is used to release the seismic mass and the suspensions. Structural polysilicon with a thickness larger than that provided by the standard CMOS technology is feasible,[14] but requires interruption of the regular IC process (see section 2.3).

Figure 1(b) illustrates the CMOS-compatible sacrificial-metal surface micromachining technique.[2–5,15–17] The final structure is obtained by local removal of the lower CMOS metallization layer after completion of the IC process; this is achieved by including pad-like structures in the design layout that provide access to the metal layer to be removed. For the post-processing step, all exposed metal areas (contact pads) on the chip surface are protected with photoresist, except the access openings to the sacrificial layer. The selective removal of this metal by a commercial wet etchant results in a suspended membrane composed of the intermetal dielectric and the passivation layer, possibly with an upper metal layer sandwiched inbetween.

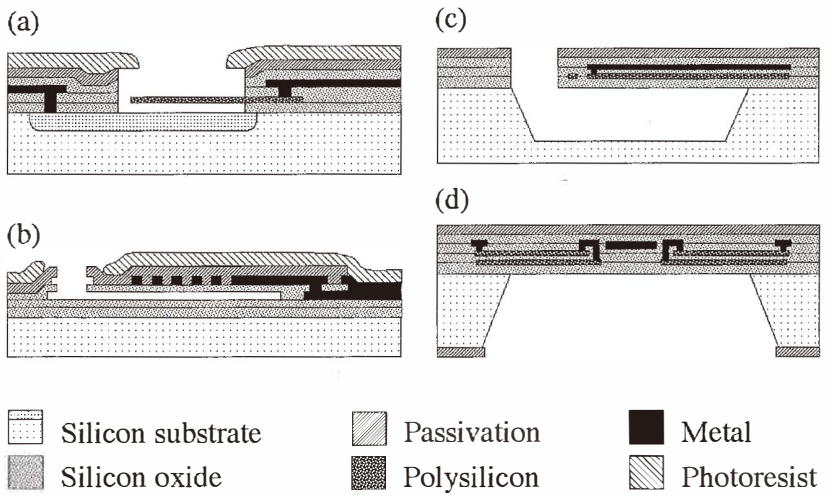

Fig. 1. Post-CMOS surface (a, b) and bulk (c, d) micromachining: sacrificial oxide etching for polysilicon microstructure (a), sacrificial metal etching for cavity structure (b), wafer front silicon etching for beam (c), and wafer back silicon etching for membrane (d).

A combination of sacrificial metal and oxide etching allows fabrication of the CMOS-based electrostatic deflectable micromirror[18,19] shown in Figs. 2 and 3. The mirrors are made from the second metallization of the CMOS process deposited in two passes. Supercritical carbon-dioxide drying after the final rinse prevents the mirror from sticking to the substrate.

The two approaches to CMOS-compatible bulk micromachining illustrated in Fig. 1 are the removal of a portion of the silicon substrate from the front (c) or the back (d) of the wafer. Inherent features of CMOS technology and the etching properties of its (100) substrate allow the fabrication of open microstructures (beams or suspended membranes) by anisotropic silicon etching from the front of the wafer.[1–5] Possible etchants are EDP or TMAH, which preserve the integrity of the bonding pads. By design, the passivation layer serves as a mask. CMOS dielectric (oxide/nitride) beams or suspended membranes supporting thermal flow sensors[20,21] or thermally actuated micromirrors[22] can be made in this way. For thermal sensors, removal of part of the silicon substrate by bulk micromachining is crucial for thermal isolation. While EDP or TMAH front etching is useful for laboratory exploration of the feasibility of new microtransducer designs, this method may be less suitable for practical application.

Closed dielectric membranes (less sensitive to dust and humidity) are formed by etching from the back of the finished CMOS wafer.[1–5,23,24] An extra mask is required to define the membrane size. The preferred etchant is KOH. The front of the wafer is protected from the etchant by a mechanical chuck or etch protection layer. Here is an

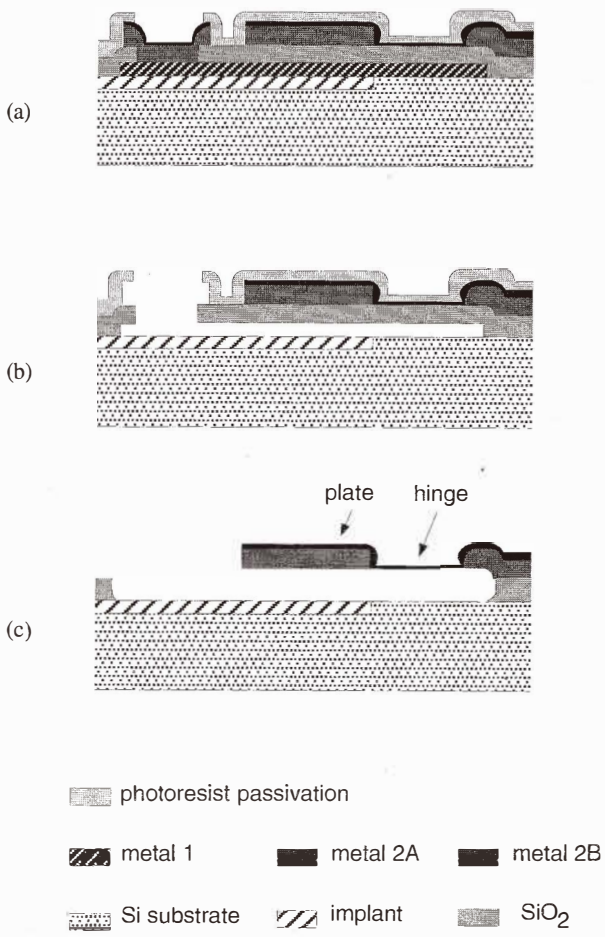

Fig. 2. Post- and intermediate-CMOS fabrication of electrostatic deflectable micromirror using combined sacrificial metal and sacrificial oxide etch and double-pass metallization: after CMOS process (a), after sacrificial aluminum etch (b), and after oxide and passivation etch (c).

example for a specific list of process steps performed subsequent to the CMOS process sequence:

- Deposition of stress-compensated passivation nitride.
- Deposition of an etch protection layer on the wafer front.
- Isotropic etching of the wafer back to achieve good adhesive conditions.
- Deposition of the back nitride mask.
- Photolithography on the wafer back.

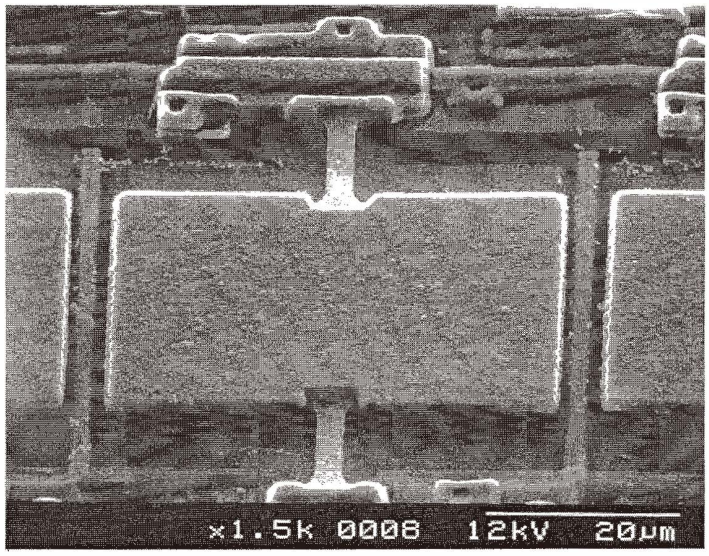

Fig. 3. SEM micrograph of electrostatically actuated CMOS-based micromirror.

- Etching in a 6 molar 95°C KOH solution.
- Dicing of the wafer.

The overall membrane yield after dicing is above 98%. Thanks to stress-controlled deposition of the silicon nitride passivation, low-stress membranes with less than 0.1 μm buckling over an area as big as 720 μm by 720 μm are feasible.[2-5,23,24] The above bulk micromachining techniques produce CMOS dielectric beams or membranes with sandwiched metal and polysilicon thin-film structures used for a variety of thermal microtransducers such as thermoelectric infrared, vacuum, power and flow sensors, or thermally actuated micromirrors (see section 3).

Four alternative CMOS-compatible micromachining techniques have been demonstrated recently, two of which include the etching of silicon from the front of the wafer, the other two from the back:

(i) One front-etching technique uses the n-well as an electrochemical etch stop for EDP or TMAH and forms an n-well silicon beam suspended by dielectric hinges with electrical leads.[25] This thermally insulated n-well carries a CMOS circuit, which can be used for a temperature-regulated bandgap voltage reference[25] or a thermal vacuum sensor.[26]

(ii) The other front-etch technique produces laminated high-aspect-ratio microstructures starting from a finished triple-metal CMOS wafer post-processed by anisotropic oxide etching (to cut through the dielectric layers) followed by anisotropic and isotropic silicon etching to release a beam.[27]

(iii) A thermally isolated closed silicon membrane carrying thermocouples can be obtained using a SIMOX (Separation by IMplanted OXide) substrate.[28] The final silicon

membrane (thickness 200 nm) is separated from the bulk silicon by the implanted oxide layer (thickness 400 nm), which stops etching with TMAH from the wafer back.

(iv) Monocrystalline silicon membranes formed by the epitaxial silicon layer can be obtained by post-processing electrochemical etching with bipolar IC or BiCMOS technology on (100) silicon; here the epi-junction serves as etch stop for KOH etching of the silicon substrate from the back.[29] Similarly, the substrate can be partially removed by KOH anisotropic etching under the epi-layer in order to suppress the substrate current of magnetotransistors.[30]

Moreover, sacrificial polysilicon layer etching can be combined with bulk silicon etching in order to form cavities for integrated infrared sensors.[31]

2.2 *Post-CMOS deposition*

The substrate temperature during deposition must be kept below 400°C in order to preserve the CMOS metallization structures (consisting mainly of aluminum) of the preceding IC process. Permalloy (NiFe) layers can be deposited and patterned on finished CMOS wafers in order to form magnetic flux concentrators, enhancing the sensitivity of integrated silicon magnetic field sensors[32] or accelerometers.[33] The cost-effective deposition process uses standard ultraviolet (UV) lithography, a UV-sensitive resist such as photosensitive polyimide, and electrodeposition.[33]

The deposition of moisture adsorbing or absorbing thin films such as porous ceramics or organic polymers has been used for the demonstration of IC humidity sensors. Chemically selective polymers can be deposited on CMOS capacitive structures for hydrocarbon sensing.[34] On-chip capacitance measurement circuitry is crucial in view of the required femto Farad capacitance resolution.[35] A combination of post-processing bulk silicon micromachining and polyimide deposition and patterning has been used to demonstrate the feasibility of a CMOS integrated multisensor for HVAC (heating, ventilation, air conditioning), including a thermal flow sensor supported by a CMOS dielectric membrane and a capacitive moisture sensor.[36]

A post-processing sequence producing three additional aluminum layers separated by low-temperature oxide and an air gap has been developed for future application to finished CMOS wafers.[37] The additional structure serves as a variable capacitor by acting as a tuning element in voltage-controlled oscillators.

2.3 *Other CMOS microtransducer technologies*

Replacement of the usual CMOS metallization by tungsten with $TiSi_2$ drain/source contact barriers allows post-CMOS micromachining and deposition with temperatures up to about 800°C.[38]

The BiMEMS technology of Analog Devices, Inc., combines the BiCMOS IC process with surface micromachined polysilicon structures for gyroscopes.[14,39] The IC process is interrupted before the last metallization; a spacer sacrificial oxide is deposited which allows the formation of 2-μm-thick polysilcon mechanical structures. Finally, the aluminum metallization and the passivation of the IC process are completed.

A combined pre- and post-CMOS approach has been proposed where the polysilicon mechanical structures are embedded in an anisotropically etched trench below the surface

of the wafer.[40] Prior to the CMOS IC fabrication, this trench is refilled with oxide, chemical-mechanically polished, sealed with a nitride cap, and annealed to relieve stress in the structural polysilicon. After completion of the IC process, the nitride cap over the micromechanical layer is removed and the micromechanical structures are released by etching.

A different kind of merged MEMS CMOS process uses silicon wafer bonding to create a substrate that can be fitted into an existing IC fabrication line.[41] Front-end micromachining is used to form a sealed cavity substrate. Since the cavity is internal to the substrate, IC fabrication can proceed as usual, followed by low-temperature post-CMOS micromachining steps. Recently, the SCREAM (Single-Crystal-silicon Reactive Etching and Metallization) MEMS process has been redesigned to fit post-CMOS processing.[42] CMOS chips have been equipped with aluminum hinges to make contact with microhandling systems thanks to post-CMOS dry etching using XeF_2.[43]

3. Post-CMOS Microsensor Prototypes

The post-CMOS technology outlined in sections 2.1 and 2.2 is illustrated by some prototypes designed, post-processed and characterized at the Physical Electronics Laboratory of ETH Zurich and CMOS-processed by its corporate partners. Sensors based on post-CMOS bulk micromachining (section 3.1), surface micromachining (section 3.2), deposition (section 3.3) and bulk micromachining combined with deposition (section 3.4) are reported.

3.1 *CMOS thermoelectric sensors*

An infrared sensor[1–5,23,44] and an electrical power sensor[2–5,24] are presented as examples of microtransducers based on closed CMOS oxide/nitride membranes supporting n-polysilicon/p-polysilicon thermopiles, which are available in bidoped-poly CMOS IC technology.

The infrared sensor shown in Fig. 4 converts infrared radiation to a temperature increase by absorption in the CMOS passivation. Silicon dioxide/nitride absorbs in the wavelength range between 8 μm and 14 μm, which is useful for intrusion detection. The resulting temperature increase of a few mK on the sensor membrane is detected by the thermopile. Optimized devices with 1 mm^2 membrane reach a responsivity of about 100 V/W, a detectivity of about 5×10^7 cm$\sqrt{\text{Hz}}$/W, and a rise time of about 30 ms. Co-integration of an auto-zero operational amplifier[6–8] with a gain of 1,000 leads to a responsivity of 10^5 V/W.

The AC power sensor or thermal converter detects the true root mean square value of an unknown ac signal in a wide frequency band. It is based on the square-law relationship between voltage and power in a 1000 Ω polysilicon heater resistor. The dissipated power is measured using bidoped polysilicon thermopiles with a sensitivity above 100 V/W. The nonlinearity at high power levels and the dependence on the ambient temperature are compensated for using a high dynamic range interface system.[6–8] It consists of two identical thermal converters operated at the same power level and a feedback circuit. The AC-DC voltage transfer difference is below 30 ppm between 1 kHz and 1 MHz. An

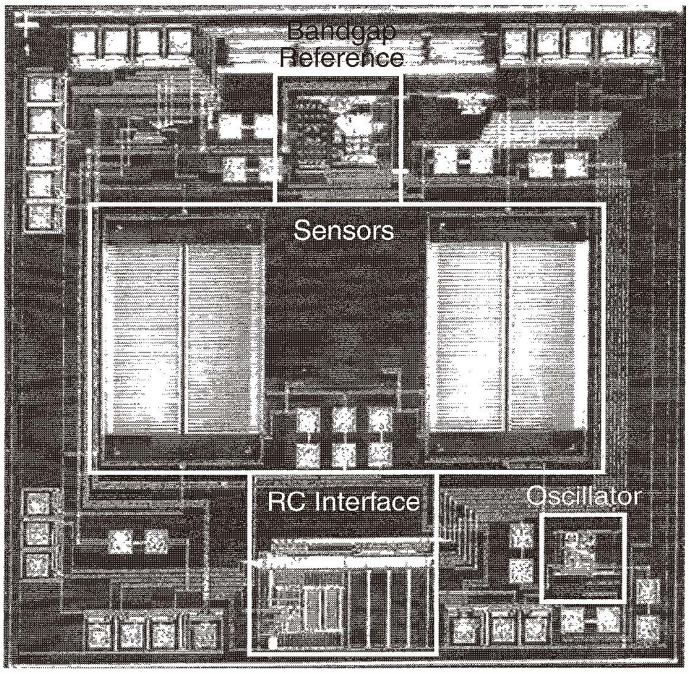

Fig. 4. Chip photo of two CMOS thermoelectric infrared sensors cointegrated with interface circuitry.

oversampled A/D converter embedded in the feedback loop provides a digital output proportional to the input power. The dynamic range is maximized by a variable bitstream amplitude adjusted according to the input signal and measured on-chip. Figure 5 shows an optical micrograph of an AC power sensor system chip with two pairs of thermal converters, one located on two separate membranes, the other on a single membrane.[24]

3.2 *Thermal vacuum sensor*

Thermal vacuum sensors can be based on the pressure-dependent heat transfer across an air gap separating a heat source from a heat sink. As shown in Fig. 1(b), the post-CMOS vacuum sensor[1–5,15–17] builds on the first metal layer (which is removed to form the gap), the intermetal dielectric, the second metal layer (which serves as heating resistor) and the passivation layer. The thermal power dissipated by the heater causes a temperature increase of the membrane, which depends on the thermal conductance provided by the (signal) heat transfer across the gap modulated by the air pressure and the (parasitic) heat flow through the sensor materials. The useful pressure range is 10^2 to 10^6 Pa in air.

Figure 6 shows a chip photo of the vacuum sensor microsystem[17] with four surface micromachined pressure sensors (with gap) and four reference structures (without gap)

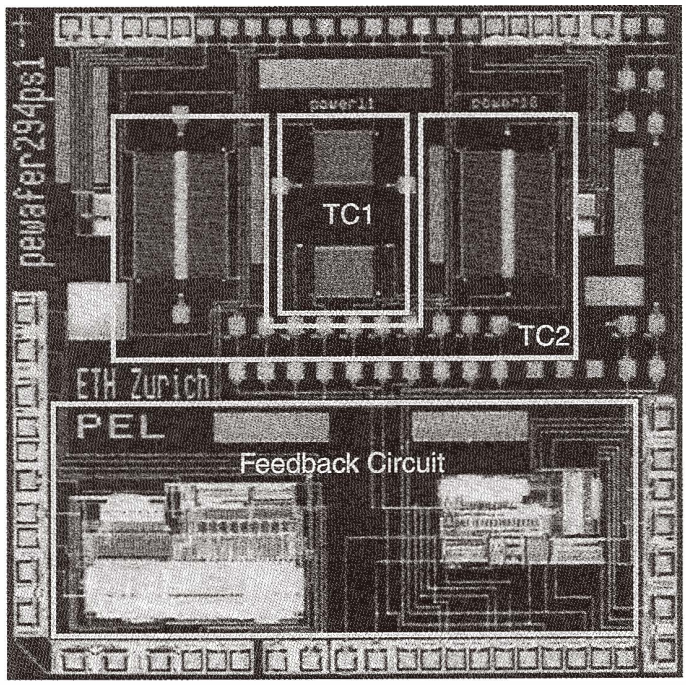

Fig. 5. Chip photo CMOS power microsensor with two pairs of thermal converters: one pair is located on two separate membranes, the other on a single membrane.

integrated with a front-end interface. The circuitry includes two incremental analog-to-digital converters and a bandgap reference, and measures the pressure-dependent power required to maintain a constant temperature increase of the sensors. The chip (3.3 mm by 2.8 mm) was fabricated using a 2 μm CMOS IC process followed by the sacrificial metal etching discussed in section 2.1.

3.3 *CMOS magnetotransistor with electroplated flux microconcentrator*

As mentioned in section 2.2, thick ferromagnetic films can be deposited on passivated silicon wafers by electrodeposition.[33] This technique allows fabrication of the lateral magnetotransistor (LMT) with the permalloy flux microconcentrator[2,32] shown in Fig. 7. The microconcentrator consists of two funnel-shaped parts separated by an air gap in order to capture the external magnetic flux and guide it to the LMT located below the gap. For magnetic fields below 1 mT, the microconcentrator enhances the sensitivity by more than a factor of 20.

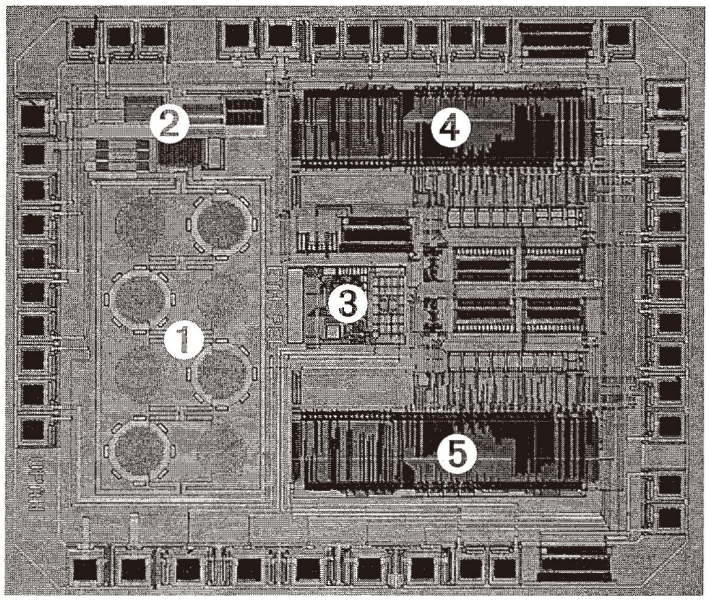

Fig. 6. Chip photo of CMOS microsystem consisting of four pressure and reference sensors (1) connected in series, front-end interface (2), bandgap reference (3), two incremental ADCs for current (4) and voltage (5) measurement.

3.4 *HVAC CMOS multisensor*

Heating, ventilation and air conditioning (HVAC) require the control of air flow, humidity and temperature. Figure 8 shows a multi-sensor chip[36] with an air flow, a humidity and a temperature sensor connected, via a multiplexer, to a second-order sigma-delta analog-to-digital converter achieving 15-bit resolution.[6–8] No additional read-out circuitry is required. Prototypes (area 7 mm by 4 mm) have been fabricated using a commercial 2 μm CMOS IC process combined with post-CMOS bulk micromachining and polyimide deposition.

The gas flow sensor consists of a CMOS dielectric membrane obtained by removing the bulk silicon locally under the thermal oxide. A heating resistor and p-polysilicon/n-polysilicon thermopiles are integrated in the membrane. The thermopiles measure the asymmetry of the temperature distribution occurring in the presence of flow. The humidity sensor consists of an interdigitated capacitor based on the CMOS metal layers; a polyimide cover is deposited after completion of the CMOS process. When the polyimide layer absorbs moisture from the environment, its permittivity, and thus the capacitance, increase. The chip includes an identical interdigitated structure, but without a polyimide cover, which serves as a reference capacitor.

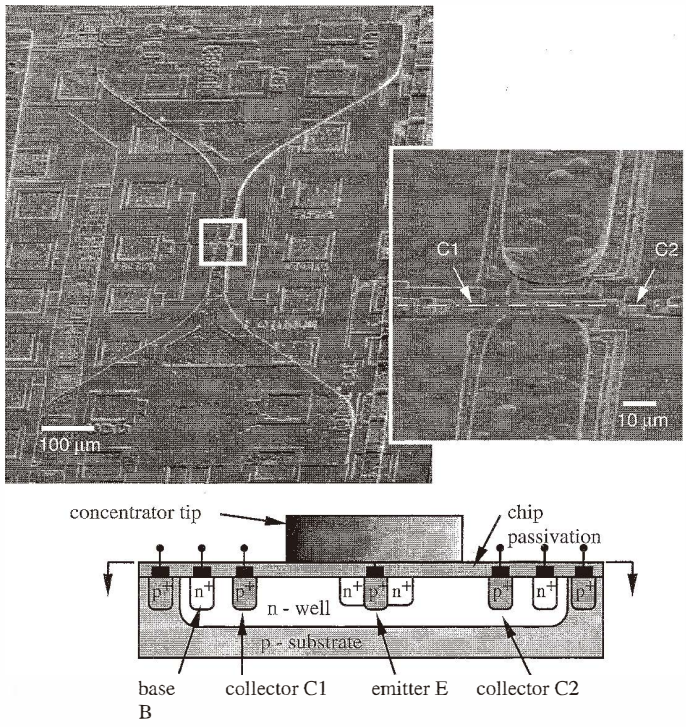

Fig. 7. SEM micrograph and cross section of CMOS dual-collector magnetotransistor with integrated permalloy flux concentrator made by post-CMOS electroplating.

4. Modeling and Characterization Tools

The design of CMOS MEMS is facilitated by the CAD tools SOLIDIS-a simulation toolbox for the numerical modeling of electrical, magnetic, thermal and mechanical effects and their couplings, and ICMAT-a data base of process-dependent electrical, magnetic, thermal and mechanical CMOS MEMS materials parameters measured with dedicated characterization microstructures, which may also serve as fabrication test structures.

4.1 *SOLIDIS*

SOLIDIS was developed at the Physical Electronics Laboratory of ETH Zurich [9–11,45–47] for efficient and accurate simulation of realistic three-dimensional microstructures performed by the microtransducer designers. The benefits are fast and inexpensive numerical simulation (faster and less expensive than prototyping) and the clarification of topographically complex scenarios.

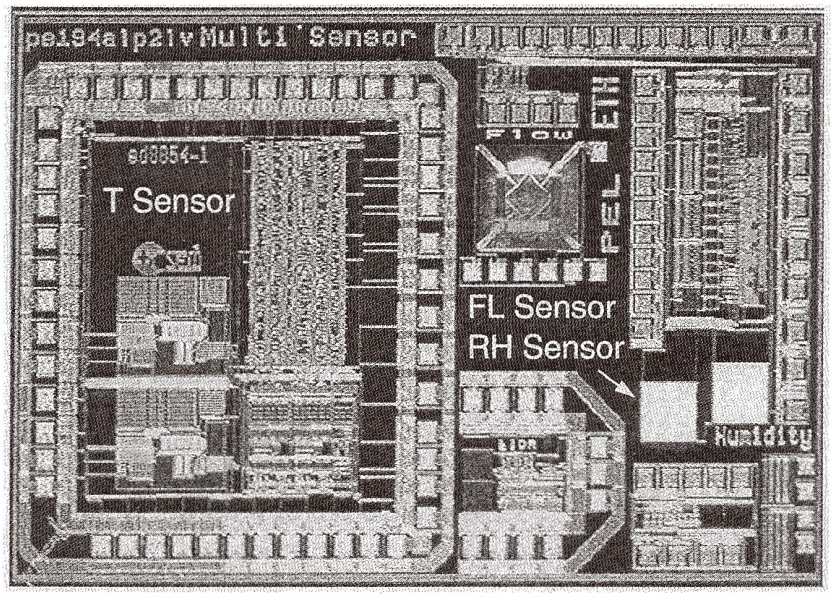

Fig. 8. Chip photo of CMOS HVAC multi-sensor for temperature (T), air flow (FL), and relative humidity (RH).

Coupled physical effects are basic to many IC microtransducers. The finite element program system SOLIDIS reflects this fact by providing analytical facilities for different physical effects in both individual and coupled form. The theoretical basis for the coupling is an Onsager scheme for the case of irreversible effects, and a Nye scheme for the case of reversible effects. Both of these have similar mathematical structure and only contain operators derived from conservation and constitutive laws. The variables and operators are discretized using the finite element method, and the discrete system of equations is automatically partitioned to reflect the different coupling requirements of various zones in a typical microstructure.

The present program couples electrostatics, thermostatics and elastostatics. These three effects are important not only in MEMS devices, but also for any other micromechanical structure producing heat, as well as for packaged microsystems. Crucial to the microtransducer designer are the available boundary conditions, interface conditions and nonlinear physical model equations. Accuracy is attained by automatic adaptation of the finite element mesh according to a refinement estimator, together with the ability to solve for very large meshes (about 100,000 finite elements) on engineering workstations in reasonable time. As an example, the simulation[11] of the fabricated electrostatically actuated integrated micromirror in Fig. 3 is shown in Fig. 9.

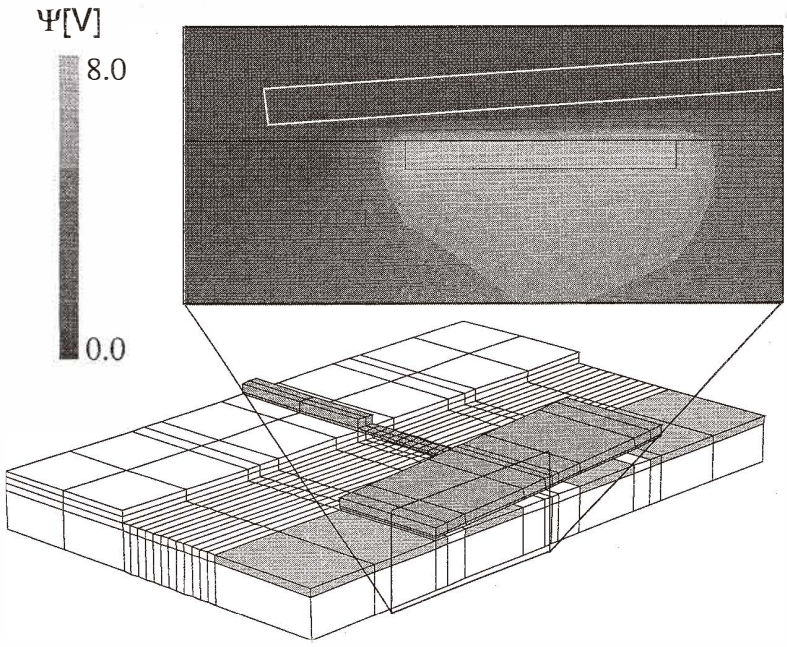

Fig. 9. Coupled simulation of deflection and electrostatic potential distribution in a cross section of the micromirror shown in Fig 3.

4.2 *ICMAT*

The knowledge of precise values of material properties is a prerequisite of design and simulation of microtransducers. This is particularly true for microstructures produced using commercial CMOS processes. Many more physical properties than those routinely monitored in IC fabrication play a role and must be determined for each CMOS layer:

- Thermal properties such as thermal conductivity and heat capacity.
- Electronic transport properties such as thermopower, carrier density n (or p) and piezoresistance of polysilicon.
- Mechanical properties such as Young's modulus, Poisson's ratio and stress.

A systematic characterization of these thin film properties and the variation with different vendors, processes, and batches is required in view of their process-dependence.[4,5,10,48–50]

These measurements are conducted using dedicated CMOS-compatible characterization microstructures, an example of which is shown in Fig. 10. Such test structures are produced by appropriate design layout and post-CMOS technology similar to the post-CMOS microtransducer technology described in section 2.1. The thermal properties of oxides are only slightly different from the bulk values. Metal layers have thermal conductivities reduced by typically 30% from bulk. The thermal properties of polycrystalline silicon deviate strongly from those of monocrystalline silicon.[48–50]

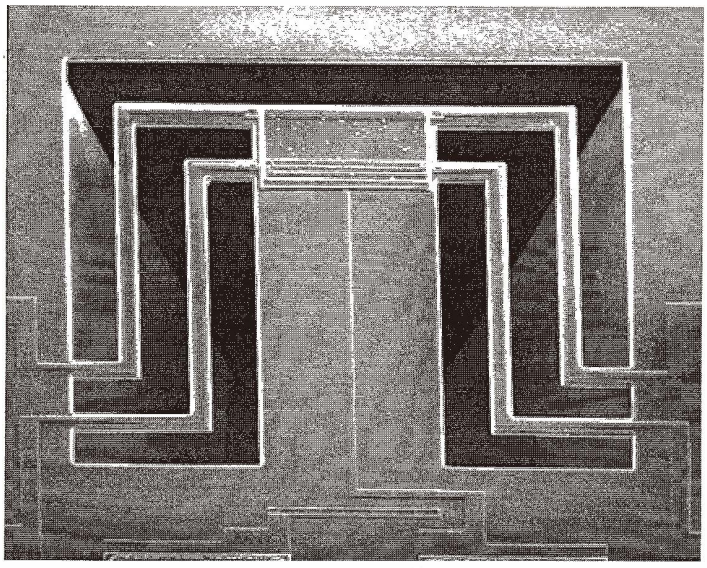

Fig. 10. SEM micrograph of characterization microstructure, with polysilicon heating resistor and thermistor at the tip, used to determine the Seebeck coefficient of a CMOS polysilicon layer.

5. Outlook

From the technological feasibility viewpoint, the most promising technologies for CMOS MEMS products are those requiring minimal post-processing of finished CMOS wafers. Simple intermediate processing using conventional IC fabrication equipment with the wafers remaining in the CMOS line is another likely candidate. While industrial CMOS MEMS chip manufacturing seems to be only a couple of years away, the packaging of microtransducers is more demanding. Strong efforts must be made to develop microtransducer packaging techniques, case by case, until they become established.

By exploiting the predicted progress of semiconductor IC capabilities, the part that makes the sensor smart will increase at a phenomenal rate. By the year 2010 we will probably have not only a pressure sensor with integrated microcontroller, but also the HVAC sensor, the viscosimeter and even the taste sensor, artificial nose and atomic force microscope on a chip. Thus the trend to merge MEMS and IC technologies will continue. The author believes that the potential for joint university-industry IC MEMS development is overwhelming.

Acknowledgments

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