High-performance Electrostatic Discharge Protection Device for Power Chip Based on 28 nm Process

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As the characteristic size of semiconductor devices in ICs decreases, ICs are becoming more sensitive to electrostatic discharge (ESD). Electrostatic protection has become one of the most important reliability indexes in ICs, and the ESD protection structure has also become a difficult problem in chip design. A sensor exposed to static electricity can be damaged and its output signal can be disturbed. Therefore, electrostatic protection also plays an important role in sensors. As the scale of ICs increases, the number of chip pins is increasing and a larger area is being used for ESD protection circuits, resulting in higher costs. Silicon controlled rectifier (SCR) ESD protection devices have the highest performance per unit area among the known ESD protection structures, and are thus the first choice for low-cost, on-chip ESD design solutions. In this study, through a Sentaurus simulation, two SCRs with different structures (a directly connected SCR and a modified lateral SCR) are established, and transmission line pulse tests are carried out on the two devices. The key characteristic indexes are analyzed theoretically and by using experimental data. According to the simulation results, the opening voltage of the directly connected SCR is about 1.5 V and its secondary breakdown current is above 5 A, indicating that the device has a high protection level.

1. Introduction

Electrostatic discharge (ESD) is a common phenomenon in nature. With the reduction of the semiconductor manufacturing process size and the increasing scale of ICs, the problems of electronic product failure and yield reduction caused by ESD are becoming increasingly significant. Therefore, ESD has been paid increasing attention in industry.[1] ESD also plays an important role in the sensor field. To reduce the loss caused by ESD, the ESD protection of ICs has become an essential part of chip design. Although the working voltage of a chip decreases with the reduction of the process size, the rate of decrease is much lower than that of the breakdown voltage of the oxide layer and the source/drain, which leads to serious compression of

the ESD protection design window, and ESD design is facing increasing challenges. Therefore, it is of great importance to explore ESD protection devices with a low trigger voltage, low on-resistance, and high robustness for the construction of all-chip ESD protection schemes in small-size processes.[2]

Although traditional silicon controlled rectifiers (SCRs) naturally have advantages including high discharge efficiency, robustness to excess electrical stress, low static leakage, and small parasitic capacitance, their trigger voltage is also very high, which is a problem that must be solved for traditional SCRs to ensure excellent discharge performance. Upon lowering the trigger voltage, care should be taken to maintain the voltage to avoid latch problems. By adjusting the device structure or process parameters, or adding trigger (detection) circuits and other means, we can reduce the trigger voltage, improve the hold voltage, reduce the parasitic effect, and avoid latch problems.[1] Therefore, reducing the trigger voltage of the device and improving the protection level have become important directions for SCRs. On the basis of these two points, two different types of SCR structures were designed in this study.

2.   Analysis and Design of SCRs

2.1   Basic principle of analysis of SCRs

The I–V hysteresis curve in Fig. 1 is characterized by three inflection points: at the first inflection point A (V_{t1}, I_{t1}), V_{t1} is the triggering voltage and I_{t1} is the triggering current; at the second inflection point B (V_h, I_h), V_h is the maintenance voltage and I_h is the maintenance current; at the third inflection point C (V_{t2}, I_{t2}), V_{t2} is the secondary breakdown voltage and I_{t2} is the secondary breakdown current.[3] The basic working mechanism of the SCR is as follows.

(a) Cutoff state: Under normal working conditions, the anode of the device is connected with a high potential and the cathode is grounded. At this time, the N-well of the device is inversely aligned with the p-type substrate, the reverse-biased diode leakage current is very low, and the device is in the cutoff state.

(b) Trigger voltage on state: When the voltage of the anode reaches the trigger voltage V_{t1}, avalanche breakdown occurs in the pn junction of the negative–positive–negative (NPN) transistor, and a current starts to be generated. The current creates a voltage drop across the
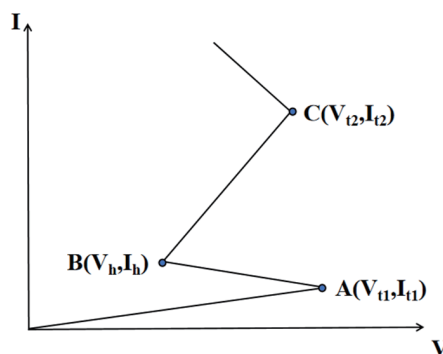

Fig. 1. I–V hysteresis curve of basic SCR.

parasitic resistance of the p-type substrate. When the voltage drop is greater than the forward-biased junction voltage between the base and the emitter of the NPN transistor, the NPN transistor is triggered to conduct, and the current is further amplified. The parasitic resistance of the N-well creates a voltage drop because there is current flowing. This voltage is applied across the base and emitter of the positive–negative–positive (PNP) transistor, and the current is further amplified. Therefore, the PNP transistor and the NPN transistor form a positive feedback loop.

(c) Hold the discharge stage: The device enters the hysteresis zone, as shown in Fig. 1. In the negative resistance zone of the hysteresis curve, the device voltage decreases to the holding voltage V. Then, with the sharp increase in current, the ESD event current is released rapidly and the voltage increases slightly.

(d) Second breakdown current stage: As the current continues to increase, the temperature of the semiconductor also rises due to the continuous high-current flow. When the temperature reaches the melting point of silicon, the device undergoes thermal breakdown, and the breakdown current is I_{t2}, corresponding to the third inflection point in Fig. 1. After that, the device completely fails and becomes a conductor.

At present, a transmission line pulse (TLP)[4,5] tester or human body model (HBM) tester is used to test the protection effect against ESD. An HBM tester can simulate a complete HBM waveform test but is relatively expensive; thus, a TLP tester is generally used. The CDM mode is tested with an ultrashort pulse (VF-TLP) tester, which is very similar to a TLP tester but produces a pulse with a shorter rising edge and a shorter duration.

The principle of a TLP test is to use the transmission line to generate a series of stable pulsed square waves that gradually increase according to the set voltage step size to simulate the discharge waveform under different ESD stresses. These pulsed square waves are applied to the device in sequence. After each pulse, the test device records the current and voltage waveforms generated on the device. By extracting and calculating the voltage and current waveform data, the *I*–*V* characteristic points of the device under the impact can be obtained.. After many pulses, a series of *I*–*V* characteristic points obtained from the test are plotted on a curve. The *I*–*V* characteristic curve reflecting the change of the device characteristics can be obtained.

As can be seen from Fig. 1, the SCR device immediately enters the hysteresis zone after triggering and opening, and the voltage decreases rapidly and the current increases. At this time, the NPN and PNP transistors operate in the saturation zone. The minimum voltage at the anode and cathode ends of the device in the hysteresis zone is defined as the holding voltage V_h of the ESD device, and the current is the holding current I_h, corresponding to the second inflection point of the curve in Fig. 1.

V_h is analyzed using the equivalent circuit diagram in Fig. 2 and is given by

$$V_h = V_{BE1} + V_{CES2} = V_{BE2} + V_{CES1}. \tag{1}$$

In this formula, V_{BE1} is the base and emitter voltage of the NPN transistor (about 0.7–1 V) and V_{CES2} is the voltage difference between the PNP collector and transmitter in the saturation region (about 0.5–0.7 V); thus, V_h is about 1.5 V, which is less than most of the chip supply
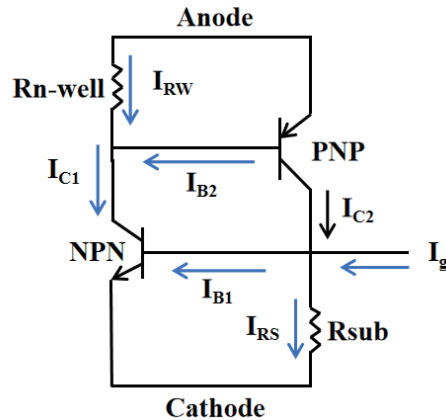
Fig. 2.   (Color online) Equivalent circuit diagram of basic SCR device.

voltages (VDD). If no improvement measures are taken, under the existing 3.3 or 5 V power supply voltage in the CMOS process, it is very easy to cause the chip latch-up effect.

The holding voltage in the equivalent circuit in Fig. 2 is analyzed as follows.

$$I_{C1} = I_{RW} + I_{B2} = \beta_1 \times I_{B1} \tag{2}$$

$$I_{C2} = I_{RS} + I_{B1} = \beta_2 \times I_{B2} \tag{3}$$

$$I_h = I_{RS} + I_{E1} = \frac{V_{BE1}}{R_{sub}} + (\beta_1 + 1)I_{B1} \tag{4}$$

These formulas are combined to obtain

$$I_h = \frac{\beta_1(\beta_2 + 1)}{\beta_1\beta_2 - 1}\frac{V_{BE1}}{R_{sub}} + \frac{\beta_2(\beta_1 + 1)}{\beta_1\beta_2 - 1}\frac{V_{BE2}}{R_{n-well}}. \tag{5}$$

Since $\beta_1\beta_2$ is much greater than 1, we obtain

$$I_h = \frac{V_{BE1}}{R_{sub}} + \frac{V_{BE2}}{R_{n-well}}. \tag{6}$$

With this formula, the substrate resistance and well resistance can be adjusted to change the holding current.

After the SCR device enters the positive feedback conduction discharge area, the current increases sharply due to the positive feedback. Between the second and third inflection points in Fig. 1, part of the device melts due to the excessive current and temperature rise, resulting in the complete conduction of the device, that is, complete breakdown (secondary breakdown) of the device.

In Fig. 1, the slope of the line between points B and C is approximately equal to the conducting resistance R_{on}, from which the following formula can be obtained:

$$V_{t2} = (I_{t2} - I_h)R_{on} + V_h. \tag{7}$$

With the formula, I_{t2} can be measured by performing a transient pulse test on the device, and the secondary breakdown current is related to the protection level of the device. For example, the HBM satisfies

$$V_{HBM}(\text{kV}) = K \times I_{t2}(\text{A}), \tag{8}$$

where K is determined by the process conditions and is generally 0.96–1.71. Therefore, the ESD protection level of the HBM of the device can be determined using this formula and the secondary breakdown current.

2.2   Device structures and operation mechanisms

The structure of a directly connected SCR (DCSCR)[6,7] is shown in Fig. 3. It is composed of two adjacent diodes, D1 (P+/N-well diode) and D2 (P-well/N+ diode). The connecting end (N+ end) of diode D1, where the anode is located, and the connecting end (P+ end) of diode D2, where the cathode is located, are directly connected through metal wires. If the ESD pulse applied to the anode of the device is greater than the sum of the positive guide voltages of diodes D1 and D2, then the two diodes conduct electricity, and the parasitic PNP and NPN transistors conduct at the same time. As the current increases rapidly, positive feedback of the transistor occurs and the main SCR turns on (the SCR path is shown by the red line). Owing to the rapid positive feedback process resulting from ESD current injection, the triggering voltage of the SCR channel is mainly determined by the positive guide voltages of diodes D1 and D2.

The DCSCR structure reduces the trigger voltage of a traditional SCR device to the sum of the positive guide voltages of the two diodes, which means that SCRs are widely used at low
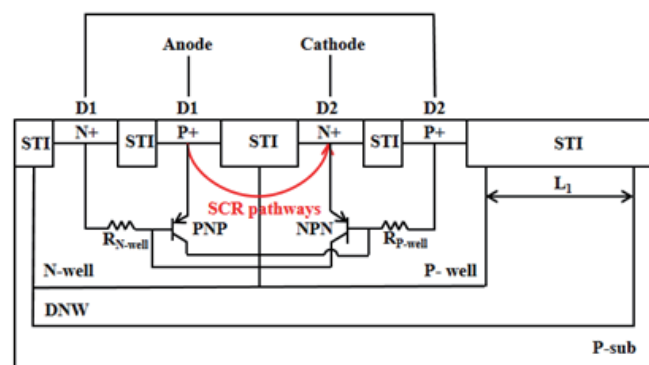

Fig. 3.   (Color online) Structure and equivalent circuit diagram of DCSCR.

voltages. The P-well of the DCSCR, which is the anode of diode D2, requires a nonzero potential to keep diode D2 on; thus, the P-well must be isolated from the grounded P-sub.

Figure 4 shows the structure of a modified lateral SCR (MLSCR).[8–10] Compared with the basic structure, there is an additional P+ region between the N-well and P-well, and there is also N+ doping. The P+ region is more concentrated than the P-well, and the avalanche breakdown region is not the contact surface of the N-well and P-well but that of the N-well and P+ contact. The breakdown voltage is reduced, resulting in a reduction in the trigger voltage of the SCR device.

3.   Results and Discussion

In this study, two SCR structures (DCSCR and MLSCR) based on a 28 nm process are designed.[11–13] A series of simulated HBM pulses are applied to both structures. The rising edge time of the pulse current is 10 ns, the falling edge time is 10 ns, and the pulse width is 150 ns. The size of the pulse current is set according to the turn-on current, discharge current, and secondary breakdown current of the device. By applying a series of current pulses, the electrical parameters of the device under different pulse stresses, such as the holding voltage, turn-on voltage, and secondary breakdown current, can be measured and used to analyze the maximum endurance of the device.

3.1   Simulation settings for SCR devices

To study the maximum withstand capability of the DCSCR and increase its protection level, a current pulse is applied to the DCSCR. The rising edge time of the pulse current applied to the DCSCR is 10 ns, the pulse width is 150 ns, the falling edge time is 10 ns, and the pulse current size is set to 1, 3, 4, 4.5, 5, 6.5, 7.5, 8.5, 8.6, 8.63, and 8.75 A. The pulsed current is applied across the anode and cathode of the DCSCR. A suitable computational model is selected for the simulation, in which the computation is performed for each pulse. The maximum temperature–time curve and *I–V* characteristic curve for each pulse are obtained.
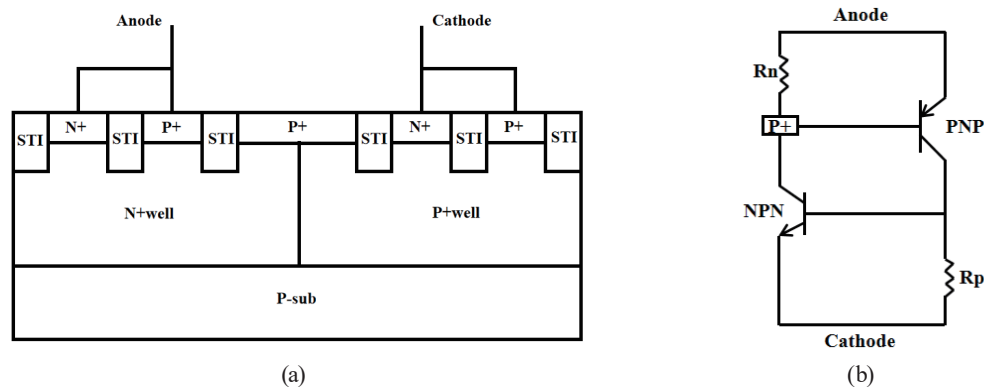

Fig. 4.   (a) Structure of MLSCR. (b) Equivalent circuit diagram of MLSCR.

The pulse current applied to the MLSCR is 1, 2, 2.08, or 2.1 A, which is applied to its anode and cathode. Owing to the high-voltage and high-current environment of the ESD pulses, the simulation setup in this study takes into account the following relevant physical models, equations, and temperatures:

(a) As the carrier mobility model, the HighFieldSaturation model, DopingDependence model, Enormal model, and PhuMob model are considered.

(b) For the carrier generation and recombination mechanisms, the Avalanche model, indirect recombination model (SRH model), and Auger model are considered.

(c) For other aspects, the EffectiveIntrinsicDensity model, thermodynamic model, and AnalyticTEP model are considered.

(d) During the simulation, the Poisson equation, semiconductor transport equations, and electron/hole continuity equations are used.

(e) The substrate during the device simulation is the heat dissipation area, and the ambient temperature is set to 300 K.

3.2 Results for DCDCR and MLSCR

As shown in Fig. 5, when the pulse current applied by the DCSCR is 8.63 A, the temperature of the device does not stabilize and begins to drift upward. This shows that the pulse current at this time has reached the secondary breakdown current of the device. When the applied pulse current of the MLSCR is 2.08 A, the current reaches the secondary breakdown current.

As shown in Fig. 6, when the voltage increases to 4.94 V, the DCSCR starts to conduct. The voltage at this time is the turn-on voltage of the device. After the device is turned on, the voltage decreases to a minimum value, which is the voltage at the second inflection point on the curve. The voltage at this time is the holding voltage of the device. The device quickly discharges the electrostatic current, the voltage increases slowly, and the current increases sharply to the third inflection point. The third inflection point is the secondary breakdown current and secondary breakdown voltage of the device. The MLSCR also has the same hysteresis characteristics as the DCSCR.
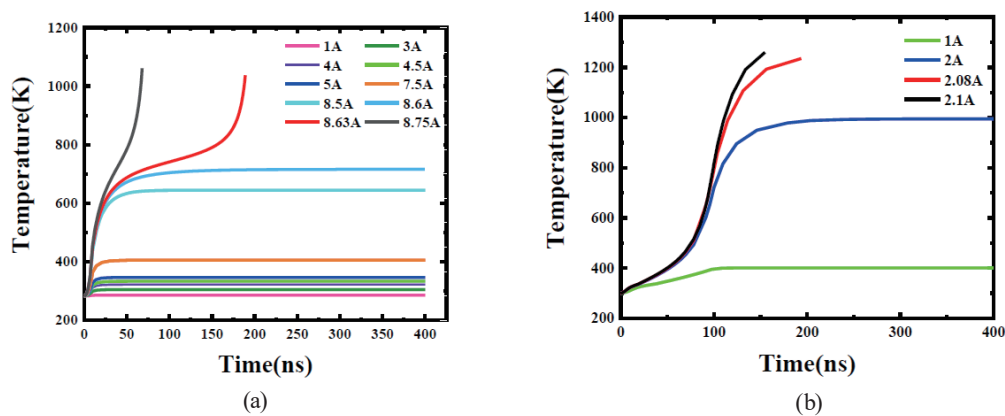

Fig. 5.   (Color online) Temperature–time curves obtained by multiple single-pulse transient simulations of (a) DCSCR and (b) MLSCR.
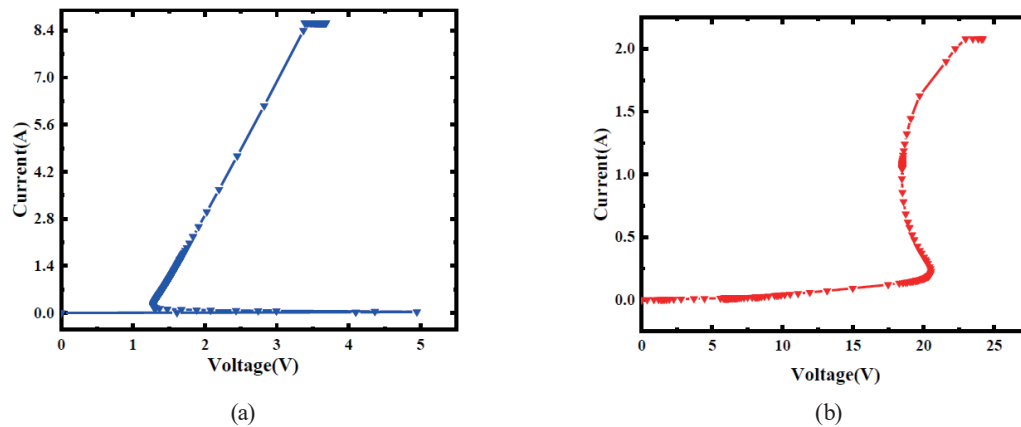
Fig. 6.   (Color online) (a) Hysteresis curve of DCSCR at applied current of 8.63 A. (b) Hysteresis curve of MLSCR at applied current of 2.08 A.

Table 1
TLP test results for DCSCR and MLSCR.

Device	V_{t1} (V)	I_{t1} (A)	V_h (V)	I_h (A)	V_{t2} (V)	I_{t2} (A)
DCSCR	4.94	0.03	1.28	0.20	3.36	8.4
MLSCR	20.51	0.23	18.47	1.05	22.97	2.08

As can be seen in Table 1, the turn-on voltage of the DCSCR is much smaller than that of the MLSCR. Also, the secondary breakdown current of the DCSCR is larger than that of the MLSCR. The discharge capability of the DCSCR is stronger than that of the MLSCR. Because the DCSCR is compared with an ordinary SCR device, its anode and cathode are placed inside the device, changing the current direction of the diode in the series path inside the device. It can be seen from the DCSCR structure diagram that the current discharge path of the DCSCR is composed of a P+/N-well diode and a P-well/N+ diode, and the diode path is composed of N+ and P+. This makes the SCR path shorter and easier to trigger.[14,15] The turn-on voltage of the MLSCR is about 20 V, while the turn-on voltage of ordinary SCRs is 24 V. The reverse breakdown current of the diode is reduced because of the heavy doping of P+ inserted in the middle of the diode. The holding voltage of the MLSCR device is higher because the middle P+ region increases the current path and, at the same time, the on-resistance increases.

From the current density plot, it can be seen that the current of both devices is concentrated near the anode (Fig. 7). This is due to the pulsed current applied to the anode. On the other hand, the MLSCR has a widened current path due to the insertion of a heavily doped P-type region, which makes the current distribution of the entire device more uniform. The temperature in the DCSCR and MLSCR devices is highest at the PN junction (Fig. 8). Because the avalanche breakdown of the PN junction occurs, the local temperature caused by the breakdown is high. Overall, the current distribution of the two devices is uniform, the robustness is good, and the current discharge ability is high.
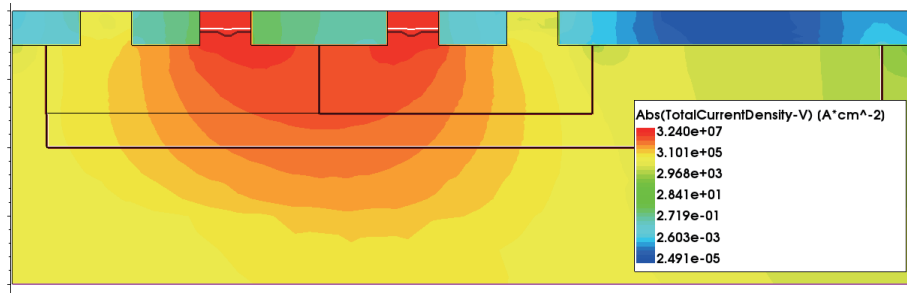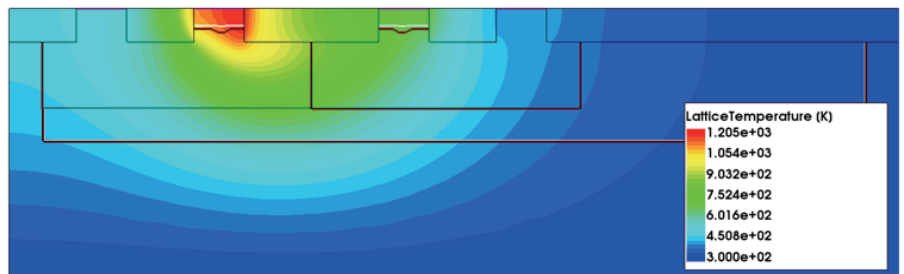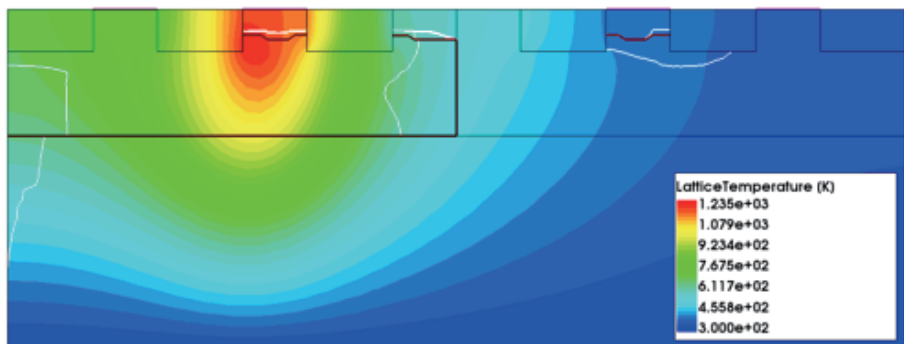
(a)
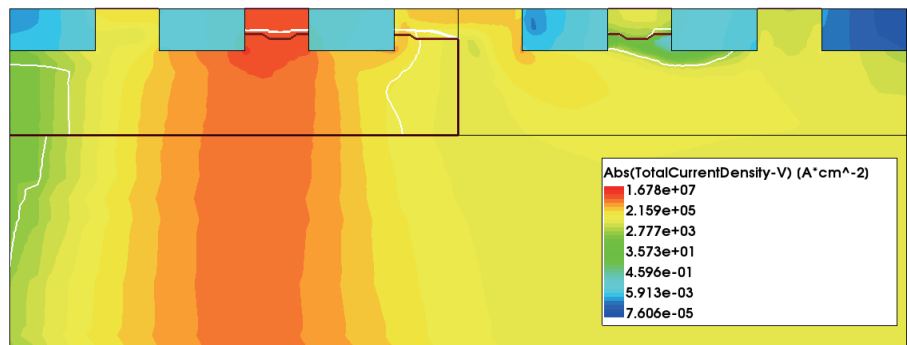
(b)

Fig. 7.   (Color online) Current density diagrams. (a) DCSCR. (b) MLSCR.

(a)

(b)

Fig. 8.   (Color online) Temperature distributions of devices. (a) DCSCR. (b) MLSCR.

4. Conclusions

In this paper, DCSCR and MLSCR device structures are proposed for the traditional SCR structure. For these two structures, a TLP test is simulated by TCAD. The DCSCR has a low open voltage and a high secondary breakdown current, whereas the MLSCR has a more uniform current density and temperature distribution because of P+ doping. The sensor transmission signal will be disturbed by static electricity. Therefore, the study of ESD devices is of great significance for the protection of sensors.

Acknowledgments

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