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Chopper-stabilized Multipath Instrumentation Amplifier with Output Voltage Offset Compensation Using R-2R Digital-to-Analog Converter

Hyunwoo Heo,[1] Hyungseup Kim,[1] Donggeun You,[1]
Yongsu Kwon,[1] Dong-il "Dan" Cho,[2] and Hyoungho Ko[1*]

[1]Department of Electronic Engineering, Chungnam National University, Daejeon 34134, Republic of Korea
[2]ASRI/ISRC, Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, Republic of Korea

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This paper presents a 3-opamp resistive bridge sensor analog front-end (AFE) integrated circuit (IC) with offset voltage compensation using an R-2R digital-to-analog converter (DAC). The proposed IC is implemented with a 3-opamp instrumentation amplifier (IA) to achieve high gain, high input impedance, and linearity. The two amplifiers in the first stage are multipath amplifiers with a chopper stabilization technique and ripple reduction loop (RRL). The chopper stabilization technique reduces 1/f flicker noise and DC offset, and the RRL mitigates the output ripple voltage resulting from the chopper stabilization technique. The multipath amplifier scheme compensates the notch characteristic in the frequency response caused by the RRL. A fully differential amplifier with a class-AB output stage is used in the second stage to achieve power efficiency. The 12-bit R-2R DAC is implemented to compensate the offset of the second-stage output of the IA. The IA gain can be controlled from 12 to 48 dB using 2-bit and 3-bit programmable feedback resistor arrays in the first and second stages, respectively. The proposed IC is designed with a 0.18 μm complementary metal-oxide-semiconductor (CMOS) process and has an active area of 7.2 mm^2. The simulated input-referred noise is 36.7 nV/√Hz at a frequency of 1 Hz and the simulated input offset voltage is 2.2 μV.

1. Introduction

As the nano/micro-electromechanical system (NEMS/MEMS) sensor market continues to grow with the development of Internet of Things (IoT) technologies and the demand for high-performance sensor applications increases, high-precision sensor interface circuit technology is required. Resistive MEMS sensors are used in various applications such as strain gauges, pressure sensors, acceleration sensors, and force sensors.[1–5] For the implementation of a high-precision sensor interface circuit for these high-performance resistive sensors, low noise, low offset, and high input impedance are required. There are two general architectures for a resistive

*Corresponding author: e-mail: hhko@cnu.ac.kr
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sensor interface circuit: a current-feedback instrumentation amplifier (CFIA) and a 3-opamp voltage feedback instrumentation amplifier (IA).[6] The CFIA has an advantage of high input impedance but the gain accuracy is limited due to the mismatch between the transconductance of the input stage and the output stage. The 3-opamp IA has high input impedance and can also achieve high linearity, and because the gain of the IA is determined by the resistance ratio, the IA gain can be controlled easily.[7] This paper presents a resistive sensor analog front-end (AFE) using a 3-opamp architecture.

To obtain a low-noise and high-precision sensor interface circuit, the auto-zeroing and chopper stabilization techniques are commonly used.[8] The auto-zeroing technique involves subtracting the offset voltage and reducing the low-frequency noise using a sampling capacitor. However, this technique is only suitable for discrete time operation and has limited ability to remove low-frequency noise because of noise folding due to aliasing. The chopper stabilization technique modulates low-frequency noise and generates a high-frequency ripple voltage at the output. As the low-pass filter (LPF) needed to remove this ripple voltage occupies a large area, a ripple reduction loop (RRL) can be used.[9] However, the RRL causes a notch characteristic in the frequency response near the chopper frequency and limits the bandwidth of the IA.

This paper presents a chopper-stabilized multipath IA using a 3-opamp architecture with offset voltage compensation using an R-2R digital-to-analog converter (DAC). The multipath amplifier consists of a low-frequency path and a high-frequency path, and compensates the bandwidth limitation caused by the RRL. The R-2R DAC is used in the input of the second stage and is implemented with a fully differential amplifier to compensate the output offset voltage.

2. Proposed 3-Opamp Multipath IA with R-2R DAC

2.1 Top architecture

The proposed resistive sensor AFE is implemented with a 3-opamp structure for high input impedance and high linearity. The proposed 3-opamp multipath IA with a 12-bit R-2R DAC is shown in Fig. 1. The first stage is implemented with chopper-stabilized multipath amplifiers for low-frequency noise performance, and the second stage is implemented with a fully differential amplifier with chopper stabilization and an RRL. A 12-bit R-2R DAC is used to calibrate the offset voltage. The output of the IA can be expressed as

$$V_{out} = \frac{R_4}{R_3} \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot (V_{inp} - V_{inn}) - \frac{R_4}{R_{DAC}} \cdot V_{DAC} \,. \tag{1}$$

The feedback resistors R_2 and R_4 make up 2-bit and 3-bit programmable resistor arrays, respectively, and the gain of the IA can be controlled from 12 to 48.16 dB.

2.2 Multipath amplifier

Figure 2 shows the structure of the multipath amplifier used in the proposed IA. The multipath amplifier consists of a high-frequency path and a low-frequency path. The high-

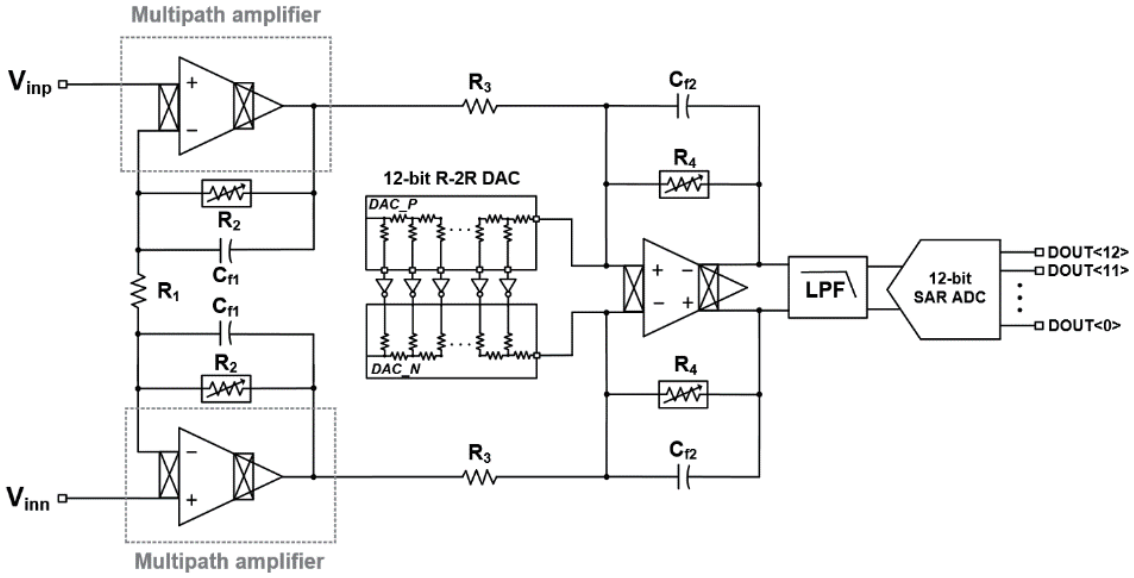

Fig. 1. Top architecture of proposed multipath IA with output voltage offset compensation using R-2R DAC.

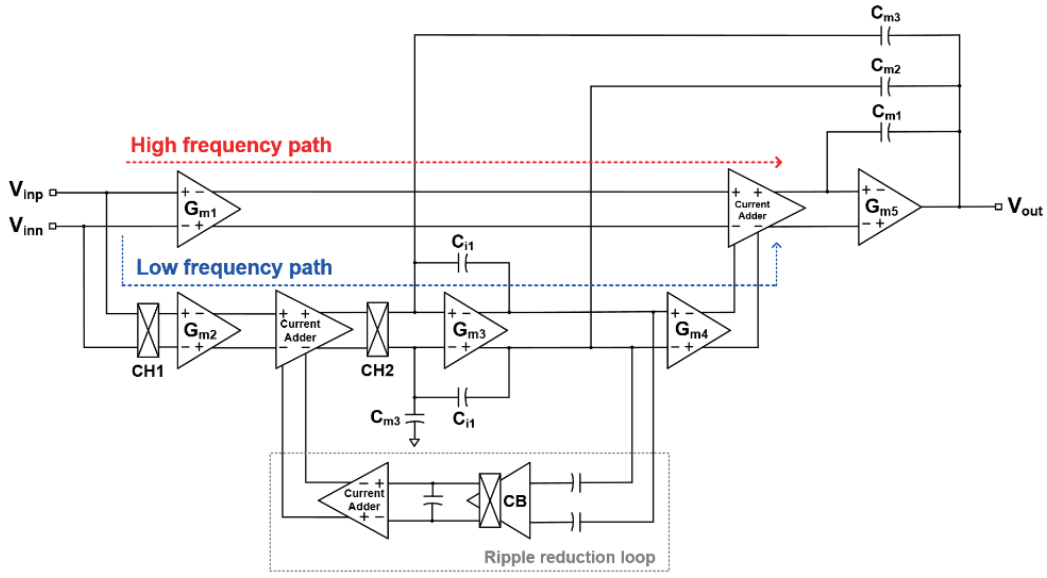

Fig. 2. (Color online) Schematic of the multipath amplifier.

frequency input is amplified twice by G_{m1} and G_{m5} in the high-frequency path, and the low-frequency input is amplified four times by G_{m2}, G_{m3}, G_{m4}, and G_{m5} in the low-frequency path. To reduce the low-frequency noise such as the offset and low-frequency noise, chopper stabilization is implemented in the low-frequency path.

In the low-frequency path, an input signal in the baseband is modulated by chopper CH1. The modulated input signal is demodulated by chopper CH2 to the baseband and the offset or the low-frequency noise is also modulated by CH2. The modulated offset or low-frequency noise appears as a ripple at the output voltage. A multistage LPF is needed to remove this ripple

effectively, which deteriorates the area efficiency. To improve the area efficiency, an RRL is used in the low-frequency path. The RRL reduces the ripple at the output of G_{m3} by a feedback method using the current adder.

2.3 Fully differential amplifier

Figure 3 shows the structure of the fully differential amplifier used in the proposed IA. The fully differential amplifier is also implemented with chopper stabilization for low-frequency noise performance, and an RRL is used to reduce the ripple at the output. The common-mode rejection ratio (CMRR) is improved using two common-mode feedback (CMFB) circuits. The R-C CMFB in the cascode stage and the CMFB using the error amplifier give negative feedback of the common mode of the output signals of the cascode stage and the output stage, respectively.

2.4 12-bit R-2R DAC

Figure 4 shows the R-2R DAC circuit used for offset calibration. The R-2R DAC output can be controlled with a 12-bit digital register input. The upper four bits are operated by a thermometer code so that the error at the upper bits can be reduced. The R-2R DAC can calibrate the offset voltage from −3.3 to 3.3 V with a step size of 1.61 mV.

3. Simulation Results

The transient simulation result of the proposed IA is shown in Fig. 5. The graph shows the input and output forms of a differential signal. The gain of the IA is set to the maximum gain of

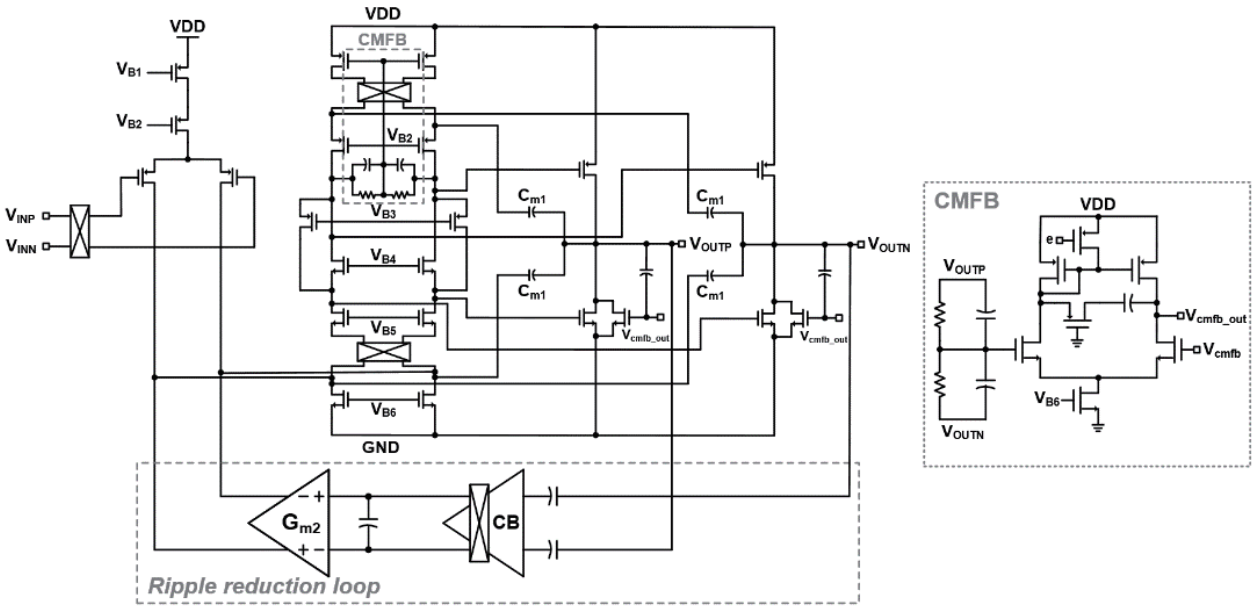

Fig. 3. Schematic of the fully differential amplifier.

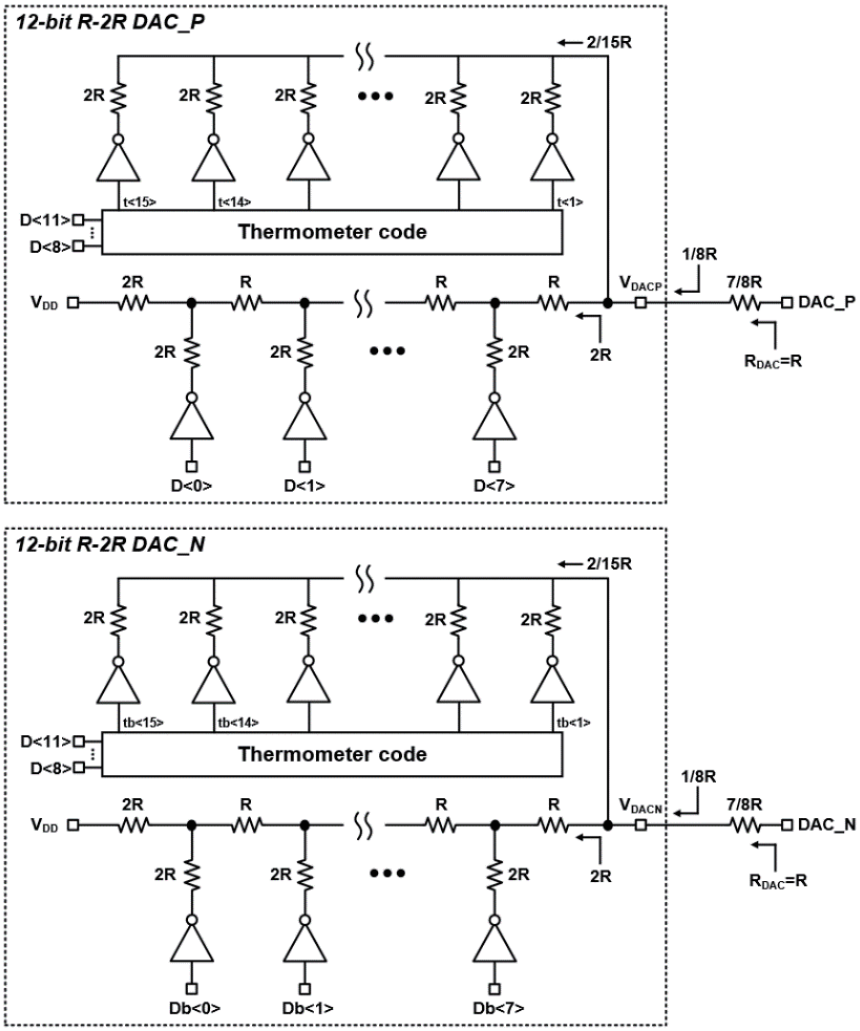

Fig. 4. Schematic of the 12-bit R-2R DAC.

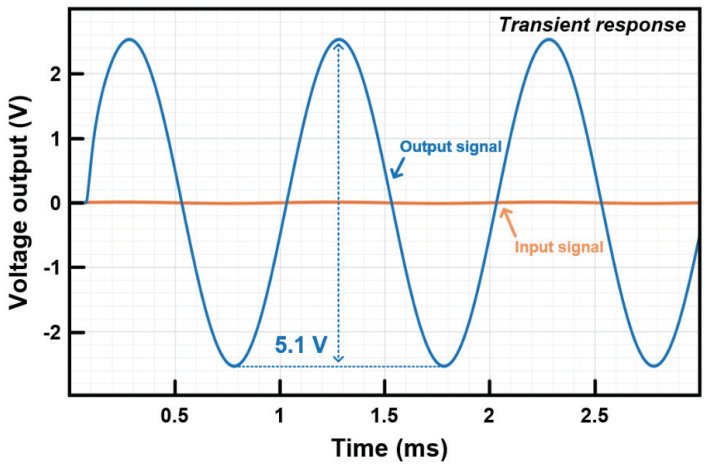

Fig. 5. (Color online) Transient simulation result of the proposed IA.

48.16 dB using the 2-bit and 3-bit programmable resistor arrays. An input signal of a 1 kHz sine wave with a peak-to-peak voltage of 20 mV is applied, and the output signal has a peak-to-peak voltage of 5.1 V.

Figure 6 shows the simulation result of the frequency response of the proposed IA. The chopper frequency is 125 kHz, and as the bandwidth limitation near the chopper frequency is compensated using the multipath amplifier, the IA has a unit-gain bandwidth (UGBW) of 904 kHz at the maximum IA gain of 48.16 dB.

The CMRR and the power supply rejection ratio (PSRR) simulation results are shown in Figs. 7 and 8, respectively. As the proposed 3-opamp resistive sensor AFE is implemented with a fully differential architecture and two CMFBs are used in the fully differential amplifier in the second gain stage, the IA achieves a high CMRR performance. The simulated CMRR and PSRR are 156.4 and 133.9 dB, respectively. Figure 9 shows the input-referred noise simulation result. The proposed IA has an input-referred noise of 36.7 nV/√Hz at a frequency of 1 Hz.

Figure 10 shows the DC offset voltage simulation result of the R-2R DAC. Under the variation of the digital register input code, the DC operating point of the IA output can be linearly

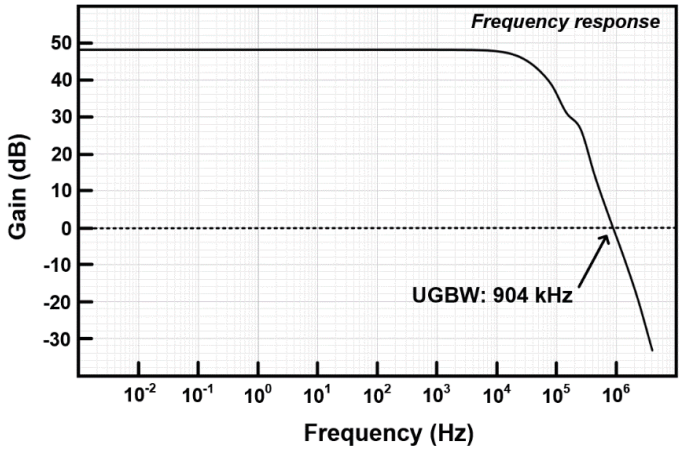

Fig. 6. Simulation result of the UGBW.

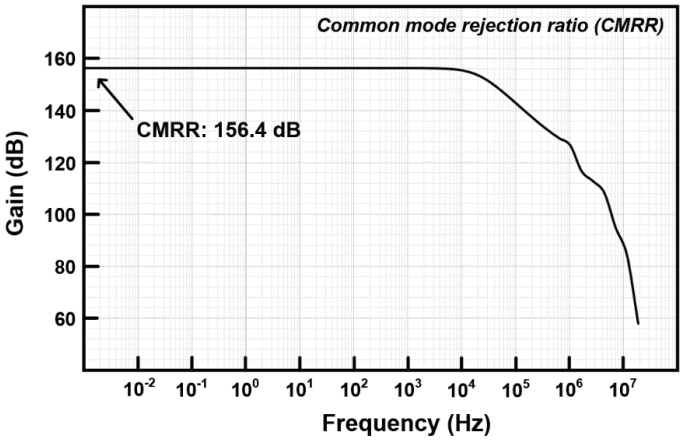

Fig. 7. CMRR simulation result.

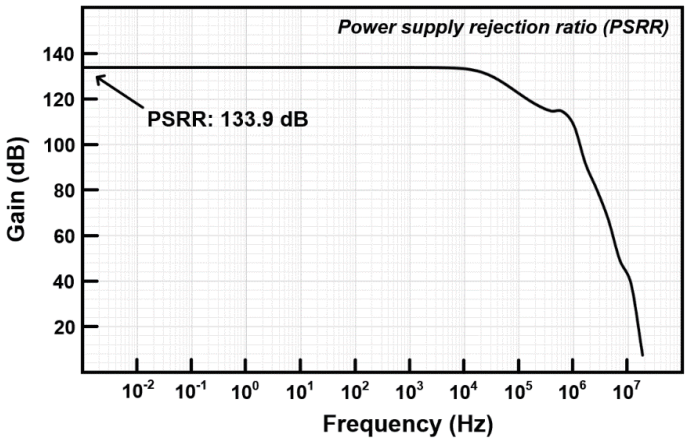

Fig. 8. PSRR simulation result.

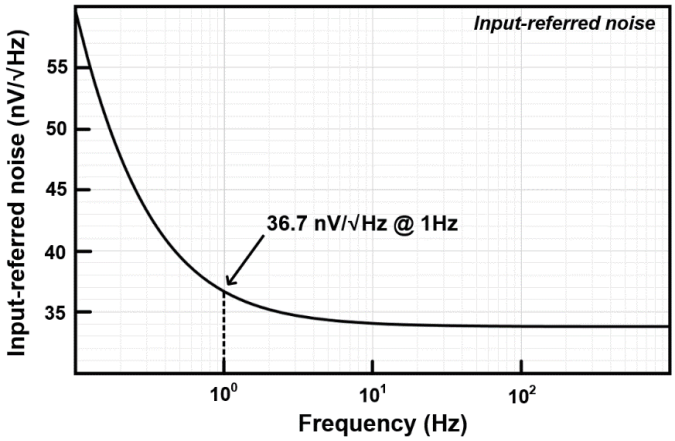

Fig. 9. Input-referred noise simulation result.

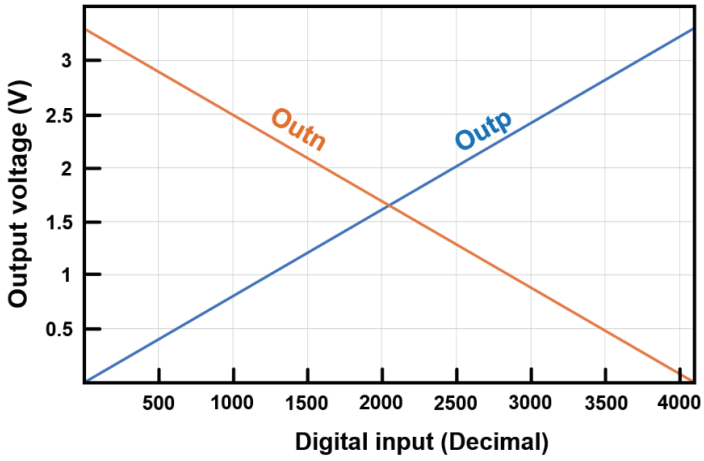

Fig. 10. (Color online) DC offset simulation result of the R-2R DAC.

controlled from −3.3 to 3.3 V. A summary of the performance of the proposed chopper-stabilized multipath IA and a comparison with other studies are shown in Table 1.[10–13]

Table 1
Performance of the proposed chopper-stabilized multipath IA and a comparison with other studies.

Parameter	**This work**	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]
Technology (μm)	**0.18**	0.065	0.5	0.7	0.5
Supply voltage (V)	**3.3**	1	3–5.5	5.5	2.5
Supply current (μA)	**698.6**	12.3	1700	325	61
Input offset voltage (μV)	**2.2**	—	2.8	<2.5	160
Offset calibration technique	**R-2R DAC**	Capacitive trimming	Auto-zeroing	Auto-zeroing	Two-phase clocking
CMRR (dB)	**156.4**	97.5	142	130	110
PSRR (dB)	**133.9**	64	138	114	102
BW (kHz)	**904**	—	800	640	—
Input-referred noise (nV/√Hz)	**36.7**	347.8	27	42	175
NEF*	**34.7**	46.9	43	29.2	52.5

*NEF = $V_{ni}\sqrt{(2 \cdot I_{tot}/\pi \cdot U_T \cdot 4kT \cdot BW)}$.

4. Conclusions

A chopper-stabilized multipath IA with offset voltage compensation using an R-2R DAC was presented. The IA is implemented with a 3-opamp for high input impedance and high linearity. The first stage of the proposed IA is implemented with a chopper-stabilized multipath amplifier with an RRL to achieve low-frequency noise performance and compensate the bandwidth limitation. The second stage is implemented with a chopper-stabilized fully differential amplifier with an RRL. An R-C CMFB and a common-mode output feedback CMFB with an error amplifier in the fully differential amplifier improve the CMRR of the IA. The total gain of the IA can be controlled from 12 to 48.16 dB using programmable resistor arrays. A 12-bit R-2R DAC is used to control the output DC offset of the IA and the offset can be adjusted linearly from −3.3 to 3.3 V. The proposed IA has an input offset voltage of 2.2 μV and an input-referred noise of 36.7 nV/√Hz at a frequency of 1 kHz. The CMRR and PSRR of the IA are 156.4 and 133.9 dB, respectively.

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About the Authors

Hyunwoo Heo received his B.S. degree in electronics engineering from Chungnam National University, Daejeon, Republic of Korea, in 2019, where he is currently pursuing his M.S. degree. His current research interests are in the design of CMOS analog and mixed-mode ICs.

Hyungseup Kim received his B.S. degree in electronics engineering from Chungnam National University, Daejeon, Republic of Korea, in 2014, where he is currently pursuing his Ph.D. degree. His current research interests are in design of sensor interface circuits, biosignal acquisition circuits, secure ICs, data converters, and mixed-mode ICs.

Donggeun You received his B.S. degree in electronics engineering from Chungnam National University, Daejeon, Republic of Korea, in 2019, where he is currently pursuing his M.S. degree. His current research interests are in the design of CMOS analog and mixed-mode ICs.

Yongsu Kwon received his B.S. degree in physics from Chungnam National University, Daejeon, Republic of Korea, in 2019, where he is currently pursuing his M.S. degree in electronics engineering. His current research interests are in design of CMOS analog and mixed-mode ICs.

Dong-il "Dan" Cho received his B.S.M.E. degree from Carnegie-Mellon University, Pittsburg, PA, USA, and his M.S. and Ph.D. degrees from Massachusetts Institute of Technology, Cambridge, MA, USA, in 1980, 1984, and 1988, respectively. From 1987 to 1993, he was an assistant professor at Princeton University, Princeton, NJ. Since 1993, he has been with the Department of Electrical and Computer Engineering, Seoul National University, Seoul, South Korea, where he is currently a professor. He is the author/coauthor of more than 120 international journal articles and the holder/coholder of more than 110 US and Korean patents. Dr. Cho has served on the editorial board of many international journals. He is currently a senior editor of IEEE Journal of Microelectromechanical Systems and International Federation of Automatic Control (IFAC) Mechatronics. He was the president of the Institute of Control, Robotics and Systems (ICROS) in 2017 and is currently vice president of IFAC and the chair of the Technical Board of IFAC. He is an elected senior member of the National Academy of Engineering of Korea.

Hyoungho Ko received his B.S. and Ph.D. degrees in electrical engineering from Seoul National University, Republic of Korea, in 2003 and 2008, respectively. From 2008 to 2010, he worked with Samsung Electronics as a senior engineer. In 2010, he joined the Department of Electronics Engineering at Chungnam National University, Republic of Korea, where he is currently a professor. His current research interests are in the design of CMOS analog and mixed-mode ICs.