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Fabrication and Packaging of Mesa ISFETs

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A novel three-dimensional structure for the ISFET is developed, which simplifies the encapsulation procedure and enables flat packaging. The chemical and electrical characteristics of the ISFET are unchanged by the new structure. The ISFET is encapsulated in a self-aligning process with a Kapton foil by polymer bonding, while at the same time, the source and drain pads are connected to the preprocessed copper leads on the Kapton foil.

1. Introduction

Since 1981, silicon micromachining techniques have successfully been applied for the fabrication of ISFETs of various three-dimensional structures.[1–6] In most cases the geometry is adapted to simplify the encapsulation process. ISFETs with a fully insulated substrate are fabricated using silicon-on-sapphire (SOS) wafers[1] or using silicon-insulator-silicon (SIS) structures[2–4] which are fabricated by anodic bonding of two wafers at least one of which is polished on both sides. The use of these ISFETs facilitates encapsulation but causes some disadvantages in the production process. Wafers that are polished on both sides and SOS wafers are more expensive than normal single-side-polished wafers. Furthermore, gate definition and protection of the bonding wires is not simplified by these structures and thus there is no real advantage in the use of this type of ISFET.

Needle-type ISFETs[5] and back-contact ISFETs[6] have been developed to simplify gate definition as well as wire protection. The problem of gate definition is reduced by enlarging the distance between gate and contact pads or by placing them on opposite sides of the chip. The back-contact ISFETs are well suited for use in flow cells,[7] but are difficult to encapsulate as a dipstick device. Both types of ISFETs have some major drawbacks in

the fabrication process. In particular, photolithography on the structured surfaces is very difficult.

In this paper, a novel three-dimensional ISFET structure, the mesa ISFET, will be introduced. In this structure, the gate area is on top of a large principal mesa, and the contact pads are on small subsidiary mesas on opposite sites of the principal mesa (Fig.1). The height differences simplify the packaging procedure and can be adapted for specific applications. The new structure has the additional advantage that it enables flat packaging, since the gate is no longer in a valley as it is with most of the conventional packaging methods. For the preparation of the mesa, two different etchants have been investigated. A KOH-isopropanol (IPA) etching solution is compared with metal-free tetramethylammonium hydroxide-IPA solution. Drift and sensitivity of both types of ISFETs are compared with those of traditional ISFETs.

Two different methods for packaging the mesa ISFET will be described, i.e., a standard manual procedure and a procedure using Kapton foil with preprocessed copper leads. Ho *et al.*[8] suggested the use of Kapton foil for the encapsulation of ISFETs. This commercially available polyimide foil has excellent properties with respect to its electrical and chemical resistance. However, Ho *et al.* used three layers of Kapton foil that had to be aligned to the chip under a microscope. Conventional wire bonding is not possible in this situation, whereas other methods such as tape automated bonding or controlled collapse connection are more suited for larger numbers of interconnections. Ho *et al.* only briefly discussed the bonding of the electrical contacts and suggested the use of bumps which are interconnected ultrasonically or by thermocompression.

In this work, only one layer of Kapton foil is used. This layer has a hole with the same dimensions as the principal mesa and is placed over the ISFET. The structure of the copper leads makes self-alignment possible. Two alternative interconnection techniques using commercially available materials, i.e., conductive ink and conductive adhesive transfer tape (CATT), have been investigated for application to the mesa ISFET. Polymer bonding[9] with HTR 3-200 is used to adhere the chip to the Kapton foil at the same moment the electrical connections are made. In our original study on polymer bonding, the polymer is applied by a stamping technique. In this work, the polymer is applied at wafer level by the spinning technique and patterned by photolithography.

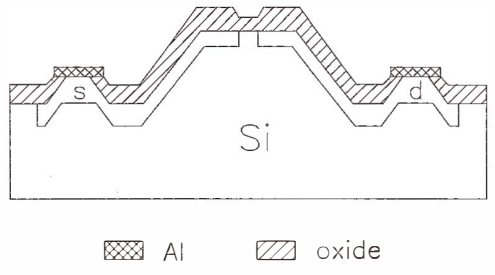

Fig. 1. Cross-sectional view of the mesa ISFET.

2. Experimental

2.1 *Sensor fabrication*

Formation of the mesas is the only additional step in the fabrication process of mesa ISFETs compared with the standard fabrication process of planar ISFETs. The mesas are formed by anisotropic etching in strongly alkaline solutions. Principal mesas with heights of 80 μm and 150 μm were prepared using metal-free and metal-containing etch baths. The process for the fabrication of the mesa structures (Fig. 2) was as follows.

(1) Dry oxidation
(2) Oxide patterning (principal mesa)
(3) Silicon etching (33% KOH-isopropanol (IPA) at 73°C or 25% tetramethylammonium hydroxide (TMAH)-IPA at 75°C)
(4) Dry oxidation
(5) Oxide patterning (principal and subsidiary mesas)
(6) Silicon etching
(7) Oxide removal

As mentioned in the previous section, photolithography on structured surfaces is more difficult than on planar surfaces. Conventional resist will result in coverage failure at the edges of the mesa.[10] Therefore, a photosensitive polyimide (HTR 3-200, OCG Microelec-

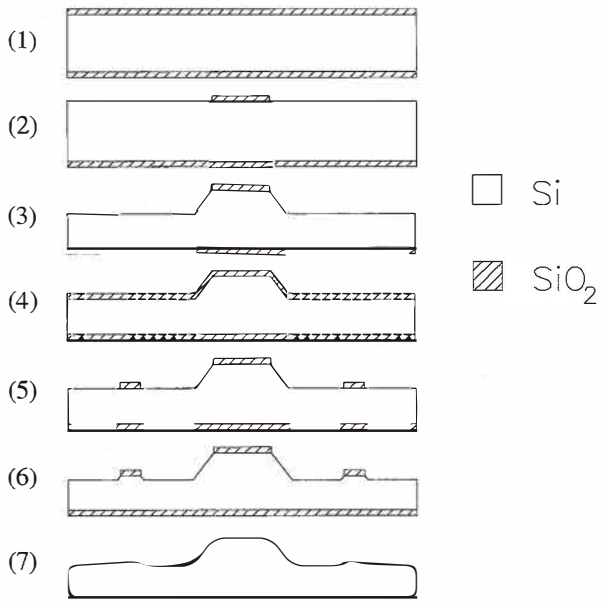

Fig. 2. Schematic drawing of the fabrication of the mesa structures.

tronic Materials) with a high viscosity was used for patterning on the mesa structures. Two layers of polyimide were applied with a total thickness of 15 μm on top of the mesa. After exposure, the layers were developed in HTR D-2 (OCG Microelectronic Materials) and baked at 300°C under reduced pressure. After patterning the underlying layer, the polyimide was removed in Piranha (70% H_2SO_4 (98%), 30% H_2O_2 (40%)). The method with photosensitive polyimide described above was used in every patterning step of ISFET fabrication, except for the definition of the contacts where conventional resist was used.

The process for the fabrication of ISFETs on the mesa structures (Fig. 3) was as follows.

(1) Deposition of boron-doped SiO_2
(2) Patterning of drain/source regions (with HTR 3-200)
(3) Deposition of phosphorus-doped SiO_2
(4) Gate opening (with HTR 3-200)
(5) Gate oxidation and boron and phosphorus diffusion
(6) Evaporation of the tantalum layer (50 nm)
(7) Opening of contact holes (with HTR 3-200)
(8) Oxidation of the tantalum layer to the Ta_2O_5 sensing layer
(9) Evaporation of the aluminum layer
(10) Definition of the contacts (with conventional resist)

Except for the evaporation of the tantalum layer, oxidation of the tantalum layer and evaporation of the aluminum, the wafers etched in TMAH were processed separately from the wafers etched in the KOH solution to prevent cross contamination. Normal (planar) ISFETs were fabricated parallel to the mesa ISFETs using conventional resist for all lithographic steps.

2.2 *Manual encapsulation*

The first, and probably still most frequently used, packaging procedure for ISFETs is manual encapsulation.[11,12] Recently, the benefits of using a polyimide layer as a first protective layer were discussed.[13] This protective layer of polyimide was prepared on the wafer level. A covalent linkage between the polyimide and the oxide surface was achieved by pretreatment of the surface with 3-aminopropyl triethoxysilane (APS). A solution of 0.1 percent APS in methanol water (19:1) was stored in the refrigerator for at least one night and for a maximum of three weeks to obtain a solution of oligomerized APS. The wafers with mesa ISFETs were covered with this solution for 1 min and subsequently rinsed with ethanol and spin dried. Rinsing with ethanol was essential to prevent the formation of thick layers of APS on top of the mesa. A thermal step at 120°C (5 s) was performed to force the condensation reaction to completeness. Next, a layer of photosensitive poly(amic acid) (HTR 3-200) was applied by the spinning technique (3000 rpm, 20 s). After a soft bake at 90°C (20 min) to remove the solvent, the layer was patterned by photolithography. After 40 s of exposure, an intermediate bake at 90°C (5 min) was performed to improve the resolution, followed by development in HTR D-2 and rinsing with isopropanol. Preparation of the polyimide layer was finished by a hard bake at 300°C (1 h) under reduced pressure. During this hard bake, the poly(amic acid) is converted into the final polyimide. The wafers were diced into single chips which were glued on a printed circuit board with

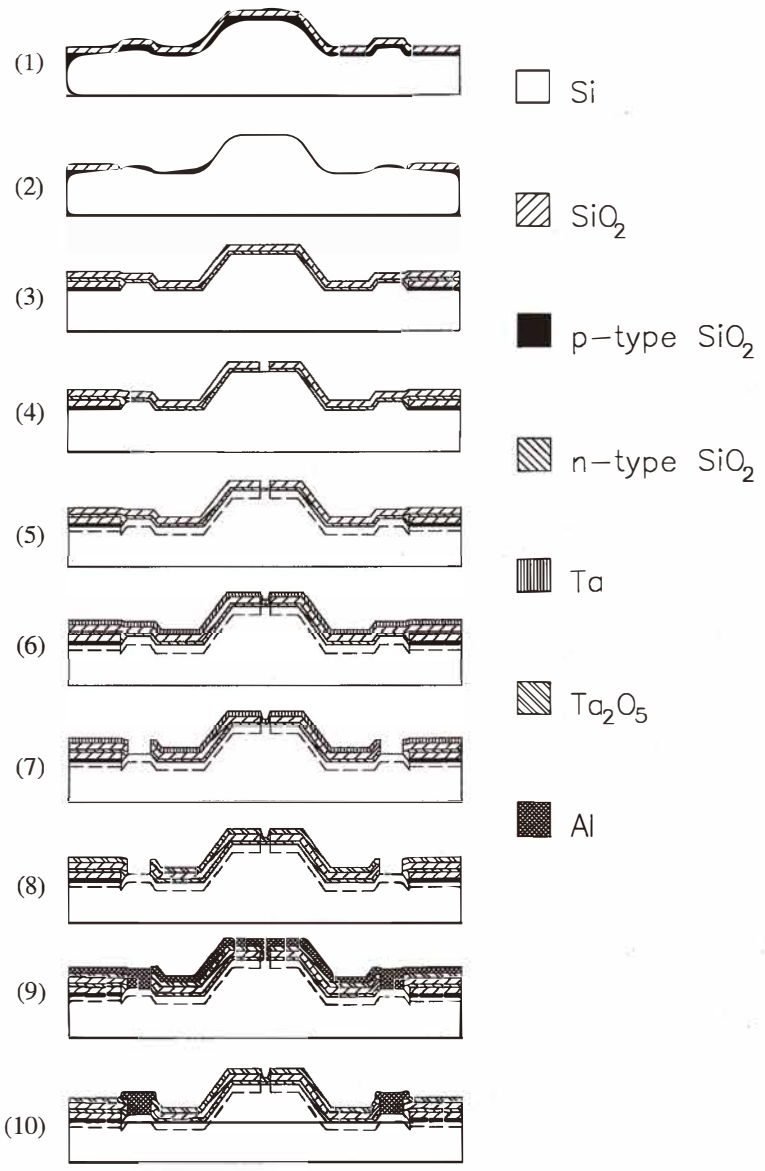

Fig. 3. Schematic drawing of the fabrication of the ISFET on the mesa structures.

the two-component epoxy resin Hysol (Dexter). The prepolymer and the hardener were mixed in a ratio of 4:1 and heated to 50°C for 10 min to start the polymerization reaction. The contact pads were wire bonded to copper strips on the printed circuit board. The lower level of the chip, the bonding wires and the copper strips were manually encapsulated with Hysol. This epoxy resin was poured around the mesa while the gate was easily kept free of epoxy resin due to the difference in height. The encapsulated ISFETs were stored at 50°C overnight to complete polymerization of the epoxy resin.

2.3 *Packaging with foil*

Commercially available 80-μm-thick Kapton foil with a 30-μm-thick copper layer on one side was used for packaging the mesa ISFETs. The copper layers were patterned into two copper tracks with a width of 1 mm. The distance between the ends of the copper tracks was slightly less than the distance between the contact pads, reducing the precision required for self-alignment of the chips. An opening with the dimensions of the mesa was punched in the Kapton foil between the copper tracks.

ISFETs with a poly(amic acid) ring around the mesa were used in this encapsulation procedure. The polymer was covalently linked to the surface oxide with APS. A complete description of the preparation of these layers was given in the previous subsection.

2.3.1 *Packaging of ISFETs using CATT for the interconnections*

The CATT 9703 (Scotch 9703, 3M) contains silver-coated nickel particles that protrude from the foil on both sides and have a diameter of 20–50 μm and a density of about 100 per square mm. The thickness of the tape is approximately 50 μm and both sides of the tape have an adhesive layer. The current flows only perpendicularly through the adhesive tape and not along the plane of the tape. The tape can be applied by a simple process and adheres well to Kapton foil and copper.[14]

Small pieces of CATT were adhered to the ends of the copper tracks on the Kapton foil. After removal of the protective layer from the pieces of CATT, an ISFET or a test structure provided with a ring of poly(amic acid) was placed on the foil, while the mesa was adjusted in the opening in the Kapton foil. The contact pads were automatically aligned above the CATT-covered copper leads (Fig. 4).

The chip was pressed against the foil for 1 h at 300°C in a nitrogen atmosphere. During this process, the interconnections are made and the poly(amic acid) is converted into polyimide which holds the chip and the Kapton foil together. Subsequently, partly prepolymerized epoxy resin (Hysol) was poured on the back of the mesa ISFET and the Kapton foil. No further precautions were taken to prevent contamination of the gate (Fig. 5). The creep behavior of the epoxy resin results in complete coverage of the copper leads, the contact pads and the CATT. Polymerization was completed overnight at 50°C.

2.3.2 *Packaging of ISFETs using conductive ink for the interconnections*

ISFETs and test structures with a ring of poly(amic acid) around the mesa were used. Small drops of the conductive ink (Electrodag 427 SS, Acheson) were manually placed on the contact pads. The conductive ink consists of very finely dispersed silver particles in a thermoplastic resin.[15] The chip was subsequently placed on Kapton foil with the mesa

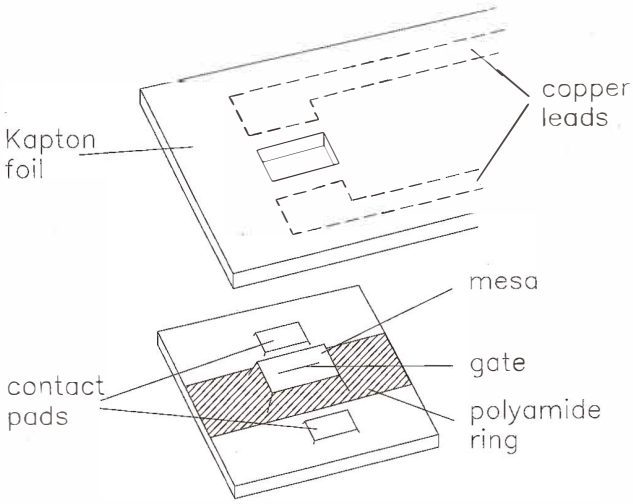

Fig. 4. Alignment of the Kapton foil over the mesa ISFET.

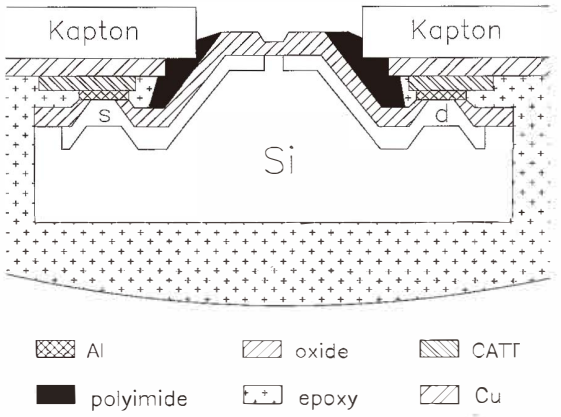

Fig. 5. Cross-sectional view of a fully encapsulated mesa ISFET.

adjusted in the opening of the foil. The contact pads were automatically aligned above the copper leads. The chip was pressed to the foil and heated for about 2 min to 300°C with a soldering iron. The conductive ink was cured and the poly(amic acid) was mostly converted into polyimide during this thermal step. Next, partly prepolymerized epoxy resin (Hysol) was poured on the back of the chip and the foil. The epoxy resin covers the copper leads, the contact pads and the adhesive ink completely due to the creep behavior of the epoxy resin. Polymerization was completed overnight at 50°C.

2.4 *Leakage current measurements*

The leakage current of encapsulated ISFETs was measured 30 min after immersion in a 0.1 M $NaNO_3$ solution. Source and drain were connected together and negatively biased to the solution. The bias voltage of 5 V was generated by a Philips 1542 PE power supply. The leakage current was directly measured by a Keithley 602 Solid State Electrometer.

3. Results and Discussion

3.1 *Electrical characteristics of the mesa ISFETs*

The resistance of source and drain was about 35 Ω in all cases, showing that source and drain diffusion are not interrupted at the foot or at the top of the mesa. The measured resistance is in the same range as the resistance of 60 Ω found for normal planar ISFETs and corresponds to a sheet resistance of 10 Ω/□.

An important parameter for the operation of ISFETs is the threshold voltage, because some oxides (i.e., SiO_2 and Ta_2O_5) will degrade when they are too highly negatively biased to the solution. Without any precautions the ISFETs would be normally off. The channel conductance at zero gate bias is very low and a positive bias voltage is required to obtain properly biased ISFETs. However, with ion implantation or by the creation of more surface states, the threshold voltage can be shifted to the negative direction, resulting in an n-channel at zero bias (ISFET is normally on). The creation of a mesa may influence the threshold voltage because of contamination of the silicon surface and/or surface roughening during the additional etch steps. In general, surface roughening causes more surface states and thus a shift to more negative values. The threshold voltage of the mesa ISFETs were compared with the threshold voltage of planar ISFETs that were prepared parallel to the mesa ISFETs.

The threshold voltage was determined with the help of a MOSFET test structure. From the 'adapted' transfer characteristics (i.e., the square root of the drain current, $\sqrt{I_d}$, versus the gate source voltage, V_{gs}) the threshold voltage could be derived. The measurements were done on wafers using a probe setup. A fully automatic parameter analyzer HP 4145 was connected to supply and measure the current. In Fig. 6 the transfer characteristics of a planar MOSFET and a mesa MOSFET are shown.

In Table 1, the average threshold voltage of at least five MOSFETs of each type are given. The mesa MOSFETs etched in a TMAH-IPA etching solution show a slight shift of the threshold voltage compared with the planar MOSFETs. The shift of the MOSFETs etched in KOH-IPA is much larger. However, the variation in threshold voltage on one wafer is of the same order for planar MOSFETs as for mesa MOSFETs. From these results it can be concluded that the shift of the threshold voltage is caused mainly by contamination of the silicon and the silicon dioxide with potassium ions. Oxidation of the silicon and subsequent removal of this oxide layer, which are necessary for mesa fabrication, have only minor influence on the threshold voltage.

From Fig 6, it can be seen that the slope $\sqrt{I_d}/V_{gs}$ is steeper in the case of the mesa MOSFETs. However, there are large variations in this slope among the mesa MOSFETs of one wafer (Table 1). The steeper slope of all mesa MOSFETs compared to planar MOSFETs is caused by a slightly smaller gate length which in turn is caused by divergence

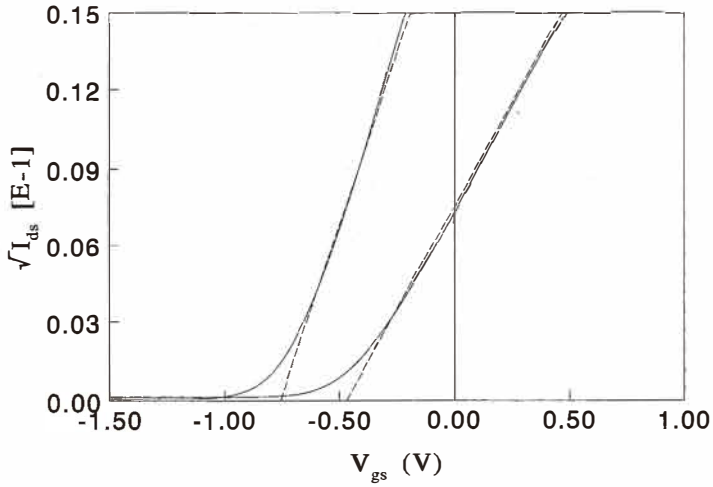

Fig. 6. Transfer characteristics of a planar ISFET (right) and a mesa ISFET (left).

Table 1
Electrical characteristics of MOSFETs.

Height [μm]	Etchant	Threshold voltage [V]	Slope $\sqrt{I_d}$ $-V_{gs}$
Planar	–	-0.50 ± 0.04	16.1 ± 0.1
80	TMAH-IPA	-0.73 ± 0.02	25.7 ± 3.0
150	TMAH-IPA	-0.73 ± 0.04	24.2 ± 1.2
80	KOH-IPA	-0.97 ± 0.06	24.5 ± 2.3
150	KOH-IPA	-1.19 ± 0.06	23.0 ± 1.6

of light during the exposure for gate definition. The steeper slope corresponds to a higher sensitivity of I_d for changes in V_{gs} and would cause a variation in sensitivity. However, the ISFETs are normally measured using a source and drain follower circuit[16] by which sensitivity variations of individual ISFETs are cancelled. Therefore, the smaller gate length is not a disadvantage. The smaller gate length does not cause the shift in the threshold voltage.

3.2 *Chemical characteristics of the mesa ISFETs*

ISFETs that were encapsulated manually were examined to determine their chemical characteristics. The most important parameter of an ISFET is its sensitivity to changes in

the pH of a solution. This sensitivity has been extensively described in terms of the intrinsic buffer capacity and the differential capacitance.[17] There is no reason to expect any difference in sensitivity between planar ISFETs and mesa ISFETs. The sensitivity of the ISFETs was measured using a source and drain follower circuit.[16] The drain source voltage (V_{ds}) was set at 0.5 V, whereas I_d was set at 100 μA. A solution of 40 ml 0.1 M tetrabutylammonium chloride (TBACl) with 0.8 ml of a 0.5 M standard buffer mixture (citric acid, phosphoric acid, acetic acid) was used as the starting solution for titration. The solution was automatically titrated with 0.1 M tetrabutylammonium hydroxide (TBAOH) in 20 steps of about 0.45 pH units each. The total titration time was 2 h.

In Fig. 7, the typical responses of the four types of mesa ISFETs and the planar ISFETs are shown with arbitrary offset. The sensitivities of all ISFETs were close to their theoretical maximum of 59.55 mV/pH (27°C), as summarized in Table 2. The sensitivity of the mesa ISFETs etched in KOH-IPA was slightly lower than those of the other ISFETs. However, this difference was within the usual variation between different wafers.

The drift characteristics were measured in a Faraday cage to prevent electromagnetic influence. The drift measurements were performed in the same setup as was used for the titration. The measurement was started within 5 min after the ISFETs were immersed in the solution. Five hundred measurement points were divided over the total measurement time, in this case 15 h. In Fig. 8, the drift characteristics of all types of ISFETs are shown. The initial drift, i.e., the drift in the first 3 h, was, in all cases, within 5 mV. This value for the initial drift is in agreement with previous results for Ta_2O_5 ISFETs.[R] The small variations in the initial drift are comparable to normal variations between wafers.

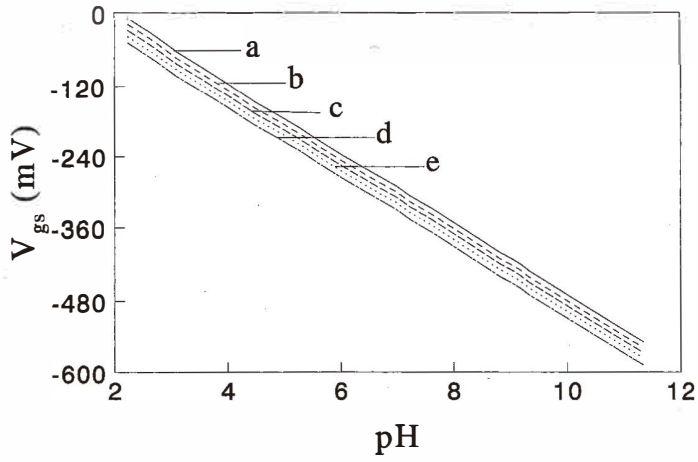

Fig. 7. ISFET pH response of (a) planar ISFET, (b) mesa ISFET (80 μm, TMAH-IPA), (c) mesa ISFET (150 μm, TMAH-IPA), (d) mesa ISFET (80 μm, KOH-IPA), (e) mesa ISFET (150 μm, KOH-IPA).

Table 2
Sensitivity and drift characteristics of ISFETs.

Height [μm]	Etchant	Sensitivity [mV/pH]	Initial drift [mV]	Long-term drift [μV/hr]
Planar	–	–58.9	2.44	10
80	TMAH-IPA	–58.9	3.67	78
150	TMAH-IPA	–58.7	2.44	46
80	KOH-IPA	–58.8	2.68	52
150	KOH-IPA	–58.7	2.19	58

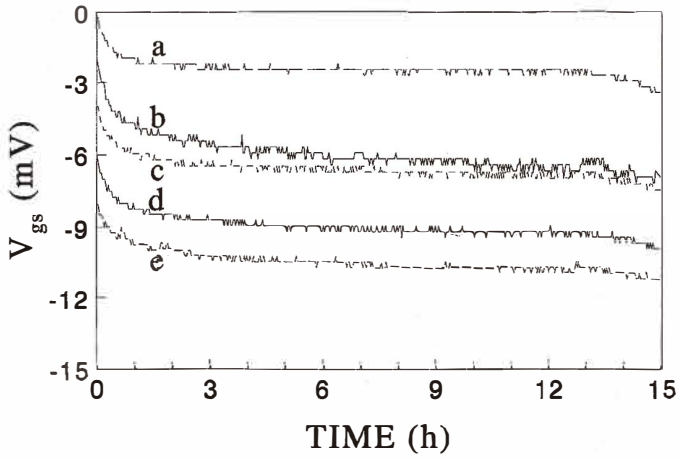

Fig. 8. Drift characteristics of (a) planar ISFET, (b) mesa ISFET (80 μm, TMAH-IPA), (c) mesa ISFET (150 μm, TMAH-IPA), (d) mesa ISFET (80 μm, KOH-IPA), (e) mesa ISFET (150 μm, KOH-IPA).

The long-term drift of all ISFETs was very low, about 0.05 mV/h. The variation between the long-term drifts of different ISFETs is within the variation between different wafers. The drift rates obtained are comparable to the results obtained by Bomer for planar Ta_2O_5 ISFETs.[18] Possible contamination of the mesa ISFET with potassium and/or sodium ions during KOH etching did not affect the drift rate.

3.3 *Manually encapsulated ISFETs*

The manual encapsulation of ISFETs was considerably facilitated by the presence of the mesa structure. The viscosity of the epoxy resin must be high in order to prevent

coverage of the mesa. All mesa ISFETs having an intermediate layer of polyimide showed a low leakage current (below 1 nA) during the entire test lasting 24 h and were not tested further to determine their lifetime. Planar ISFETs encapsulated according to this procedure had a lifetime of at least 4 – 5 months. The use of a polyimide layer is required to reduce the stress caused by shrinkage of the epoxy resin and/or the absorption of water by the epoxy resin.[15] The cured epoxy resin is in the glassy state, which implies that it is hard and rigid and unable to reduce stress. The glass transformation temperature of polyimide is far below room temperature, which means that polyimide is in the rubber state. Polyimide in the rubber state has a high flexibility which enables the accommodation of stress. Furthermore, the polyimide is linked to the oxide surface by covalent bonding which is stronger than binding by electrostatic interactions or hydrogen bonding which occurs in the case of an epoxy resin-oxide interface. Residual amino acid groups of the polyimide can act as a local hardener for the epoxy resin and the so-formed covalent bonds in combination with entanglement of the two polymers can explain the very strong binding between polyimide and epoxy resin.

3.4 *ISFETs encapsulated with foil*

The test structures without channels and with a poly(amic acid) ring around the mesa that were bonded with CATT 9703 gave good results in all aspects. The contact resistance between the aluminum contact pads and the copper leads was on the order of 1 Ω and was unaffected by vibrations and shocks. During baking, the poly(amic acid) layer is converted into polyimide and the layer thickness is reduced to 70 percent of its original value. The good stability can be explained by the good adhesion strength between the polyimide and the Kapton foil, which is also a polyimide. The nature of the adhesion was not investigated, but might be entanglement of polymer chains or formation of covalent bonds. The high bond strength was confirmed by the tape pull test. None of the four chips tested could be removed from the Kapton foil in this rigid test and the contact resistance was the same as before the pull test. The epoxy resin could be poured out on the back of the ISFET without any special precautions. The polyimide ring around the mesa prevented contamination of the gate area during epoxy encapsulation of the back. The leakage current of ISFETs encapsulated in this manner was 0.1 nA or lower. These values are below the value of 2 nA that is generally taken as the upper limit for an acceptable leakage current.[19]

In the experiments using conductive ink, accurate placement of the small drops of conductive ink on the contact pads required some practice. The ink tends to flow from the contact pads. Good results were obtained when a polyimide ring was used around the mesa. The contact resistance was about 1 Ω and the mechanical strength was high. No variations could be measured in the contact resistance. The chips could not be removed from the foil in a tape pull test, due to the good adhesion properties of the polyimide. The gate was not contaminated with the epoxy resin (Hysol) that was poured on the back of the chip and the foil. Here, fully encapsulated ISFETs also showed leakage currents below 0.1 nA.

4. Conclusions

The novel ISFET with a three-dimensional mesa structure shows good electrical characteristics which are unaffected by the fabrication process of the mesa, although the threshold voltage is shifted slightly to more negative values. The sensitivity of the ISFET is not influenced by the mesa structure. The drift rates are independent of the etching solution and were not affected by the mesa structure.

The manual encapsulation procedure for these mesa ISFETs is simpler than that for planar ISFETs. In particular, the definition of the gate area is easier due to the difference in height between this area and the contact pads. The use of an intermediate polyimide layer is required to reduce the stress in the epoxy resin-substrate interface caused by shrinkage of the epoxy resin during the polymerization.

Packaging of the mesa ISFET with Kapton foil is a very simple process due to the self-alignment procedure. Polymer bonding can be used to adhere the ISFET chip to the Kapton foil. During the hard bake step required for polymer bonding, the CATT or ink interconnections can be made. The use of CATT is the easiest method. Further encapsulation of the back of the chip and of the copper leads with epoxy resin is facilitated by the presence of the polyimide ring around the mesa, which prevents contamination of the gate area. For all encapsulated mesa ISFETs, leakage currents below the maximum acceptable level were obtained. None of the encapsulated ISFETs failed during their testing procedure which lasted 24 h. However, more measurements are required to determine the lifetime of the encapsulation using Kapton foil.

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