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Rapid Thermal Annealing of Doped Silicon Films to Relax Intrinsic Stress

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The effect of rapid thermal annealing (RTA) on intrinsic mechanical stress in doped silicon films has been investigated. Film stress was evaluated by means of comparative wafer curvature measurements. We present results for boron- and arsenic-doped films deposited as amorphous and polycrystalline layers, respectively. The thermal budgets necessary to achieve low-stress silicon films were reduced by a factor of 100 compared to those for conventional furnace processing and are now compatible with those of current very large-scale integration (VLSI) processing.

1. Introduction

Besides its well-known applications in very large-scale integration (VLSI) technology,[1–3] polycrystalline silicon is increasingly used as a structural layer in surface micromachining.[4–7] Free-standing structures for capacitive and piezoresistive sensors are fabricated by lateral etching of a sacrificial layer (*e.g.*, silicon oxide) underneath the structural layer (*e.g.*, polycrystalline silicon). As-deposited polycrystalline silicon films generally show compressive stress after deposition.[8,9] This compressive stress leads to buckling of free-standing structures such as membranes and bridges (Fig. 1) after sacrificial layer etching.

In most micromachining applications, buckling is unacceptable. Especially for capacitive sensors, straight structures with an initially constant electrode spacing are necessary (Fig. 2). This can only be achieved by using stress-free structural layers or layers with

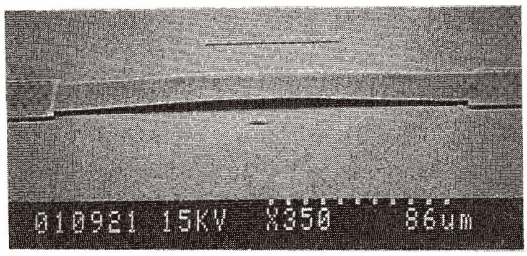

Fig. 1. Buckled bridge, fabricated using as-deposited polycrystalline silicon.

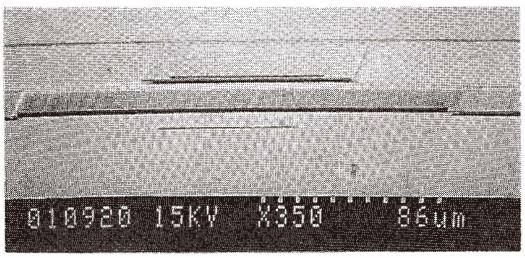

Fig. 2. Straight free-standing bridge, fabricated using RTA stress-annealed silicon.

tensile stress. There are various methods of obtaining the desired stress states.

Stress compensation can be achieved by forming sandwich structures consisting of layers with opposite stress orientation.[10,11] However, this approach might lead to process complications and problems with different thermal expansion coefficients.

The influence of intrinsic film stress can be reduced by stress-compensating sensor design. Structures such as folded beams are applied to allow stress relaxation without buckling[12] but can only be used for certain applications.

Finally, long furnace annealing time has been proven to reduce intrinsic film stress and even to convert it to tensile stress.[13]

However, full integration of micromechanical structures into a complementary metal-oxide-semiconductor (CMOS) process[14,15] does not allow stress reduction by means of furnace annealing. The corresponding thermal budgets are much higher than those applicable in VLSI processing, thus preventing stress annealing within a submicron process. To realize full integration of micromechanical structures it is necessary to achieve stress relaxation at much lower thermal budgets.

Although rapid thermal annealing (RTA) increasingly substitutes furnace annealing in advanced CMOS processes, little is known about the influence of RTA on intrinsic film stress in polycrystalline silicon layers. To investigate this influence, stress measurements were carried out for arsenic- and boron-doped films.

The results indicated that RTA is an appropriate means of VLSI-compatible stress

annealing in polycrystalline silicon, thus enabling full integration of micromechanical processing into current VLSI processes.

Although the absolute intrinsic film stress depends on the exact deposition conditions of polycrystalline films, similarities in the general annealing behavior of thin silicon films are observed. Consequently, the results obtained here are valid not only for one type of reactor-specific polycrystalline silicon, but are of general use for stress annealing in polycrystalline silicon films.

2. Experimental Procedure

2.1 *Sample preparation*

The substrates used in our experiments were 6-inch Si (100), Czochralski-grown (CZ), p-type wafers. To obtain realistic surface micromachining conditions, the wafers were covered with a 1-μm-thick oxide layer by chemical vapor deposition (CVD). Subsequently, the silicon films were deposited in a standard hot-wall reactor. On the first set of wafers (set 1) silicon films were deposited at 625°C. Transmission electron microscopy (TEM) analysis showed that these deposition conditions result in a polycrystalline film structure with columnar grains.

To investigate the influence of the initial film structure on the annealing behavior, silicon films were deposited on a second set of wafers (set 2) at 560°C, resulting in an amorphous structure. Both the amorphous and polycrystalline films were boron doped by ion implantation at a dose of 4×10^{16} cm^{-2} and an implantation energy of 30 keV, resulting in a dopant concentration of 4×10^{20} cm^{-3} after annealing.

In order to compare films with oppositely charged dopants, polycrystalline silicon films on a third set of wafers (set 3) were implanted with arsenic at the same implantation dose as above.

To avoid dopant evaporation during RTA the doped silicon films were covered with a low-temperature oxide. This oxide cover was removed by wet etching in buffered hydrofluoric acid after the RTA step, and before the first curvature measurement.

2.2 *Rapid thermal annealing*

RTA was performed in N_2 ambient. Warm-up in the annealing process was conducted by preheating at 800°C for 20 s followed by ramping to the final temperature at a rate of 50°C/s. The peak temperatures ranged from 950°C to 1100°C. The temperatures referred to below are the peak temperatures of the RTA step. The annealing times given in the plots do not include the 20 s plateau at 800°C. Annealing times in the experiments ranged from 5 s to 160 s.

2.3 *Stress determination*

Due to mechanical stress in the oxide and silicon films, the wafers showed concave and convex curvatures, respectively. After RTA, this curvature was measured using a capacitive flexure gauge.

In order to separate the contributions of oxide film stress and silicon film stress, the polycrystalline silicon layer was removed by dry etching after the first curvature measure-

ment, and wafer curvature was measured again. The comparative measurement allowed calculation of the contribution to the stress from the polycrystalline silicon film only.

The residual stress was calculated from the difference in wafer curvature before and after the removal of the silicon film, given by[16]

$$\sigma = \frac{E_S}{6(1-\nu_S)} \frac{t_S^2}{t_{film}} \left(\frac{1}{R_{S2}} - \frac{1}{R_{S1}} \right),$$

where σ is the residual film stress, E_S is Young's modulus for the substrate, ν_S is Poisson's ratio for the substrate, t_S is the thickness of the substrate, t_{film} is the thickness of the film, and R_{S1} and R_{S2} are the radii of wafer curvature before and after film removal, respectively.

The parameters in the above equation are

$$\frac{E_S}{(1-\nu_S)} = 180 \text{ GPa for a <100> silicon substrate,}$$

$$t_S = 635\ \mu\text{m} \qquad \text{and} \qquad t_{film} = 1\ \mu\text{m}.$$

The resolution of the deflection measurement is 100 nm which corresponds to a stress resolution of 1 MPa.

3. Results

Measurements of the unannealed silicon layers revealed that the applied deposition processes for polycrystalline and amorphous silicon produce layers with low compressive stresses of roughly −200 MPa for the boron-implanted films and −100 MPa for the arsenic-doped films.

The effect of RTA on the film stress varied with the initial film structure and the type of dopant.

3.1 *Polycrystalline deposition with boron doping (set 1)*

In Fig. 3, the stress relaxation characteristics of a polycrystalline silicon layer deposited at 625°C are shown.

The plot clearly shows the efficiency of RTA for stress annealing. The thermal budgets, which were very low compared to those for a furnace annealing process, resulted in substantial stress relaxation in the polycrystalline layer. A thermal budget as low as 1100°C for 10 s, which is common in submicron VLSI processing, reduced the residual compressive stress to about 15% of its initial value.

Our measurements show that stress relaxation strongly depends on the annealing temperature. To obtain satisfactory stress reduction within the annealing times common to VLSI processing, temperatures should exceed 1000°C.

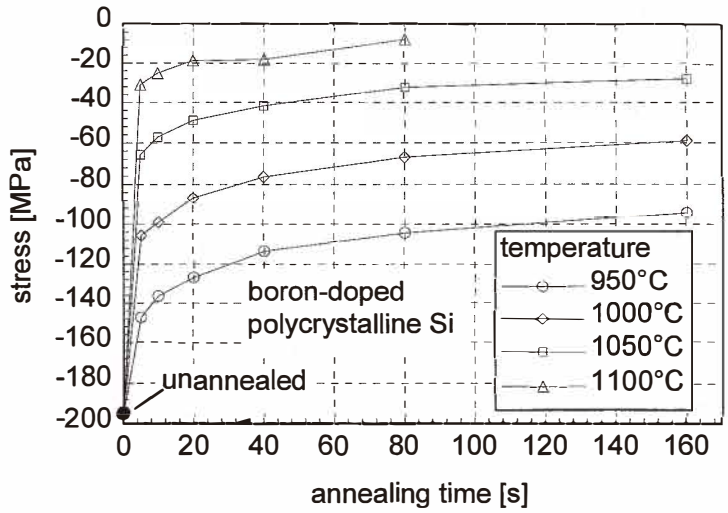

Fig. 3. Stress relaxation characteristics for a 1-μm-thick boron-doped polycrystalline silicon layer annealed by RTA.

3.2 *Polycrystalline deposition with arsenic doping (set 2)*

Figure 4 shows the stress relaxation characteristics of arsenic-doped polycrystalline films. In contrast to the boron-doped films, two phases of stress annealing can be distinguished. In the first phase, we observed a conversion from compressive stress in the polycrystalline silicon layer to a peak tensile stress of about 50 MPa.

This conversion is important because layers with a low tensile stress are highly desirable for many surface micromachining applications such as pressure membranes and resonant bridge structures.

In the second phase, the tensile stress resulting from phase 1 was reduced, producing almost stress-free layers.

The time necessary to reach the peak tensile stress strongly depends on the annealing temperature. At a temperature of 1100°C the peak stress level was reached after 5 s of annealing, whereas at a temperature of 950°C, a duration of 160 s was insufficient to reach the maximum tensile stress.

3.3 *Amorphous deposition with boron doping (set 3)*

Stress conversion from compressive stress to tensile stress becomes more evident in the annealing curves for amorphous silicon layers.

To illustrate the reduction of the thermal budget by a factor of 100 by means of RTA the annealing curves for amorphous silicon in a conventional furnace process[13] are shown in Fig. 5(a). Figure 5(b) shows the stress annealing curves for amorphous, boron-doped silicon layers obtained by RTA. The time scale is much smaller than that for the furnace

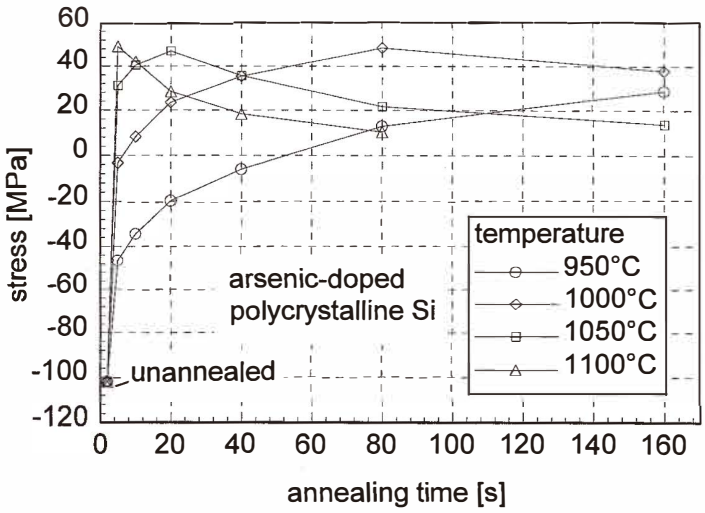

Fig. 4. Stress relaxation curves for a 1-μm-thick arsenic-doped polycrystalline silicon layer annealed by RTA.

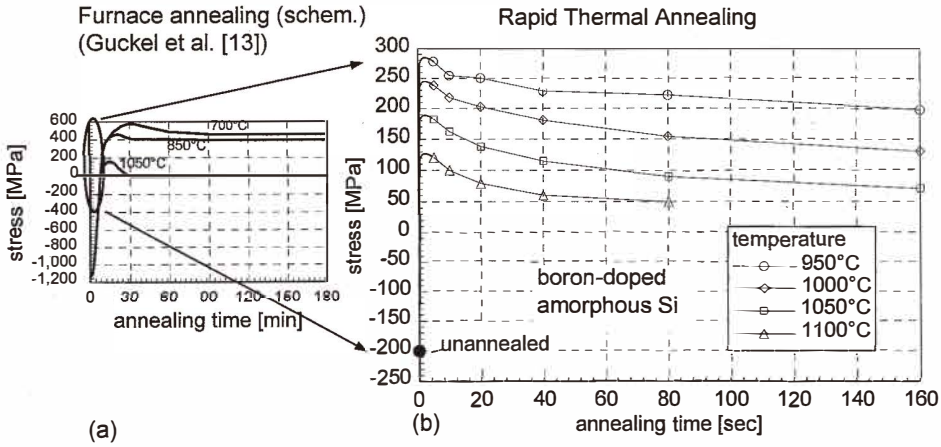

Fig. 5. (a) Annealing curves for amorphous silicon during furnace annealing (Guckel *et al.*[13]). (b) Stress relaxation of boron-doped amorphous silicon annealed by RTA.

annealing process. The annealing curves show that stress conversion in amorphous films takes place for extremely low thermal budgets. For all annealing temperatures the peak level of tensile stress was reached or exceeded after 5 s of stress annealing. Further

annealing reduced the tensile stress. The measured stress conversion corresponds well with results of investigations carried out by Guckel *et al.*[13] on amorphous silicon films undergoing furnace annealing (Fig. 5(a)). Annealing times for the RTA process are a factor of 100 lower than those for the furnace annealing process.

4. Discussion

4.1 *Intrinsic stress in as-deposited silicon films*

In agreement with the observations of other authors,[8,9] our measurements show compressive stress in the unannealed films. The measured compressive stress values of −200 MPa for the boron-doped films and −100 MPa for the arsenic-doped films are higher than the values expected from the consideration of the different thermal expansion coefficients of polycrystalline and monocrystalline silicon.[17,18] Therefore, other stress-inducing mechanisms must be operating.

One possible reason for the initial stress is grain growth effects during film deposition, which result in a columnar structure in the polycrystalline films. In the deposition process, gases such as hydrogen and oxygen are trapped in the silicon film and may contribute to the intrinsic stress. The different initial stress values for arsenic- and boron-doped polycrystalline films indicate that implantation amorphization also influences the film stress.

4.2 *Stress relaxation behavior*

Stress relaxation takes place in two phases. In phase 1 the initial compressive stress is reduced (set 1) or converted to tensile stress (sets 2 and 3) with a small time constant. For amorphous deposited films the time constant for stress conversion is less than 5 s.

In phase 2 the remaining intrinsic film stress is reduced with a larger time constant which depends on the annealing temperature. To explain the stress-annealing behavior in phase 1 we must take into account the following relaxation mechanisms:

— crystallization of initially amorphous film regions,
— grain growth effects,
— annealing of crystal defects,
— evaporation of gases trapped in the films during deposition.[19]

All of these effects result in an immediate volume shrinkage of the silicon layer, thus reducing the compressive stress, and in the cases of arsenic-doped polycrystalline and boron-doped amorphous films, converting it to tensile stress.

In the boron-doped polycrystalline films, grain growth effects are less pronounced than in the arsenic-doped films.[20] Thus, structural changes reduce the residual compressive stress, but are insufficient to cause tensile stress.

For stress conversion in the boron-doped amorphous films, crystallization and degassing of trapped hydrogen and oxygen are reasonable mechanisms. Secondary ion mass spectroscopy (SIMS) analysis revealed that the concentration of trapped gases in amorphous silicon films is two orders of magnitude higher than that in polycrystalline films. After RTA, the oxygen concentration in the crystallized amorphous film was the same as that in the polycrystalline deposited films.

The arsenic-doped films were deposited at 625°C as polycrystalline layers. The longer

annealing times necessary for stress conversion and the low concentration of trapped gases indicate that grain growth effects and the crystallization of amorphous regions in the polycrystalline film are reasonable explanations for stress conversion in the arsenic-doped films.

As revealed by TEM analyses, grain growth is enhanced by the high arsenic concentration in the polycrystalline films. TEM micrographs show the increased grain size in the upper region of the RTA-treated film (Fig. 6) compared to that in an unannealed polycrystalline film (Fig. 7).

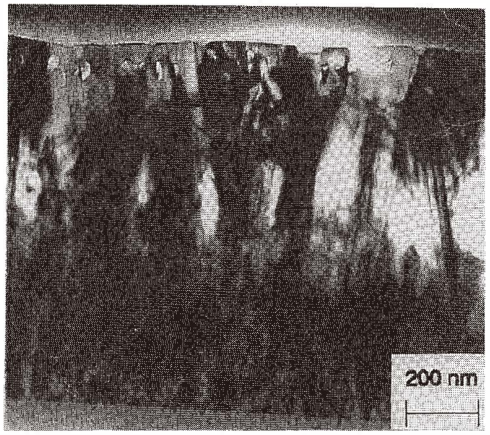

Fig. 6. TEM micrograph of an arsenic-doped polycrystalline layer, stress annealed at 1000°C for 80 s.

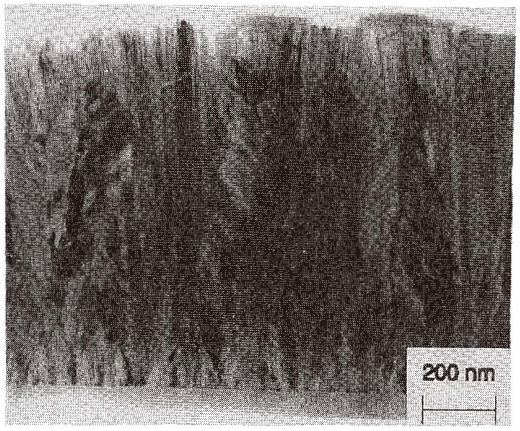

Fig. 7. TEM micrograph of an unannealed polycrystalline silicon layer.

Grain growth is a thermally activated process, because it is related to silicon self-diffusion. Therefore, the time needed to reach maximum tensile stress in the arsenic-doped films decreases with increasing temperature. After reaching the maximum tensile stress, stress relaxation via plastic deformation of the polycrystalline silicon layer occurs.

Shear stress between grains in the polycrystalline film can lead to grain boundary sliding. Dislocations act as sources and sinks for point defects and therefore affect the overall stress. The motion of dislocations and their subsequent recombination at grain boundaries and at the film surface also contribute to the observed plastic behavior. Finally, the substitutional dopant elements cause lattice deformation and therefore intrinsic stress.

5. Conclusions

The annealing behavior of doped polycrystalline and amorphous silicon films has been investigated. The observed stress relaxation curves for RTA are similar in shape to those for furnace annealing. In the initial annealing phase the compressive stress of the as-deposited film is reduced or converted to tensile stress. Subsequently, relaxation of the remaining residual stress is observed, which strongly depends on the annealing temperature.

However, the entire annealing process takes place on a time scale which is about 100 times shorter than that for conventional furnace annealing. Thus, considerable stress relaxation as well as stress conversion to tensile stress could be achieved by means of RTA with VLSI-compatible thermal budgets, and an essential requirement for complete integration of micromechanical structures into the VLSI process environment could be met.

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