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Porous Silicon Technology for Thermal Sensors

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Porous silicon as a tool for the structuring of thermal sensors is presented. The special requirements of thermal structures are discussed and microstructuring techniques are reviewed. Then the technology of porous silicon and its etch and etch stop techniques are described. Examples of thermal sensor applications of porous silicon technology are given.

1. Introduction

Thermal sensing is one of the most important issues in measurement technology. A large number of thermal transducers have been developed and are being produced. For those fabricated by silicon micromachining, anisotropic etching is conventionally used to perform the microstructuring. This method is now a well-established industrial process. It has many advantages, but also some severe drawbacks which make it worthwhile to investigate alternatives. A technique which seems to be especially suited to the fabrication of thermal transducers is microstructuring with porous silicon as a sacrificial layer. In this technique, part of the wafer is transformed from monocrystalline silicon to porous silicon by electrochemical etching. Then thin films are deposited on top of the porous silicon, and the sensor structures are realized. At the end of the process, the porous film is removed. Two features make this technology particularly interesting in relation to thermal transducers. First, the gaps structured with porous silicon are relatively wide ($\approx 100\ \mu$m). Such wide gaps are necessary in order to obtain good thermal isolation of the sensor structure from the bulk silicon and to obtain a device with high sensitivity. The other feature is that

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membranes made of insulators such as silicon nitride which are very well suited for the support of thermal sensors, can be formed easily.

In this paper, first the fundamental thermodynamics of microstructures are discussed with special consideration of the consequences for sensor structures and technology. Then, with the special needs of thermal sensors in mind, microstructuring techniques are reviewed. Porous silicon technology is discussed, and finally we present actual examples of thermal sensors realized by means of porous silicon technology.

2. Basic Concepts of Thermal Sensors

In a thermal sensor, a physical quantity is measured by determining the temperature change it induces in the sensor structure, which is often a thin membrane as used in thin-film thermopile radiation sensors. The measured effect delivers a certain amount of power ΔP to the sensor area; this generates a temperature difference ΔT, which induces a voltage ΔU either due to the thermoelectric effect (thermopile principle) or the voltage drop across a resistor (bolometer principle). A linear approximation of this is described by the following equations.

$$U = c \times \Delta T \tag{1}$$

$$T = 1/K \times \Delta P \tag{2}$$

The first constant c characterizes the efficiency of the thermoelectric conversion, which must be as high as possible to obtain high sensitivity of the device. The second coefficient K is the generalized thermal conductivity which characterizes the device as a whole, not a certain material. For high sensitivity, the thermal conductivity must be small. The sensor area must be thermally isolated, so that low power generates a high temperature difference and a large measurement sensitivity. The main problem in the construction of thermal sensors is the realization of structures with good thermal isolation. Figure 1 shows a schematic of the thermal management of a sensor structure. The main mechanisms by which a sensor gains or loses heat are joule heating, thermal conduction in the membrane, wall heat transfer from the membrane to the surrounding gas, and radiation. There may be other important mechanisms for specific sensor applications, such as chemical heat in the case of pellistors. At room temperature, radiation loss is usually negligible. Therefore, the minimization of two of the mechanisms must be investigated: conduction and wall heat transfer.

Conduction through the membrane, bridge, cantilever or other structure which supports the sensor area mechanically is dependent on the geometry and the thermal conductivity of the material. Silicon has a thermal conductivity k in the region of $k = 150$ W/mK. Thin-film insulators are far less conductive; for example, silicon nitride has $k = 2.25$ W/mK. Silicon oxide and amorphous silicon carbide have k values of the same order of magnitude as nitride. For this reason, thermal sensors are mainly based on free-standing membranes of silicon nitride or other insulators. This has an important impact on technology: while pressure sensors have silicon membranes which are a few μm thick and comparatively

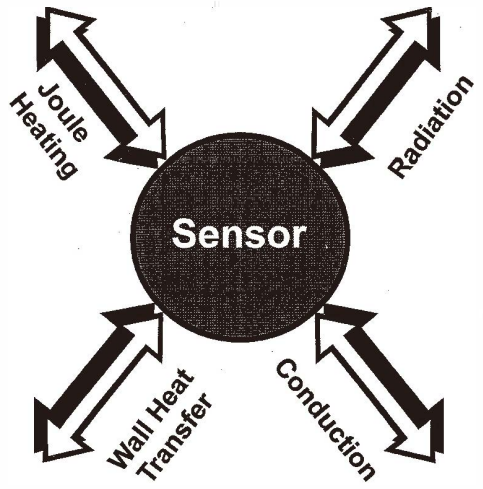

Fig. 1. The main heat flow mechanisms of a sensor.

robust, thermal sensors have very thin membranes (thinner than 1 μm) which are rather difficult to handle without breaking. Furthermore, the silicon membranes of mechanical sensors are monocrystalline and have no internal stresses, but nitride membranes are deposited films. They may exhibit high internal stress which must be taken into account. A typical layer used for this purpose is low pressure chemical vapor deposition (LPCVD) silicon nitride with a thickness of 300 nm. To evaluate the quantities involved, we assume a typical square membrane with a side length of 1000 μm and obtain[1–3] a thermal loss due to conduction of $K_{\mathrm{cond}} = \Delta U / \Delta T = 10\ \mu\mathrm{W/K}$.

Wall heat transfer is the transfer of energy from the membrane to the surrounding air. It is characterized by the wall heat transfer coefficient α. This coefficient depends on the geometry, the temperature, the distance to the closest heatsink and the surrounding gas. The wall heat transfer is normally determined by semiempiric formulae based on experimental results and theory.[1,4] The application of these formulae to microstructures has been investigated.[2] When the distance to the closest heatsink is small, the heat transfer is represented as heat conduction in the gap. This representation is used if the thermal conductivity of the gas is to be measured by thermal conductivity gas sensors or by vacuum sensors. If good thermal isolation is required, heatsinks near the membrane must be avoided. For infinite distance from the closest heatsink, the heat transfer coefficient is evaluated using a free convection approach. In our example, the numerical value is α = 130 W/m^{2}K. The heat loss by wall heat transfer is $K_{\mathrm{trans}} = 110\ \mu\mathrm{W/K}$. Thermal flow through the air is much larger than the flow through the membrane, a situation which is typical for sensors on thin-film insulating membranes.

Infinite distance to a heatsink is not possible, of course. Therefore, we must discuss how far away the heatsink must be in order to achieve sufficient isolation. Convection

experiments show that, if the distance is greater than the thickness of the thermal boundary layer of the heated structure, increasing the distrance further does not affect the transfer. This is demonstrated by an experiment, the results of which are shown in Fig. 2. All details of this experiment are given in ref. 2. A membrane is placed in front of a heatsink at a variable distance. The thermal transfer from the front of the membrane is plotted vs the distance. The experimental data are corrected for conduction and heat transfer from the other side of the membrane. For long distances (case A in Fig. 2), the transfer is constant and can be represented by a wall heat transfer coefficient. For short distances, the transfer is represented by conduction in the air layer (case B). The theoretical thickness of the thermal boundary layer is 160 μm. In this region, the heat transfer can be represented by an interpolation formula (case C). This experiment shows that a free-standing membrane needs sufficient space around it to provide efficient thermal isolation.

The consideration above leads to three guidelines for thermal sensors.

1. In air, thermal conductivity as low as $K = 100$ μW/K can be realized.
2. The heat transfer to air is greater than the thermal conduction within the membrane.
3. The distance between the membrane and the nearest heatsink should exceed the thickness of the thermal boundary layer, which is in the range of 50 μm to 200 μm for microstructures.

With these guidelines in mind, we discuss different techniques for microstructuring thermal sensors.

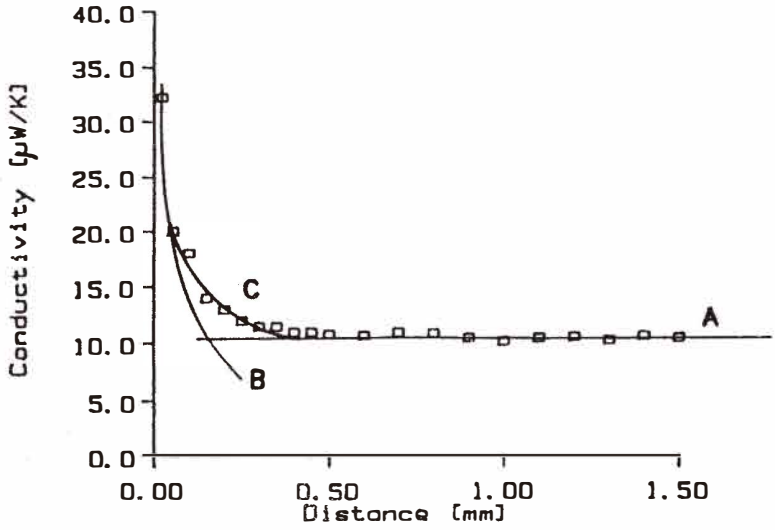

Fig. 2. The thermal boundary layer: heat transfer from a heated membrane to a heatsink at distance d. The thickness of the thermal boundary layer in this case is 160 μm. A: At distances greater than the thermal boundary layer thickness, the transfer is represented by a wall heat transfer coefficient. B: If d is small compared to the thermal boundary layer thickness, the transfer is described as conduction in air in the gap. C: Between these two cases, an interpolation formula is used.

3. Microstructuring of Thermal Sensors

The basic structure of a thermal transducer is free-standing and supports the sensor area. Several micromachining methods can be used to build such structures.

3.1 *Anisotropic etching*

Anisotropic etching, mostly performed using KOH solution, is the most common method for microstructuring.[5,6] Currently, there are two types of silicon micromechanical sensor which are produced and sold in very large numbers: the pressure sensor and the thermopile radiation sensor. Both are fabricated using anisotropic etching. The basic structures of these sensors are shown in Fig. 3(a). This method has numerous advantages.

- It is well understood; industrial processes are reliable and state of the art.
- It provides exact geometries, which are given by the crystal planes of the silicon.
- The cost of the etching equipment is low.
- Integration of CMOS electronics and anisotropically etched sensors on one chip is possible. This has been demonstrated in several devices.[7,8] These devices are realized by performing the CMOS process first, and then the microstructuring as a process outside the CMOS line.

On the other hand, this method has a number of serious drawbacks.

- The slopes of the crystal planes shown in Fig. 3(a) require considerable space on the chip, but sensors must be small to fit as many of them as possible on one wafer. This problem becomes greater with increasing wafer size and thickness.
- The process involves double-sided lithography which requires expensive, special equipment.
- KOH is not CMOS-compatible. Therefore, only part of the process may be performed in a CMOS line.
- Although the equipment for wet-chemical etching is cheap, the process is time-consuming, and therefore, etching is an expensive process.
- The long etching time often causes problems with the masking layers.
- Design freedom is limited by the crystallographic structure.
- Two etch stop techniques are common: electrochemical, which requires complicated contact structures, and p^+ etch stopping, which is only possible for highly doped materials.

KOH etching can also be performed from the front.[9] The structures are cantilevers, which are freed by underetching. However, the remaining problems are severe enough to warrant development of alternative methods.

3.2 *Surface micromachining*

This technology[10,11] involves a sacrificial layer, on which a structure layer is deposited. When the sacrificial layer is removed, the structure layer is freed, as shown in Fig. 3(b). The sacrificial layer is generally silicon oxide, in which a gap several μm thick can be formed. The structure layer is generally polysilicon. Surface micromachining is applied for mechanical sensors, especially for accelerometers.[12] This method is very powerful; small structures can be fabricated, and the method allows freedom in design. Furthermore,

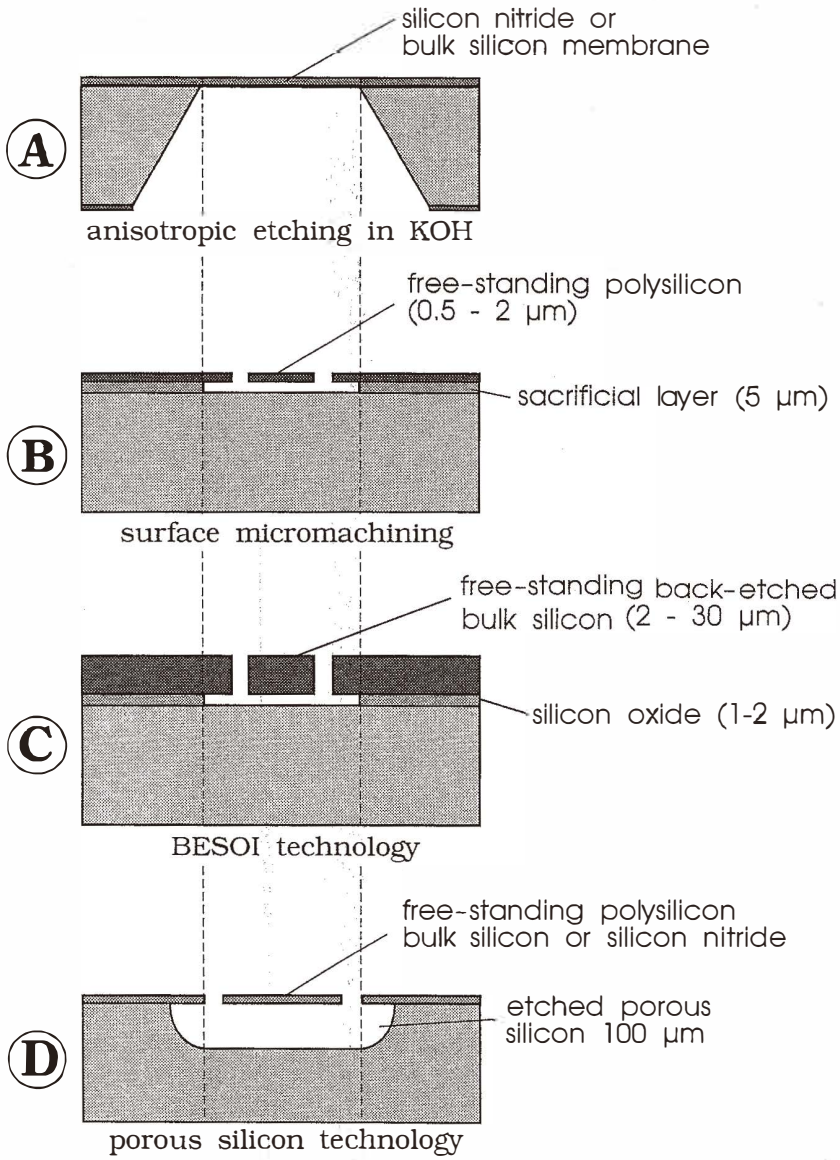

Fig. 3. Microstructuring methods for sensors. A: Anisotropic etching. B: Surface micromachining. C:BESOI-technology. D:Porous silicon technology.

the method is CMOS-compatible since only HF is used for etching. The most important technological problems are the internal stress in the film and possible adhesion of the structures to the substrare due to the small gap. Since the structures are freed by lateral undercutting, free-standing planes cannot be realized without holes for the etchant. Surface micromachining with oxide as a sacrificial layer does not allow large gaps between the structure and the bulk. Therefore, it cannot be used for thermal sensors in which large gaps are needed for isolation.

3.3 *BESOI technology*

Back-etched silicon on insulator (BESOI) is a technology used in the fabrication of mechanical sensors, particularly pressure sensors.[13,14] The principle is shown in Fig. 3(c). On a silicon wafer, a silicon oxide layer is grown. Then a second wafer is formed on top of the oxide. When the compound is annealed at a high temperature, the two wafers are bonded together (silicon fusion bonding). The top wafer is thinned by chemical mechanical polishing (CMP). Advanced polishing technology allows fabrication of a layer with good homogeneity. Thick layers can be realized as well as very thin ones. For sensor applications, the buried oxide in the compound is used as an etch stop. Another possible method of obtaining membranes is to structure the oxide before bonding. This technology is very promising for CMOS-compatible pressure sensors. For thermal devices it is more difficult to apply because, first, the membranes are silicon, which has a high thermal conductivity, and second, the distance from the membrane to the bulk is short.

3.4 *Porous silicon technology*

Considering the technologies described above, the best alternative to KOH etching is a surface micromachining process with a thick sacrificial layer. This layer must have the following features.

- It must be possible to produce layers with thicknesses which range from a few μm to several hundred μm.
- The layer should be etched very easily with high selectivity .
- It must be possible to deposit and structure thin films on top of the layer.
- The methods used to produce and etch the layer must be CMOS-compatible.
- Etch stop at a low doping level of silicon is desired.

A material which meets all these requirements is porous silicon anodically etched from a silicon wafer in HF. The CMOS compatibility of this process was demonstrated when electronic circuits were fabricated on silicon islands isolated by oxidized porous silicon. Thus porous silicon is used to make SOI substrates.[15,16] Later we show that the other requirements are also fulfilled. For thermal sensors, this technology is especially promising. A membrane layer of silicon nitride or carbide can be deposited on top of the porous material, which is removed at the end of the process. In this way, a surface micromachining process with a thick sacrificial layer is performed, as shown in Fig. 3(d). The fundamental drawback of the method is the undercutting of the structures, which limits the possible aspect ratio. Since thermal transducers always have a size of several hundred μm, this problem does not arise here.

4. Porous Silicon

When silicon is exposed to HF, it normally dissolves very little. If a current flows accross the interface of the silicon and the etchant and if the Si is at anodic bias, it starts to dissolve due to an electrochemical process.[17] The current carries holes to the surface which are necessary for the electrochemical process of the dissolution of Si in HF. Figure 4 shows the electrochemical cell used. The wafer is immersed in a solution of HF, ethanol and water usually of ratio 1:2:1. The electrodes are made from platinum. A white-light halogen lamp is installed in front of the wafer in order to illuminate it during etching, if desired.

Why does this etching cause pores? If the applied current is high, no pore formation occurs but electropolishing does. In this case, the number of holes is high due to the high bias voltage. The etching speed is controlled by the number of HF molecules at the surface which must be replaced by diffusion. Projections in the crystal are etched preferentially and the surface becomes smooth. When the current is small, the etching speed is controlled by the carriers. The carrier motion is determined by the electrical potential which is largest at the pits in the crystal. These pits grow preferentially to form pores. To obtain a porous material, the remaining silicon between the pores must be passivated to prevent further

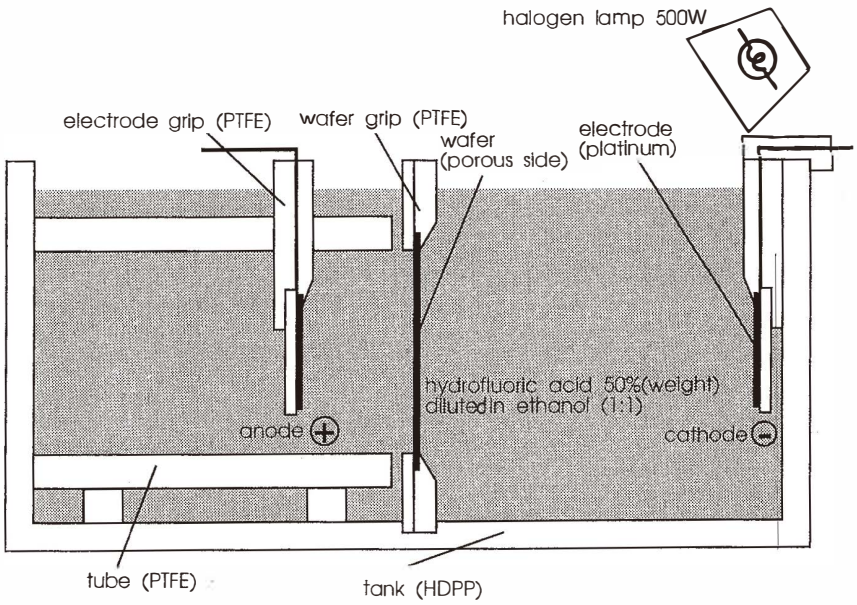

Fig. 4. Electrochemical cell used for anodic etching. The cell is made from HDPP, which is resistant to HF solution. The electrodes are made of platinum. The wafer is immersed in the etchant and can be illuminated with white light during etching.

etching. This passivation is effected by different physical mechanisms depending on the doping of the Si and on the illumination during etching. The different mechanisms generate different morphologies of porous silicon.

4.1 *Macroporous silicon*

This is formed when a low-doped n-type wafer is etched without illumination. The interface between the silicon and the HF is a Schottky contact, which is reverse biased. The etching layer is determined by the space-charge region around each pore. In this space-charge region, there are no holes available, and consequently the material cannot be etched. Between two pores, a wall with a thickness of twice the space-charge region is passivated. A typical pore and structure size is 1 μm which is determined by the doping level, the bias and the HF concentration. The pores follow the electrical current lines and are therefore mainly perpendicular to the wafer surface. When a prestructured wafer is used, a very regular arrays of holes can be fabricated.[18] Applications of macroporous silicon are for the fabrication of trenches for high electrical capacity, microfilters and microfluidics. The use of perpendicular macropores has been proposed to prepare grooves and trenches and to fill them with metals in order to obtain interconnections from the front to the back of a wafer.

4.2 *Nanoporous silicon*

If p-doped silicon is anodized, the front edge of the wafer is a forward-biased Schottky contact. Therefore, numerous carriers are present and no space-charge region develops. Here, passivation is achieved by a quantum confinement effect.[17] Below a certain thickness, the remaining structures form quantum wires, their band gap increases, and the charge carriers no longer enter those structures. The structure size is a few nm.

Nanoporous silicon can also be etched from n-type material when the wafer is illuminated during etching. The absorbed photons generate electron-hole pairs, and thus the interface is flooded with carriers and the space-charge region vanishes. Therefore, when exposed to illumination, n-type silicon shows a pore morphology similar to that of p-type material.

Nanoporous silicon is being intensively investigated due to its quantum confinement effect and its luminescence.[19,20] For sensors, it is of interest due to its large internal surface area of 600m^2/cm^3 which can be used for gas adsorption.

4.3 *Mesoporous silicon*

When either p$^+$- or n$^+$-type degenerately doped silicon is anodized, the structure size is between those of macroporous and nanoporous materials and ranges from 10 to 500 nm. Mesoporous silicon also has a large internal surface area. It is an attractive material for sensor applications. A humidity sensor made of porous silicon has been realized.[21] It is also possible to use the large surface area to support a catalyst in a pellistor or for the immobilization of active species in gas and biosensors. While nanoporous material tends to break, mesoporous silicon is mechanically stable. The surface has excellent smoothness and can be compared to bulk silicon; no cracks are observed. Thin films can be deposited on this material. The pores are so small that, during deposition, no material enters them, but a film can be grown on top of the porous film. This holds for CVD processes, PVD

processes and sputtering. If deposition into the pores is desired, it can be performed by wet-chemical deposition such as electroplating or impregnation. Furthermore, mesoporous silicon can be easily removed by weak etchants. For these reasons, mesoporous silicon is the preferred material for sacrificial layer technology.

5. Masking Layers and Etch Stop

5.1 *Masking layers*

For micromachining, it is necessary to etch defined areas and to limit the etched area laterally. This can be achieved using a resistive film as a masking layer, which is structured by thin-film technology. Since the highly concentrated HF used for anodization is a very strong etchant, the chemical stability requirements on this film are severe.[22]

Photoresist is resistant to the etchant for about 10 min. It can be used for short anodization times, but the HF and ethanol attack the edges of the mask. Therefore, the borderlines of the anodized area are rough and not very well defined. Silicon oxide and silicon nitride are resistant to the etchant for only a few seconds.

The best results are obtained with thin films of amorphous silicon carbide. It is deposited[23] by plasma enhanced chemical vapor deposition (PECVD) from hexamethyldisilane which comes from a liquid source and is carried by argon which is used as a process gas. The film is semi-insulating. Therefore, there is no current flow through it and no electrochemical attack from HF. The etching rate in HF is less than 1 nm/min. SiC is structured by reactive ion etching (RIE) in a fluoroform/oxygen plasma.

5.2 *Etch stop techniques*

The other possible method for achieving lateral structuring is to prevent part of the silicon from being anodized. Since anodization is an electrochemical dissolution, etching only occurs where current flows. When part of the wafer is isolated electrically, it is passivated from etching. One way of achieving this is to induce a p/n transition by implantation. This type of etch stop was used for SOI structures.[15] The degree of etching is mainly determined by the availability of holes in the silicon. Therefore, good selectivity is obtained between n^--type and p^--type silicon. Another possibility is the use of n^-- versus n^+-type (or p^-- versus p^+-type) material. Micromechanical structures made of monocrystalline silicon can be realized.[24–26] This type of etch stop is highly advantageous compared to the etch stopping technique in anisotropic etching in which highly doped material (p^+), which is not advantageous for integration, is required, or we must ensure electrical contact during etching, which is complicated. In the case of porous silicon, we achieve the etch stop in low-doped silicon without contacts.

Figures 5 and 6 show a cantilever fabricated using this etch stop method. The process starts with a p^--doped wafer. The structure to be protected from etching is defined by implantation (P, 250 keV, $2 \times 10^{13}/cm^2$). During an annealing step of 24 h at 1100°C an n-Si layer with a doping of $5 \times 10^{16}/cm^3$ is formed. The p/n junction is at a depth of 4 μm. Then anodic etching is performed for 40 min with a current density of 20 mA/cm^2. After that, the porous material is removed. Figure 5 shows a bridge fabricated in this way. The bridge is 600 μm long, 200 μm broad and 4 μm thick. To improve the undercutting of the

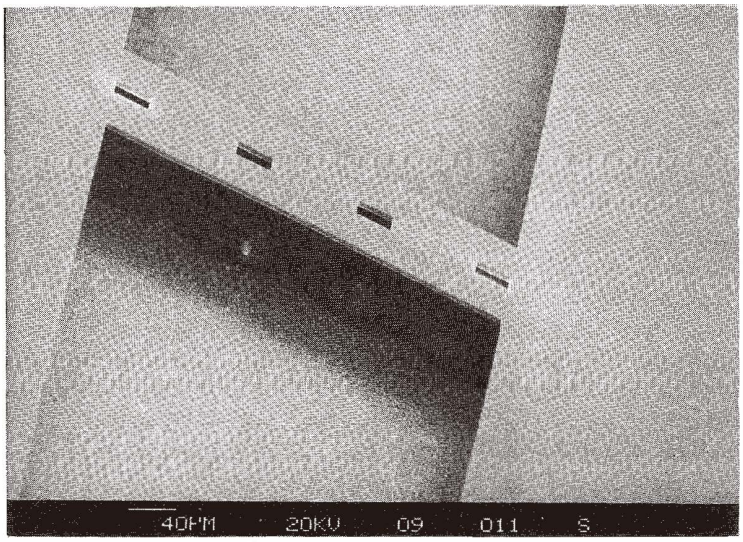

Fig. 5. A bridge made of monocrystalline silicon fabricated by porous silicon technology. The etch stop is a p/n junction.

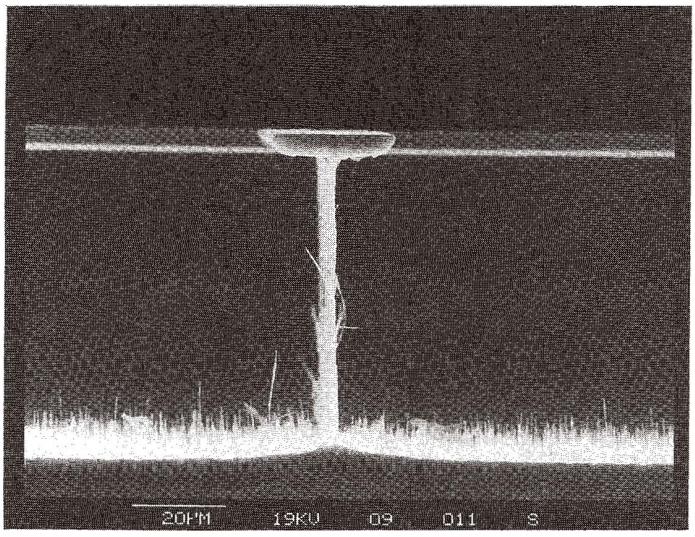

Fig. 6. Porous silicon technology allows etching of free-standing structures which are supported by vertical walls or pillars of silicon.

bridge, there are some holes in it. Figure 6 shows a free-standing cantilever from the side. Under the structure, the wall of remaining silicon can be seen, positioned at the center under the structure. This is the most difficult place for the current lines detouring around the passivated area to reach. This connection to the bulk is a typical feature of this kind of etch stop. Normally, this structure is removed together with the porous film. This phenomenon may have very interesting applications. We can make free-standing silicon structures which are supported by thin vertical walls or pillars. The thickness of the pillars can be controlled by doping the wafer. The walls of the pillar are vertical. In Fig. 6 the support is 60 μm high and 1.25 μm broad, which gives an aspect ratio of 48. Higher pillars and larger aspect ratios are possible.

The use of polysilicon as a masking and structure layer combines etch stop techniques and masking layers.[27,28] Figure 7 shows a thin bridge of polysilicon fabricated in this way. The process starts with the thermal oxidation of a p-type wafer. Then a 500-nm-thick layer of n-type polysilicon is deposited. The bridge and the pads which anchor it are structured in the polysilicon. Then the wafer is anodized. While the open parts of the wafer are etched, the polysilicon is not attacked. It is insulated from the bulk by the oxide and from the HF by a reverse Schottky contact. No carriers pass through the interface from the polysilicon to the etchant, and thus it is passivated. Using this technology, free-standing wires which are 500 nm by 5 μm in cross section and 600 μm long can be fabricated and used as hot wire flow probes.

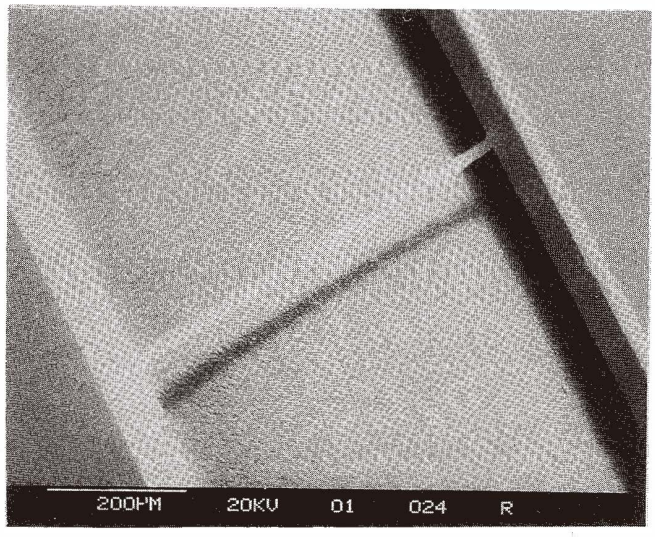

Fig. 7. SEM micrograph of a polysilicon bridge of cross section 500 nm by 20 μm and 600 μm long. The bridge is fabricated using porous silicon as a sacrificial layer.

5.3 *Undercutting*

Etching always follows the lines of electric current. At the edge of the mask, there is a lateral current from the etched region into the region under the mask. This current causes undercutting. A typical etching profile is a ramp which can be seen below the cantilever shown in Fig. 8. The undercutting is slightly different for different masking layers.[22]

The extent of the undercutting is about 1 to 2 times the depth of the porous layer. Thus, anodization causes undercutting similar to that of isotropic etchants. Figure 9 shows a flow channel made by anodization and removal of the porous material. The slope of the walls is about 45°. The figure also shows that there is no undercutting of convex corners such as that which occurs in KOH etching.

6. Examples of Application

Porous silicon is used to realize sensors on insulating bridges and membranes for measuring IR radiation (bolometer principle) and liquid mass flow.[29] The bridges have sizes ranging from 150 μm to 1000 μm and the circular sensors have diameters ranging from 300 μm to 1300 μm. Figure 10 shows the process. The material is a <100> p^+ (B, 0.010–0.018 Ωcm) silicon wafer 4 inches in diameter. For the anodization, a photoresist mask is used. Anodization is performed by electrochemical etching in HF. The solution is

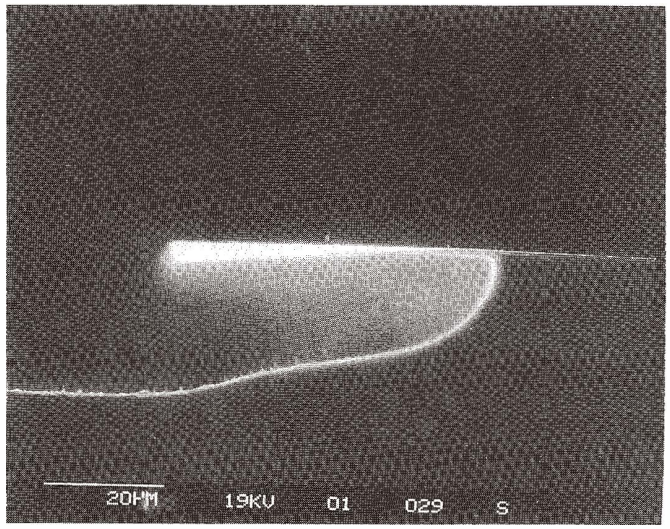

Fig. 8. SEM micrograph of a cantilever made of polysilicon, seen from the side. The micrograph shows the typical undercutting profile of anodic etching.

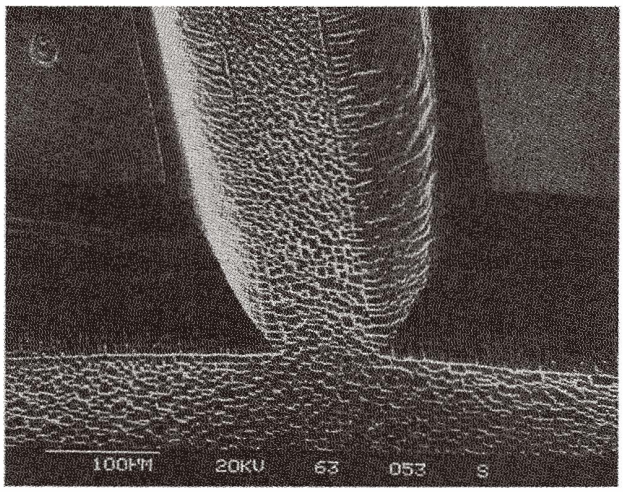

Fig. 9. A flow channel structured with porous silicon. The slope of the walls is about 45°. No undercutting of convex corners occurs.

25% (weight) HF, 25% water and 50% ethanol. A current density of 100 mA/cm^2 is applied for 20 min. Thus, a porous layer 50 μm deep is generated. The porous material generated from p$^+$ silicon is mesoporous. The average structure size of the silicon skeleton is 20 nm to 50 nm, and the porosity is 70%. Figure 10(a) shows the sensor after anodization. After the resist is removed, a 200 nm layer of amorphous SiC is deposited for the membrane. The SiC shows compressive stress after deposition, which is relaxed by annealing (600°C, 30 min, N_2). The details of the SiC process are given in ref. 23. The metallization is a 500 nm gold layer on an adhesion layer of 15 nm NiCr. The metals are structured by wet chemical etching to form the resistors and the bond pads (Fig. 10(b)). For the removal of the porous material, the membrane must be opened by RIE etching. Then, the porous silicon is removed using a weak KOH solution (10%) at room temperature.

Figure 11 shows a SEM micrograph of a free-standing flow measurement bridge at the end of the process. When the porous silicon is removed, a trench is formed. The dimensions of the bridge are 150 μm by 300 μm. A measurement resistor which has the form of a meander is placed on the bridge. This type of structure is used for flow measurement. The bridges are mechanically strong enough to withstand high flow speeds. When this chip is bonded to a second chip which only has flow channels, a fully closed throughflow measurement system is realized. Figure 12 shows a circular bolometer, which is free-standing and anchored with four supports.

The structures are characterized thermodynamically in a heating experiment. The resistor has a low resistance of $R_0 = 65\ \Omega$. The temperature coefficient of the gold is α (20°C, differential) = 1.5×10^{-3}/K. Next, the membrane is heated by an electrical current and the temperature change is measured. This gives the thermal isolation $1/K$ of the

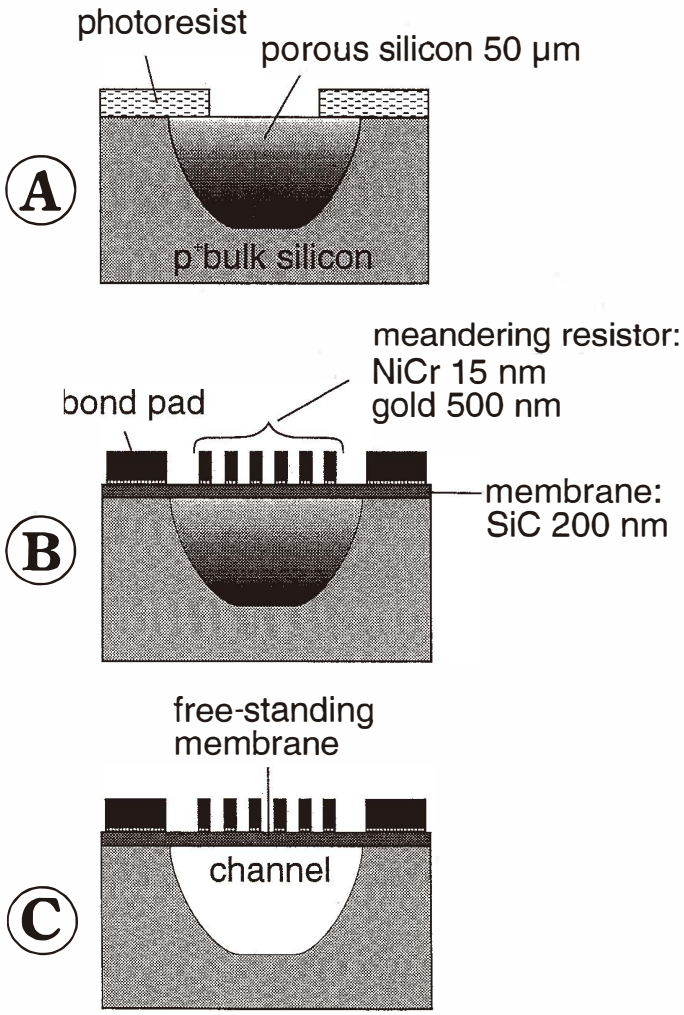

Fig. 10. Processing of a membrane sensor in porous silicon technology. A: Anodization with a photoresist mask B: Deposition of the membrane, deposition of the metal and structuring of the metal. C: Opening the membrane and removing the porous silicon.

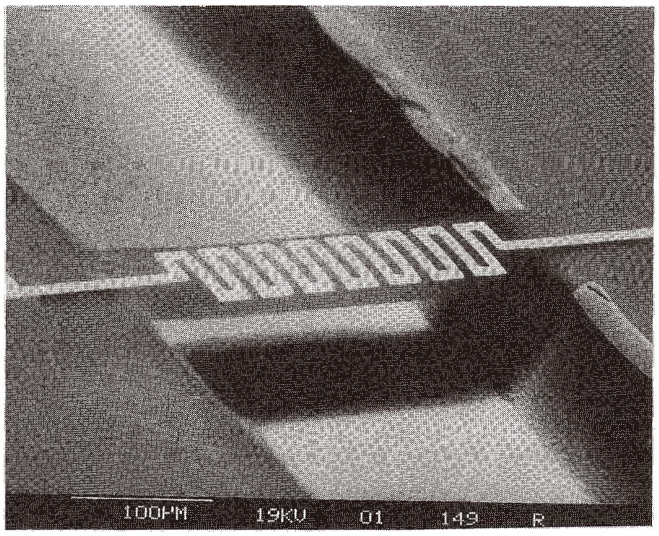

Fig. 11. Heated bridge for flow measurement fabricated using porous silicon technology.

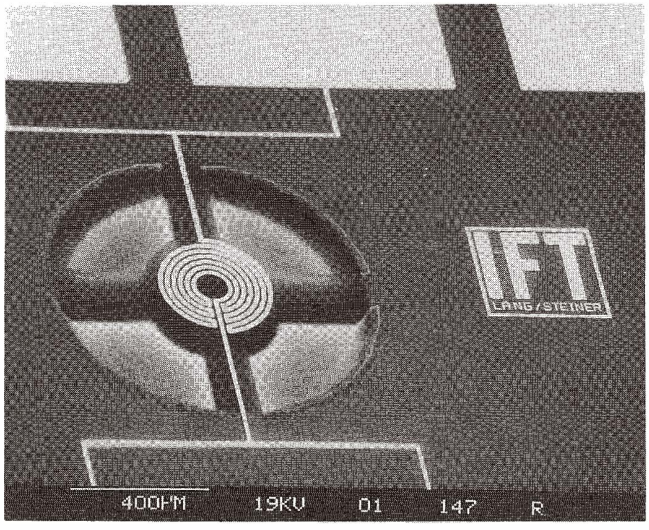

Fig. 12. Bolometer on a SiC membrane fabricated using porous silicon technology.

structure, which determines the sensitivity. Figure 13 shows the temperature difference ΔT versus the electrical power P. The thermal isolation of the structure is very good.

$$K = \Delta P / \Delta T = 104\ \mu\mathrm{W/K}.$$

This value is comparable to the heating power of commercial membrane sensors. The good thermal isolation is due to the bridge structure, which restricts thermal flow to two directions, whereas a membrane usually has four sides in thermal contact with the bulk of the chip. The response of the sensor is described by the slope S, defined as the relative resistance change per unit of power:

$$S = \Delta R / R_0 P = 15\ \mathrm{W^{-1}},$$

a value which is within the acceptable range for thermal sensors. The detection limit of the sensor is given by the noise equivalent power (NEP). For bolometers with metal resistors the noise is calculated using Nyquist's formula with the measured data for the slope. We obtain

$$NEP = 0.6\ \mathrm{nW}/\sqrt{Hz}\ .$$

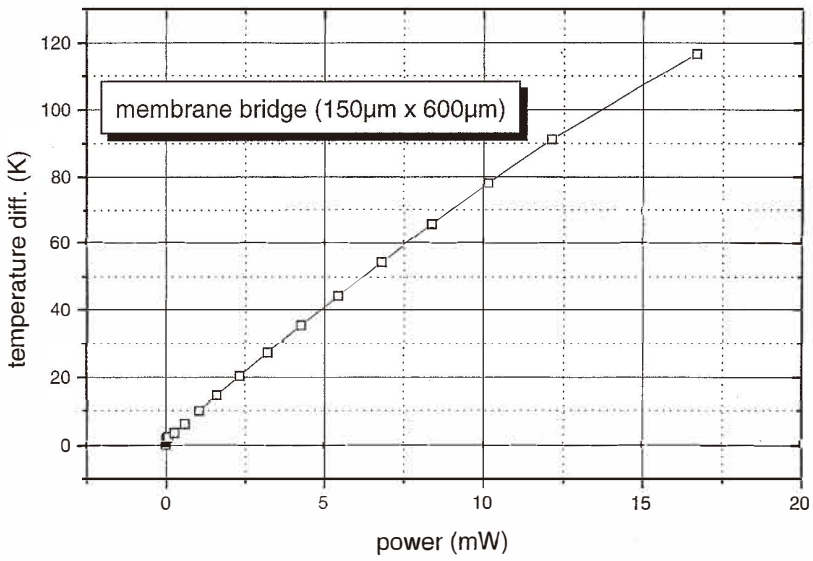

Fig. 13. Electrical heating of the bridge sensor: temperature difference versus heating power. At low temperatures, the specific heating power is 104 μW/K.

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References

1 D. R. Pitts and L. W. Sissom: Heat Transfer (McGraw-Hill, New York, 1977).
2 W. Lang: IEEE Transactions on Electron Devices **37** (1990) 958.
3 W. Kriegl, P. Steiner, B. Folkmer and W. Lang: Sensors and Actuators **A 46–47** (1995) 637.
4 R. B. Bird, W. E. Stuart and E. N. Lightfoot: Transport Phenomena (Wiley, New York, 1960) p. 412.
5 H. Seidel, L. Csepregi, A. Heuberger and H. Baumgärtel: J. Electrochem. Soc. **137** (1990) 3612.
6 H. Sandmaier, H. L. Offereins, K. Kühl and W. Lang: Transducers 1991, San Francisco p. 456.
7 U. Schöneberg, F. V. Schnatz, W. Brockherde, P. Kopystynski, T. Melhorn, E. Obermaier and H. Benzel: Transducers 1991, San Francisco, p. 304.
8 J. Weber, S. Seitz, U. Steger, B. Folkmer, U. Schaber, A. Plettner, H. L. Offereins, H. Sandmaier and E. Lindner: Sensors and Actuators **A 46–47** (1995) 137
9 H. Baltes and D. Moser: Transducers 1993, Yokohama, p.736.
10 R. T. Howe: J. Vac. Sci. Techn. **B 6** (1988) 1809.
11 H. Guckel, J. J. Sniegowski, T. R. Christenson, S. Mohney and T. F. Kelly: Sensors and Actuators **20** (1989) 117.
12 W. Kuehnel and S. Shermann: Sensors and Actuators **A 45** (1994) 7.
13 K. E. Petersen: Proc. IEEE **70** (1982) 420.
14 K. E. Petersen, D. Gee, F. Pourahmadi, R. Craddock, J. Brown and L. Cristel: Transducers, 1991, San Francisco, p. 397.
15 R. L. Smith and S. D. Collins: J. Appl. Phys. **71** (1992).
16 G. Bomchil, A. Halimaoui and R. Herino: Microelectronic Engineering **8** (1988) 293.
17 V. Lehmann and U. Gösele: Appl. Phys. Lett. **58** (1991) 856.
18 V. Lehmann: J. Electrochem. Soc. **140** (1993) 2836.
19 L. Canham: Appl. Phys. Lett. **57** (1990) 1046.
20 W. Lang, P. Steiner and F. Kozlowski: J. Luminescence **57** (1993) 341.
21 A. Richter: Transducers 1993, Yokohama, p. 310
22 P. Steiner and W. Lang: Thin Solid Films **255** (1995) 52.
23 A. Klumpp, U. Schaber, H. Offereins, K. Kühl and H. Sandmaier: Sensors and Actuators **A 41–42** (1994) 310.
24 M. Ligeon, F. Muller, R. Herino, F. Gaspard, A. Halimaoui and G. Bomchil: J. Appl. Phys. **62** (1987) 3814.
25 S. Barret, F. Gaspart, R. Herino, M. Ligeon, F. Muller and I. Ronga: Sensors and Actuators **A 33** (1992) 19.
26 J. Braneberg, C. I. J. Eijkel, J. G. E. Gardeniers and F. C. M. van de Pol: Proc. MEMS 1991, Nara, p. 221.
27 P. Steiner, A. Richter and W. Lang: J. Micromech. Microeng. **3** (1993) 32.
28 W. Lang, P. Steiner, A. Richter, K. Marusczyk, G.Weimann and H. Sandmaier: Sensors and Actuators **A 43** (1994) 239.
29 W. Lang, P. Steiner, U. Schaber and A. Richter: Sensors and Actuators **A 43** (1994) 185.