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Integration of Phototransistors in CMOS Circuits

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A solution for integrating a photosensor in custom-designed digital circuits fabricated using conventional complementary metal-oxide-semiconductor (CMOS) technology is presented. In this approach, by starting with device characterization and parameterization, a method for designing sensor cells is developed. Experimental results obtained from a programmable sensitivity photosensor, such as optical gain, linearity, spectral sensitivity and response delay, are presented. The problem of crosstalk from cell integration in an array is also discussed.

1. Introduction

CMOS has become the most popular technology in customized digital integrated circuits for specific applications (ASICs). Design tools and silicon foundries are widely available. A sensor produced using a standard fabrication process, monolithically integrated in a CMOS circuit, takes advantage of this circuitry that can be efficiently used for sensor device control as well as for output signal postprocessing. Moreover, some performances of the sensor can be customized using ASIC design methods. In spite of this, the sensor designer must create many tools not included in the software packages supplied by chip manufacturers.

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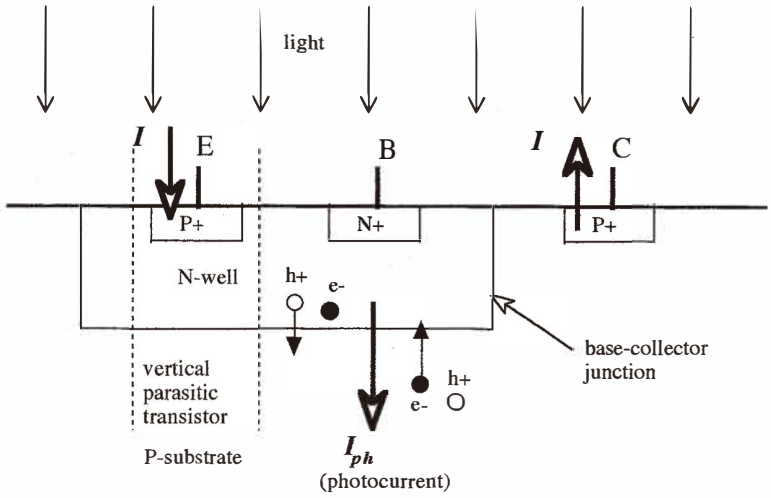
The aim of this work is to develop this methodology using the properties of one of the devices generated in a CMOS process as a photodetector integrated in an array and fabricated using a standard CMOS technology. The active device considered here is the vertical parasitic bipolar transistor of an n-well CMOS structure. The reverse-biased well-substrate junction under illumination collects a photocurrent, I_{ph}, which is amplified by the transistor (phototransistor effect). Figure 1 schematically shows the device structure.

In the past, p-n junctions of CMOS structures have been used as temperature sensors.[1] Light detection using such junctions has also been studied[2–4] and used in image processing.[5] The photo-ASIC concept has been suggested[6] for integrating photosensors in these custom designed circuits.

2. Method

The study of the sensor device begins with an analysis of electrical and electrooptical characteristics of CMOS phototransistors. Optical gain and spectral sensitivity have been measured in devices designed and fabricated using standard techniques for digital circuitry.[7] The DC electrical characteristics of the transistors in the dark and under illumination are used for SPICE parameterization and an evaluation of the photocurrent output. The



$$I = \beta (I_0 + I_{ph})$$

Fig. 1. Bipolar vertical transistor in a n-well CMOS structure.

junction capacitances are obtained from numerical simulations after fitting to measured DC characteristics. An initial estimation of the transistor cut-off frequency can then be obtained.

The second step is pixel design, which includes the phototransistor and readout and reset circuits. All the devices in these circuits are CMOS switches and capacitors. Their parameterizations are well known and will be used, along with our transistor parameterization, in a SPICE simulation to assist in circuit design.

The pixel characteristics, sensitivity and velocity, are evaluated and measured after fabrication. Integration of this sensor in an array means not only an array architecture definition but also an evaluation of the optical crosstalk effect occurring between two pixels.

Our approach to the problem follows the above-mentioned steps. Finally, a circuit demonstrating the sensor integrability in digital systems is realized.

3. Results

Transistor currents under white light are presented in Fig. 2. The photogenerated current, I_{ph}, is collected by the well-substrate junction acting as a photodiode. Optical gain is defined as

$$h_{FE} = \frac{I_{collector}}{I_{ph}}.$$

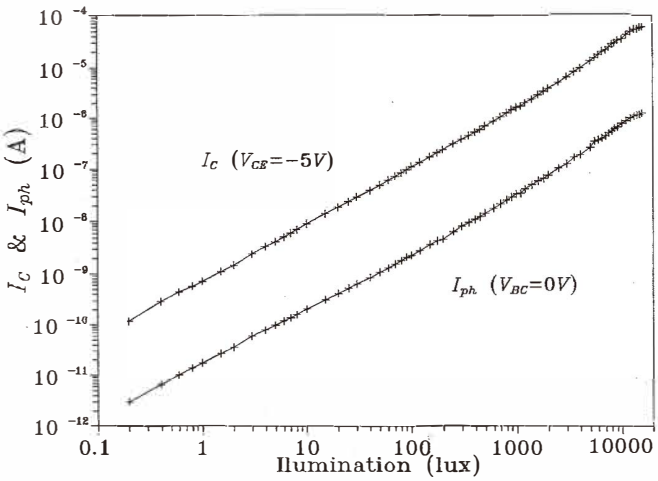


Fig. 2. Photocurrent collected by well-substrate junction (I_{ph}) and transistor collector current (I_C) as a function of illumination level. White daylight is used.

Its value is the same as the dark current gain for the same collector-current level. The response is linear across more than five decades. The absolute current values depend on the transistor size ($88 \times 110\ \mu m^2$ in Fig. 2). The leakage collector current under collector-emitter bias between 0 and 5 volts is smaller than 1 pA (smallest reliably measured value). SPICE parameters for the same transistor are summarized in Table 1.

Figure 3 displays the spectral response curve measured in 3 devices. Interference effects in isolation and chip passivation layers are responsible for the ripples observed.

The pixel designed using these values is shown schematically in Fig. 4. The T_D CMOS transmission gate is in the ON state during the photosignal integration time and OFF during reset time. The resetting operation is performed by T_R transistors.

Output voltage V_{OUT} as a function of time for different illumination levels is represented in Fig. 5 for one cycle of operation. Its behavior during the readout time is linear. Some deviations from linearity are observed in curves with large voltage swing, i.e., 5 to 0 volt.

Table 1
SPICE parameterization for a transistor with a $88 \times 23\ \mu m^2$ well (base) and $78 \times 6\ \mu m^2$ drain diffusion (emitter).

$IS = 8.14 \times 10^{-16}$	$BF = 55$	$VAF = 35$
$RC = 8.23 \times 10^{+1}$	$RE = 7.24 \times 10^{-1}$	$RB = 2.24 \times 10^{+3}$
$KF = 7.62 \times 10^{-4}$	$CJE = 2.63 \times 10^{-13}$	$CJC = 1.65 \times 10^{-13}$
$BR = 18.3$	$VJC = 6.13 \times 10^{-1}$	$VJE = 7.54 \times 10^{-1}$

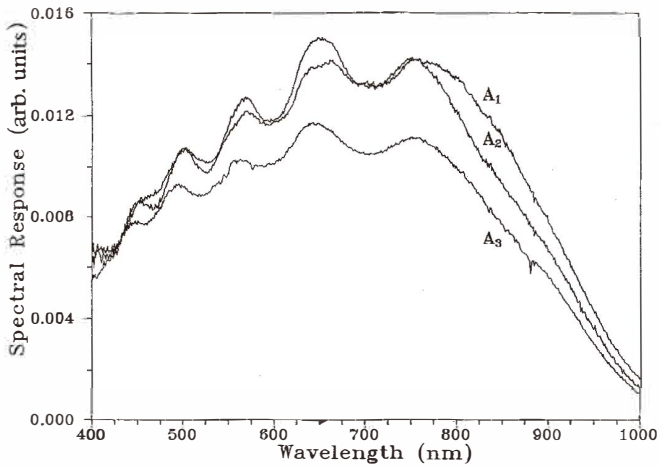


Fig. 3. Spectral sensitivity of photocurrent in 3 devices of different sizes: A_1 ($110 \times 88\ \mu m^2$), A_2 ($23 \times 88\ \mu m^2$) and A3 ($23 \times 21\ \mu m^2$).

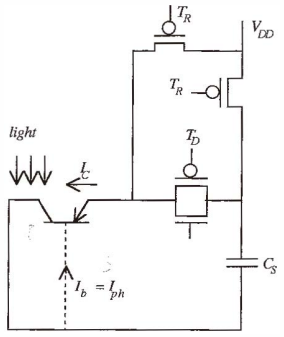


Fig. 4. Control circuit for sensor signal readout and reset operations.

The Early effect in the phototransistor is responsible for such deviations. At very low collector-emitter voltages the transistor enters the saturation region.

An optimal detector sensitivity can be achieved if the readout time corresponds with the light intensity, as shown in Fig. 6, which represents the V_{OUT} value at a fixed time as a function of the light intensity.

The transient response to light signals has been studied in the base-collector photodiode. The output voltage as a function of time when the light is switched off displays a two-time-constant behavior, often observed in photodiodes:[10] one, t_d, depends on internal device transient time and the other arises from RC circuit-device coupling. Figure 7 shows the output voltage rise time, t_r, as a function of the resistance R of the diode biasing circuit. At low R values, t_r approaches t_d, the physical limit for speed. Signal frequencies above 100 kHz can be followed by this device. Focusing the light beam (lower curve) on the transistor base reduces t_d because the photocarriers are generated closer to the collector junction. These measurements have been obtained in a 50×50 μm^2 device.

The crosstalk effects in sensor arrays have been evaluated using a two-dimensional approach. The photocurrent in the well-substrate junction is calculated from an analytical solution[11] of the minority carrier diffusion equation on both sides of the junction. The result is presented in terms of a characteristic parameter defined as follows. The array surface is divided in cells, each one containing a junction. The photocurrent collected by a cell can be considered as the sum of two terms: I_1 comprised of carriers photogenerated beneath the surface of the cell, and I_2, from the region under the surface of an adjacent cell. The ratio I_2/I_1 is defined as the crosstalk parameter. The curves in Fig. 8 show the result of this evaluation in terms of the distance between two neighbor wells.

We have designed and fabricated a programmable sensitivity detector demonstrating

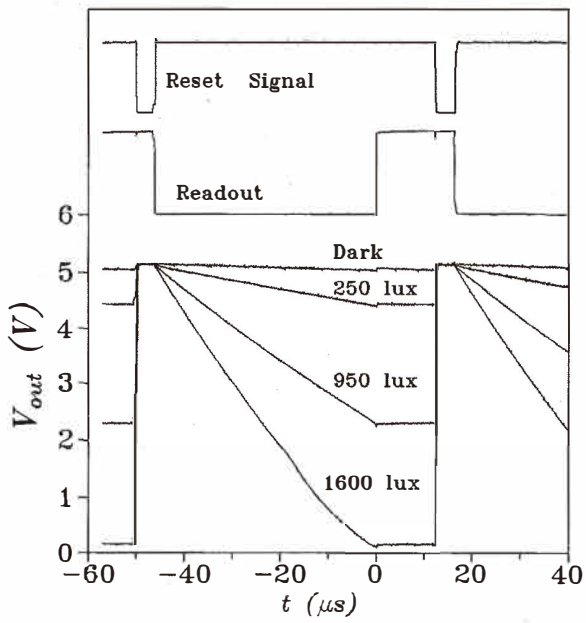


Fig. 5. Sensor output voltage as a function of time for different illumination values. Reset and readout signals are, respectively, T_R and T_D in Fig. 4.

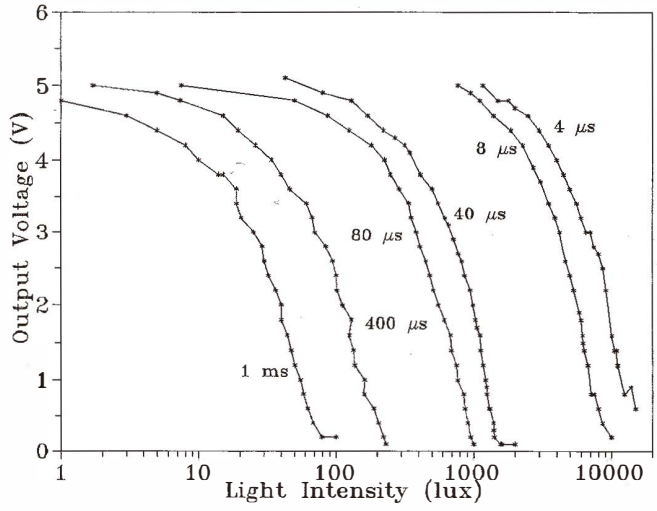


Fig. 6. Sensor output voltage as a function of light intensity for different values of readout time.

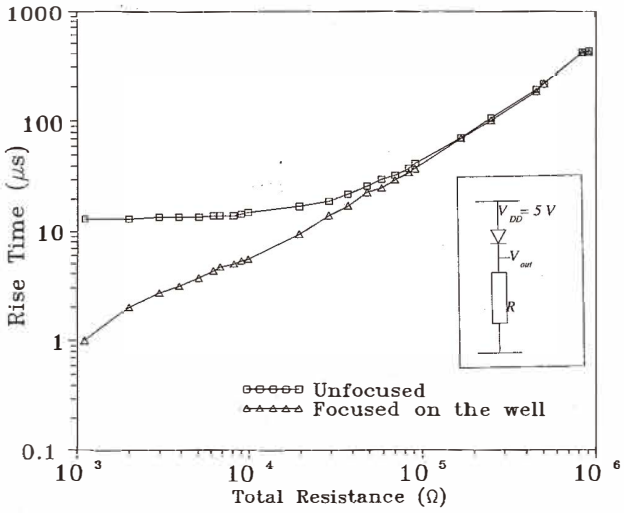


Fig. 7. Rise time of the output voltage when the light is switched off. The sensor is kept in the readout state. Focusing the light beam on the transistor base reduces the diffusion time value.

technological compatibility of sensor and digital circuits. In this system the operation cycle is controlled by a clock signal as shown in Fig. 9(a). In state S0 the system is in stand-by mode until resetting (state S1) is triggered by an external signal EN = 1. After a waiting period (state S2) the readout time begins (state S3). Its duration is N times the clock period. The value of N is given by a 4-bit binary signal input of a modulo-N-counter. The state diagram is outlined in Fig. 9(b). The counter reset signal is internally generated at the end of each cycle. Figure 10(a) is a micrograph of the chip where the counter is in the center and two phototransistors are at the bottom of the picture. It must be pointed out that no perturbations in digital circuitry is observed when the chip operates under illumination. In Fig. 10(b) the following signals are shown.

1. Reset pulse: $T_R = 0$, $T_D = 5$ volts.
2. EN. Immediately after the high-low transition of EN, the readout operation begins. Its duration is 16 clock periods, according to the actual 4-bit input value.
3. Clock signal.
4. Output voltage.

4. Conclusions

The parasitic vertical transistors in CMOS technology can be used as linear photosensors, in the visible-near-infrared spectral region with a gain of over 50, covering a light intensity range from 1 lux to 10,000 lux, and frequencies greater than 100 kHz.

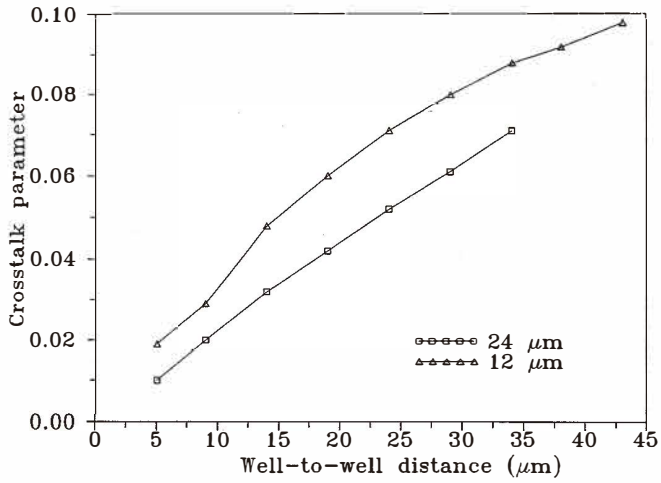
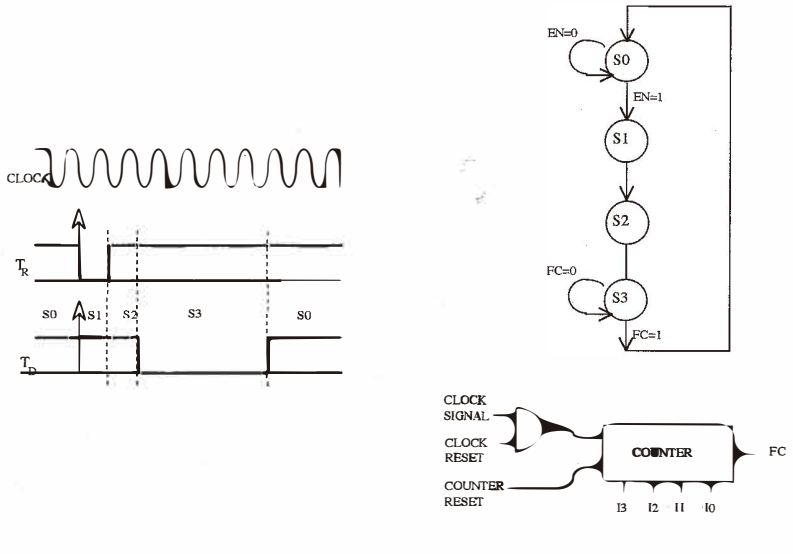


Fig. 8. Two-dimensional crosstalk effect evaluation as a function of the distance between 2 n-wells. Two well sizes have been considered, 12 and 24 μm.



(a) (b)

Fig. 9. (a) Time diagram of control signals. (b) State diagram of control circuit.

(a)

(b)

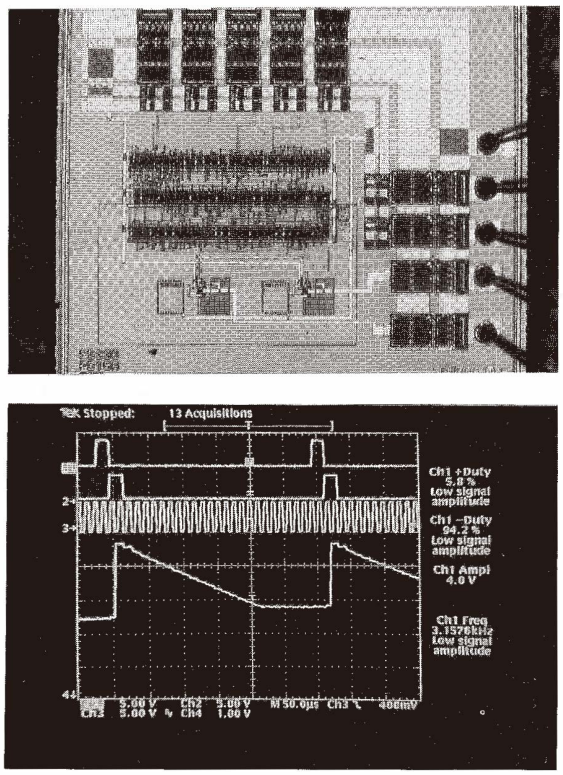


Fig. 10. (a) Micrograph of a chip with two photosensors and the control system. (b) Signals in the circuit: reset, readout operation enable, clock and output voltage.

This detector is suitable for integration in digital circuits. Crosstalk effects are reduced by increasing the ratio of cell size to cell separation. An array with random-access cells can thus be easily implemented. It has also been proven that other characteristics such as programmable sensitivity can be obtained.

A method for developing these sensors using a standard fabrication process has been established and tested. Device parameterization is used in a SPICE circuit simulation. The results obtained are in good agreement with the results of measurements on circuits.

Acknowledgments

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