Sensors and Materials, Vol. 32, No. 8 (2020) 2631–2639
MYU Tokyo

S & M 2289

Design and Theoretical Analysis of Bit Error Rate (BER)-modulated Inductive-coupling Transceiver Using Dynamic Intermediate Interference Control Technique for Low-power Communication

Ge Xu,[1] Kenya Hayashi,[1] Shigeki Arata,[1] Shunya Murakami,[1]
Dang Cong Bui,[1] Atsuki Kobayashi,[1] and Kiichi Niitsu[1,2*]

[1]Nagoya University, IB-North 423, Furo-cho, Chikusa-ku, Nagoya 464-8603, Japan
[2]PRESTO, JST, 7 Gobancho, Chiyoda-ku, Tokyo 102-0076, Japan

(Received August 20, 2019; accepted July 17, 2020)

Keywords: low power, low cost, CMOS, IoT, inductive coupling, communication, transceiver

In this paper, we present a bit error rate (BER)-modulated inductive-coupling transceiver using a dynamic intermediate interference control technique for the first time. By controlling interference from the intermediate writer, the BER can be modulated. A simulation with Simulation Program with Integrated Circuit Emphasis (SPICE) is performed for a proposal of 65 nm CMOS. The simulation results show that the proposed approach is effective for the power and cost reduction of the writer. The layout area without an I/O pad is approximately 0.015 mm^2 and the communication distance is 20 μm. The power consumption of the transmitter is reduced to 0.3 μW.

1. Introduction

The demand for reducing the power consumption and implementation cost in IoT development is increasing. To address these issues, low power consumption and cost reduction techniques have been reported. In IoT development, wireless systems will become the mainstream solution because of their greater usability and higher mobility. In addition, it may not be easy to drill holes through a wall, and a space looks neater without messy wires.(1) However, wireless communication has high power consumption and high implementation cost. One of the effective approaches to reducing the communication power and cost is to decrease the communication distance.

To satisfy this requirement, proximity communication has been developed, especially for interchip communication between three-dimensionally stacked chips.(1) Among the two schemes of proximity communication, namely, capacitive-coupling and inductive-coupling links, inductive-coupling links are advantageous from the viewpoint of communication configuration flexibility. In other words, inductive-coupling links can be applied to not only face-to-face but also face-to-back or back-to-back communication, which means that the application range is

*Corresponding author: e-mail: niitsu@nuee.nagoya-u.ac.jp
https://doi.org/10.18494/SAM.2020.2558

ISSN 0914-4935

extended from two-layer chips to multilayer chips. In addition, inductive-coupling interfaces enable low-power, high-speed, and cost-efficient communication. Pulse-based inductive-coupling transceivers have been applied to a wide range of applications, such as through-chip interfaces, noncontact memory, and wafer-level testing.[2] Since inductive-coupling links can be implemented in standard CMOS technology, they are cost-efficient.

To further reduce the power, we have newly introduced a bit error rate (BER)-modulated technique to inductive-coupling links. Recently, a Wi-Fi BER-modulated technique[3] and a Wi-Fi backscatter technique[4] have been developed for power reduction. In these studies, a marked power reduction by as much as four orders of magnitude compared with that of conventional wireless communication has been reported. The mechanism for the power reduction is interference modulation (i.e., backscattering).

Here, we present a BER-modulated inductive coupling transceiver for the first time. By using the BER modulation scheme, the required power and cost can be markedly reduced for applications in Wi-Fi environments. To verify its effectiveness, a simulation with Simulation Program with Integrated Circuit Emphasis (SPICE) has been performed for a proposal of 65 nm standard CMOS.

The remainder of this paper is organized as follows. Section 2 introduces the proposed BER-modulated inductive-coupling transmitter. Section 3 describes the circuit implementation and simulation conditions. The simulation results are shown in Sect. 4. A discussion is given in Sect. 5. Section 6 gives the conclusion of this study.

2. Methods of Interchip Communication Revisited

Over the past 50 years, Moore's law and related innovations have focused on the scaling of both transistors and wires in chip manufacturing. In the future, data communication between chips will be a bottleneck of system performance.

There are three integration types of wired technology, as shown in Fig. 1. Wire bonding in stacked chips has been widely used in large-capacity storage memory manufacturing.[1] Microbump technology[5] can only be applied to two chips that must be face to face. This could greatly limit its scope of use owing to the requirement of a high-end logic chip with many

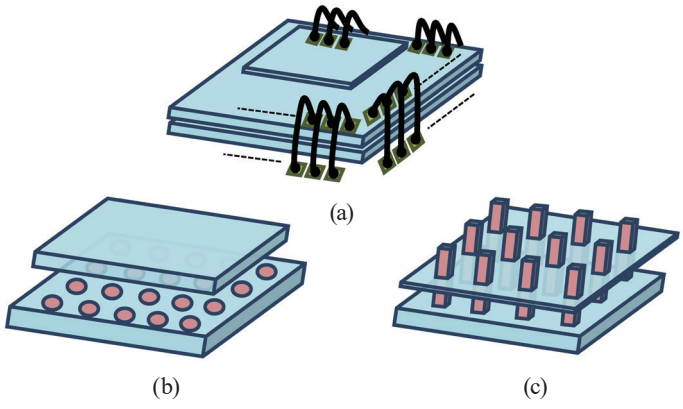


Fig. 1. (Color online) 3D interfaces of wire communication: (a) wire bonding, (b) microbump, and (c) TSV.

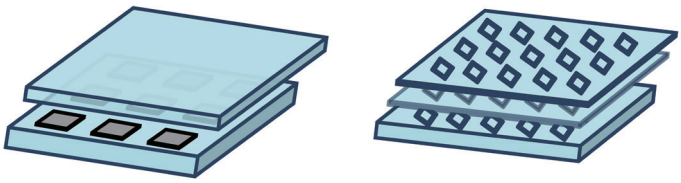
I/O pins. Through-Si via (TSV) technology is also currently attracting considerable interest and is being widely investigated.[6,7] However, because it requires cutting-edge fabrication technologies, it is not yet in practical use owing to the need for manufacturers to invest a lot of money and develop suitable fabrication equipment. Although there is no significant crosstalk when using TSV technology and it has excellent transmission speed, reliability, and power consumption, it has an extremely high cost and requires expensive equipment in manufacturing.

For wireless technology, there are currently two mainstream approaches as shown in Fig. 2: capacitive coupling[8] and inductive coupling.[3–7] Similarly to microbump technology, capacitive coupling can only be used for two face-to-face chips, whereas inductive coupling is more widely used owing to its flexibility. Also, previous studies[9,10] have shown that crosstalk between the inductive-coupling channels and interference with power lines and circuits underneath the inductors are negligible. Thus, the inductors can be placed close to each other to create a dense array of parallel interfaces on top of existing circuits.[1]

3. BER-modulated Inductive-coupling Transceiver

3.1 Concept

Figure 3 shows a conceptual image of the proposed architecture. Its concept is similar to those of the Wi-Fi BER-modulated technique[3] and Wi-Fi backscattering.[4] The proposed



(a) (b)

Fig. 2. (Color online) 3D interfaces of wireless communication: (a) capacitive coupling and (b) inductive coupling.

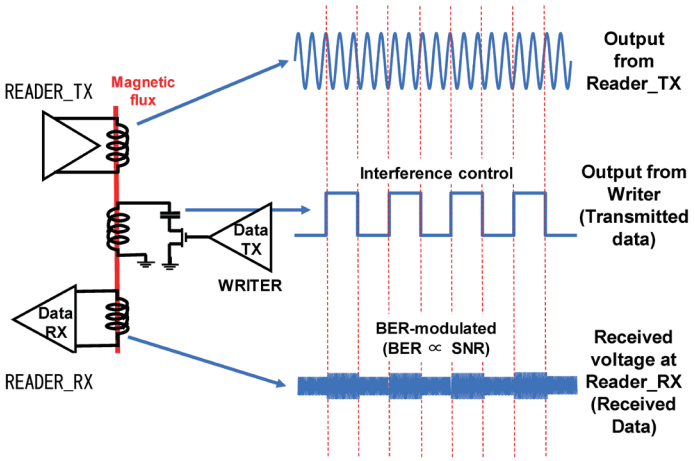


Fig. 3. (Color online) Conceptual diagram of the proposed architecture.

architecture consists of three components: a reader transmitter (READER_TX) and receiver (READER_RX), and a writer (WRITER). Data are transferred from the writer to the reader receiver.

The writer, placed between the reader transmitter and receiver, generates interference that is controlled by a load modulation scheme as well as RFID. As investigated in a previous study,[11] the interference can be changed by the impedance of the closed loop around the path of the magnetic flux.

Identical to the cases of Wi-Fi environments,[3,4] the required power for interference is much smaller than that for conventional inductive-coupling transmission. Thus, power reduction can be expected. Additionally, the size of the writer inductor is expected to be smaller than that in the conventional approach, reducing the cost.

3.2 Circuit diagram

Figure 4 shows a schematic of the proposed circuit. This is a typical example of a physical implementation in standard CMOS technologies.

The reader transmitter consists of an H-bridge transmitter.[11] The writer consists of one capacitor and a serially connected NMOS. The capacitance can be determined using the modulation magnitude while considering the trade-off with the additional footprint. The gate of the NMOS is driven by an inverter chain.

Figure 5 shows a schematic of the reader receiver. The bias voltage is applied to the center of the inductor to guarantee NMOS operation. An asynchronous reader receiver is chosen[11] to simplify the implementation to reduce the power and area of the circuit. If a clock transceiver implementation is acceptable, a synchronous receiver can also be utilized.

In addition, previous studies,[9,10] have shown that the crosstalk between the inductive-coupling channels and the interference with power lines and circuits underneath the inductors are negligible. Thus, the inductors can be placed close to each other to create a dense array of parallel interfaces on top of existing circuits.

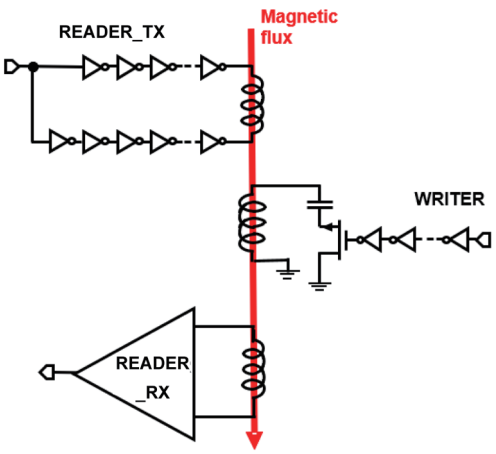


Fig. 4. (Color online) Proposed circuit.

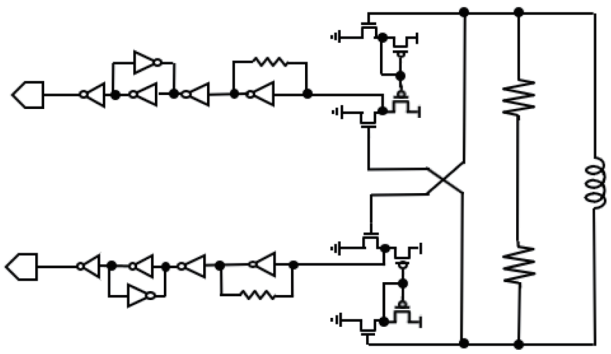


Fig. 5. Schematic of the reader receiver (READER_RX). The bias voltage is applied to the center of the inductor.

3.3 Simulation conditions and test chip design

To verify the effectiveness of the proposed approach, we have performed a SPICE simulation of the proposed circuit using a process design kit (PDK) of 65 nm standard CMOS technology. Core transistors with a nominal supply voltage of 1.2 V were utilized. The coupling coefficients between the inductors were calculated by considering Ref. 11.

The SPICE simulation was performed taking into account the size of the chip, the power consumption, and the signal received, and the chip was fabricated under the following conditions:

- Output signal frequency from Reader_TX: 500 MHz
- Output signal frequency from writer: 2 MHz
- Supply voltages of Reader_TX/RX and writer: 1.2 V
- Diameter of the inductors: 100 μm
- Communication distance: 20 μm
- Load capacitance at the writer: 10 pF

These conditions were determined by considering the performance in Ref. 11. Under these conditions, the power of the writer was calculated to be 0.3 μW and the power of the readers (Reader_TX and Reader_RX) was 200 μW.

A test chip was designed and fabricated in 65 nm standard CMOS technology to verify the effectiveness of the proposed approach. Figure 6 shows the micrograph and layout image of the test chip. To achieve a short communication distance, all building blocks were implemented in one die. By using upper/lower interconnect layers, three coils were stacked with a vertical alignment. The test chip was then measured.

4. Simulation Results

To explore the effect of each parameter on the results, only one parameter of the chip being fabricated was changed at a time in the simulation. Figure 7 shows the simulated waveforms of

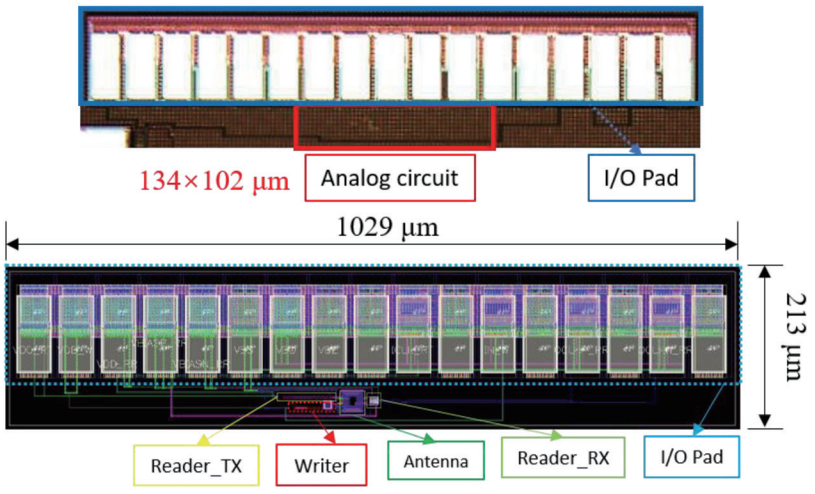


Fig. 6. (Color online) Chip micrograph and mask layout image.

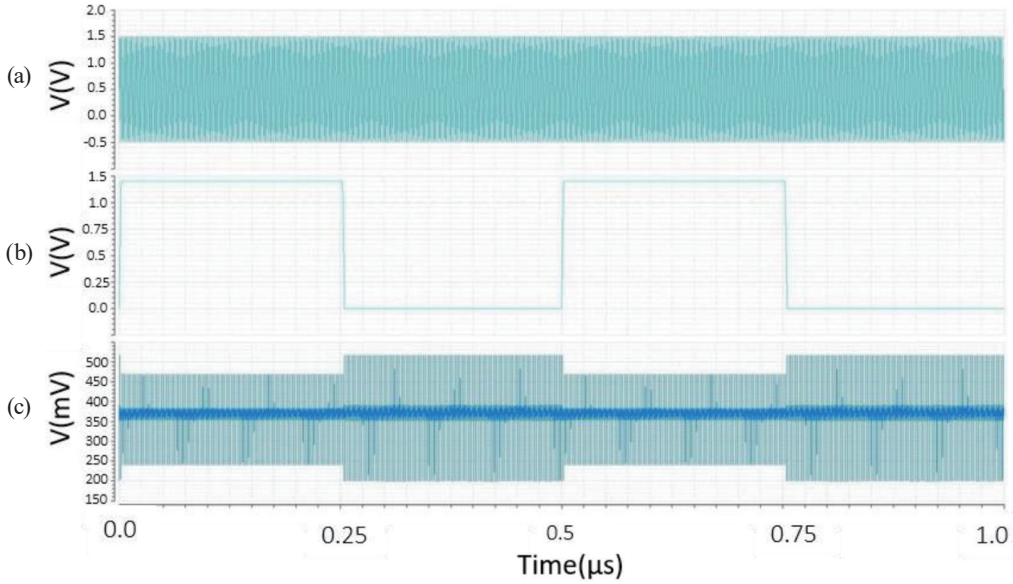


Fig. 7. (Color online) Simulated output waveforms. (a) Output from Reader_TX. (b) Output from writer (transmitted data). (c) Received voltage at Reader_RX (received data).

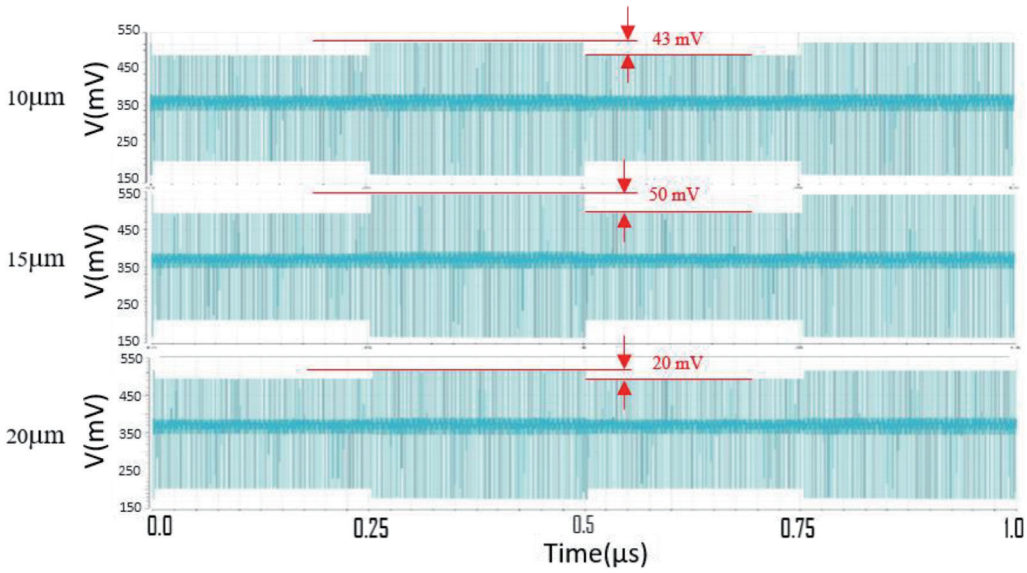


Fig. 8. (Color online) Simulated output waveforms for different communication distances.

the overall transmitted and received signals. As expected, the received signal was modulated by the interference from the writer. A lower received voltage results in a lower SNR (higher BER). Thus, BER-modulated inductive-coupling communication was successfully verified.

Figure 8 shows the simulated waveforms of the received voltage when the communication distance was varied from 5 to 15 μm. The modulation strength increases with the communication distance.

To estimate the BER from the results of the simulation, we measured the ratio of the received voltage because the BER is determined by the SNR of the received voltage. V_{on} is the voltage obtained by Reader_RX when the input of the writer is 0, whereas V_{off} is the Reader_RX voltage when the input of the writer is 1. Here, V_{on}/V_{off} is used to indirectly reflect the SNR. The following are the results of the simulation. At present, the minimum value that can be processed should be at least 1.04. As shown in Fig. 7, the value is 1.23 for the chip fabricated in this study.

Figure 9 shows the ratio of the received voltage as a function of the supply voltage of the writer (VDD_W). As expected, the ratio increased with the supply voltage of the writer. As the supply voltage increases, the magnetic field interference between the readers will also be stronger, leading to an increase in SNR.

Figure 10 shows the ratio of the received voltage as a function of the diameter of the writer inductor (Diameter_Writer). With increasing diameter of the writer inductor, the ratio first increases and then decreases. This may be because when the diameter of the writer exceeds that of the reader, the excess diameter does not affect Reader_RX, and the average magnetic flux change of the non-exceeding part will decrease.

Figure 11 shows the ratio of the received voltage as a function of the number of turns of the writer inductor (turns). The ratio increased monotonically with the number of turns of the writer inductor. This is assumed because the increase in the inductance of the writer allows greater interference.

Figure 12 shows the ratio of the received voltage as a function of the vertical position of the writer. The vertical axis is the distance to Reader_TX. Since the magnetic flux is concentrated on the Tx and Rx inductors, the interference from the writer becomes greatest at Tx and Rx, whereas it becomes smallest at the center position. Thus, a concave almost symmetric characteristic was observed as we expected.

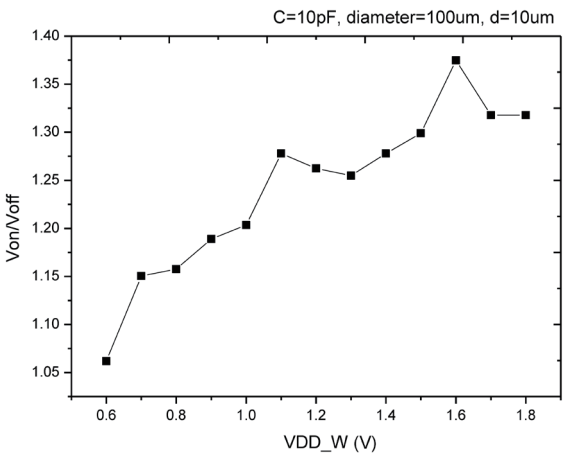


Fig. 9. Ratio of received voltage as a function of supply voltage of the writer.

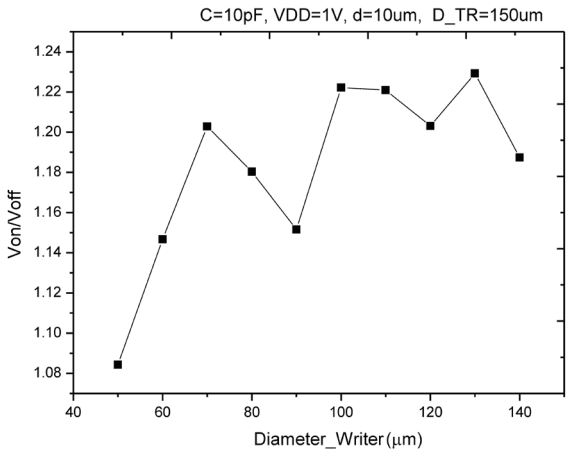


Fig. 10. Ratio of received voltage as a function of diameter of the writer inductor.

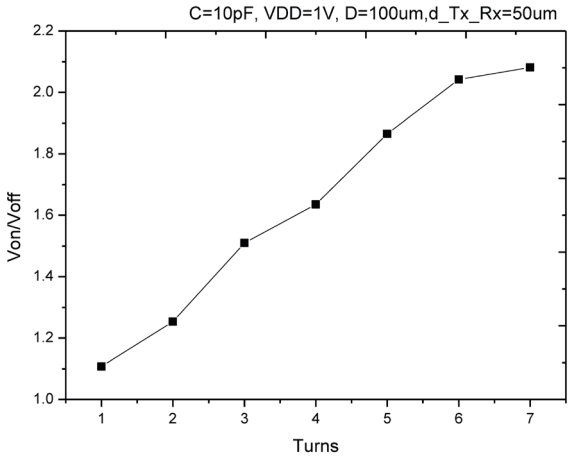


Fig. 11. Ratio of received voltage as a function of number of turns in the writer inductor.

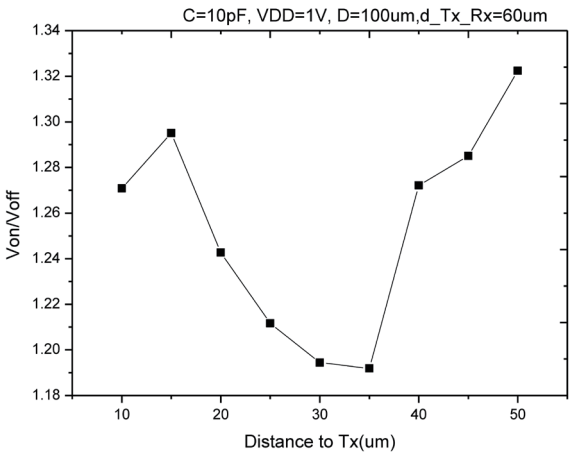


Fig. 12. Ratio of received voltage as a function of the vertical position of the writer.

5. Discussion

Although the proposed approach allows low-voltage operation and low-cost implementation, there are some disadvantages. First, three inductors are required; the proposed approach must employ the reader transmitter/receiver and the writer, increasing the total cost. Secondly, the proposed technique must employ a BER tester in the reader receiver. The BER measurement required for data transmission results in a high overload on the reader receiver side.

As discussed above, the proposed technique focuses on reducing the power and cost of the writer, making it suitable for cost-aware applications.[12–14] Therefore, the designer must take the trade-off with the above disadvantages into consideration.

6. Conclusion

We proposed and demonstrated a BER-modulated inductive-coupling transceiver for the first time. The results of a SPICE simulation showed the effectiveness of the approach and also that the modulation strength can be adjusted by changing the writer design.

Acknowledgments

This research was financially supported by JST, PRESTO (No. JPMJPR15D5), by Grants-in-Aid for Scientific Research (S) (Nos. 20226009, 25220906, and 26220801), a Grant-in-Aid for Young Scientists (A) (No. 16H06088) from the Ministry of Education, Culture, Sports, Science and Technology of Japan, and by Grants-in-Aid from the Strategic Information and Communications R&D Promotion Programme (Nos. 121806006 and 152106004) of the Ministry of Internal Affairs and Communications, Japan. The fabrication of the CMOS chips was supported by the VLSI Design and Education Center (VDEC), University of Tokyo, in collaboration with Synopsys, Inc., and Cadence Design Systems, Inc.

References

1 T. Kuroda and N. Miura: 2006 Eur. Solid-State Device Res. Conf. (2006) 3–6.
2 H. Chung and T. Kuroda: Midwest Symp. Circuits Syst. (2011) 1.
3 H. Ishizaki, H. Ikeda, Y. Yoshida, T. Maeda, T. Kuroda, and M. Mizuno: Proc. IEEE Symp. VLSI Circuits (June 2011) 162–163.
4 B. Kellogg, A. Parks, S. Gollakota, Jo. R. Smith, and D. Wetherall: Proc. ACM Conf. SIGCOMM (Oct. 2014) 607–618.
5 T. Ezaki, K. Kondo, H. Ozaki, N. Sasaki, H. Yonemura, M. Kitano, S. Tanaka, and T. Hirayama: IEEE ISSCC Digest of Technical Papers (2004) 140.
6 J. Burns, L. McIlrath, C. Keast, C. Lewis, A. Loomis, K. Warner, and P. Wyatt: IEEE ISSCC Digest of Technical Papers (2001) 268.
7 K. Takahashi and M. Sekiguchi: Symp. VLSI Circuits Digest of Technical Papers (2006) 114.
8 K. Kanda, K. Kanda, D.D. Antono, K. Ishida, H. Kawaguchi, T. Kuroda, and T. Sakurai: IEEE ISSCC Digest of Technical Papers (2003) 186.
9 N. Miura D. Mizoguchi, T. Sakurai, and T. Kuroda: Proc. IEEE CICC (Oct. 2004) 99–102.
10 K. Niitsu, Y. Sugimori, Y. Kohama, K Osada, N. Irie, H. Ishikuro, and T. Kuroda: IEEE ASSCC (Nov. 2007) 131–134.
11 K. Niitsu, S. Kawai, N. Miura, H. Ishikuro, and T. Kuroda: IEEE Trans. Very Large Scale Integration (VLSI) Syst. **19** (2011) 1902.
12 A. Kobayashi, K. Ikeda, Y. Ogawa, H. Kai, M. Nishizawa, K. Nakazato, and K. Niitsu: IEEE Trans. Biomedical Circuits Syst. **11** (2017) 1313.
13 K. Niitsu, A. Kobayashi, K. Hayashi, Y. Nishio, K. Ikeda, T. Ando, Y. Ogawa, H. Kai, M. Nishizawa, and K. Nakazato: IEEE Trans. Circuits Syst. I (in press).
14 K. Hayashi, S. Arata, S. Murakami, Y. Nishio, A. Kobayashi, and K. Niitsu: IEEE Trans. Circuits Syst. II (in press).