A Dual-feedback K-band Low-noise Amplifier
with Transformer Neutralization Technique

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A dual-feedback K-band low-noise amplifier (LNA) is presented. This circuit consists of two common-source configurations in series. Its input matching network uses the shunt inductive transformer technique to reduce the chip area and improve noise matching, and uses the transformer technique to improve the gain and isolation. The measured input and output return losses are less than −10 dB at 23 GHz, the isolation is −50 dB, and the gain at 23 GHz is 10.6 dB. This chip is implemented by 0.18 μm CMOS technology and its dimensions are 0.22 mm^2. The DC power consumption is 5.4 mW with a supply voltage of 1 V. This amplifier can improve a complete RF front-end for sensor applications.

1. Introduction

Wireless sensor networks (WSNs) have been investigated for many applications from remote sensing and monitoring to medicine, biology, and environmental studies. As the core element of WSNs, the sensor can translate a physical quantity into an electrical signal. The challenges in the design are reducing the device size and power consumption. There are many applications of 24 GHz for the U.S. Federal Communications Commission (FCC) certification and scientific and medical purposes, so the industrial scientific medical (ISM) band is the hottest band to be selected as the operating frequency band. The most common applications of this band are automotive radar and adaptive cruise control (ACC) systems for short-range sensors.[1] Traditionally, microwave and millimeter-wave integrated circuits are mostly fabricated by a GaAs high-electron-mobility transistor (HEMT) process. These circuits have the advantages of high carrier mobility, a semi-insulating substrate, and good high-frequency characteristics. In recent years, with advances in the deep sub-micron complementary metal–oxide–semiconductor (CMOS) process, the transistor cutoff frequency (f_T) has continued to improve, and the CMOS process has been used to implement high-frequency circuits, such as the 24 GHz CMOS RF front-end receiver. Owing to its high integration and low cost, the CMOS process has become very competitive in the fabrication of millimeter chip systems.

A low-noise amplifier (LNA) plays an important role in wireless communication systems. Microwave and millimeter-wave LNAs have been a popular and important research topic. Common-source and spliced-amplifier architectures are very popular for application in narrowband systems. They have a relatively high gain and a low noise figure, but the cascode architecture cannot operate at a low operating voltage. A transformer-feedback LNA that operates at a working voltage of 1 V has been proposed for reducing the supply voltage,[2] but its working frequency is low. A low-power LNA with transformer feedback in the K-band has also been designed.[3] This LNA employs the current reuse technique and has a maximum gain of 10.1 dB and a power consumption of 7.2 mW. A three-stage K-band LNA achieves a gain of 12.86 dB,[4] but its power consumption is as high as 53 mW. A wideband LNA design[5] has a flat forward gain, an excellent noise figure, and a small group-delay variation, but its linearity is poor. Another LNA has been fabricated using a more advanced 45 nm CMOS technology[6] that only uses high-Q above-IC inductors. This LNA has increased linearity and reduced power consumption at the cost of a larger size.

In this paper, a dual-feedback K-band LNA that uses the shunt inductive transformer technique is proposed. This LNA achieves a gain of 10.6 dB and an isolation greater than 50 dB. The chip is fabricated using the 0.18 μm CMOS process, and its chip area is 0.22 mm^2. Its DC power consumption is 5.4 mW with a supply voltage of 1 V.

2. Circuit Design and Implementation

The circuit schematic of a dual-feedback K-band LNA is shown in Fig. 1. This chip circuit architecture contains two cascaded common-source transistors (M_1 and M_2). Its input matching network uses the shunt inductive transformer technique to reduce the chip area. Also, this circuit is combined with an optimum noise match technique to enhance the gain and improve the reverse isolation. This circuit operates at a low supply voltage of 1 V to achieve low power consumption.

Gate inductor impedance matching can be divided into two categories, series and shunt inductor matching, as shown in Fig. 2. Compared with the series inductor matching (a), the
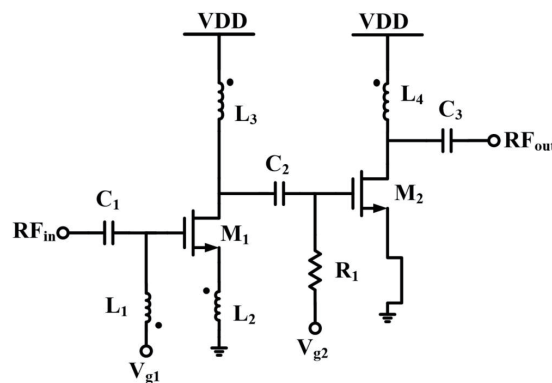

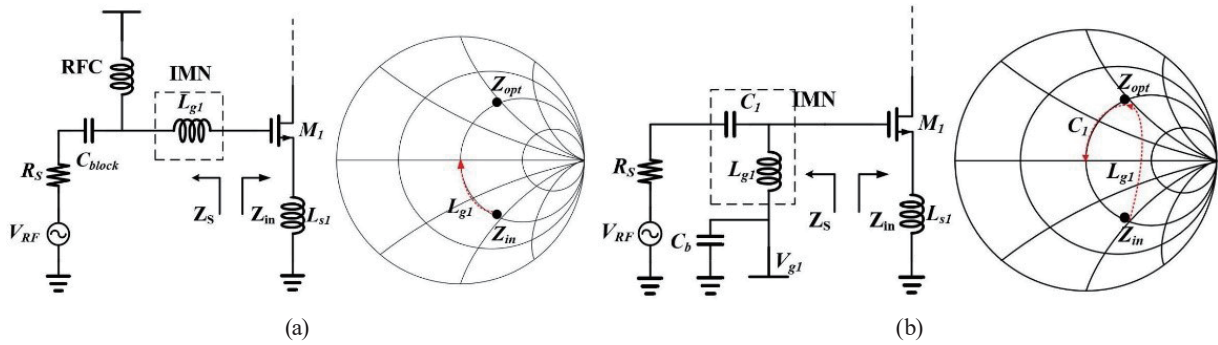Fig. 1.   Circuit schematic of proposed dual-feedback LNA.

Fig. 2.   (Color online) (a) Series inductor matching and (b) shunt inductor matching.

shunt inductor matching (b) has higher noise matching and frequency response. For the input matching of the design, in order to obtain the lowest noise, the power side looking into impedance should choose $Z_S = Z^*$, and the circuit input impedance should be selected as $Z_{in} = Z^*_S$.

Transistor gate and drain capacitance is a parasitic capacitance that cannot be avoided, and the parasitic capacitance provides a non-inverting signal path that causes severe attenuation of the amplifier gain. This path also enables reverse isolation and causes rapid serious deterioration that not only affects the stability, but also increases the difficulty in design.

$$f_t = \frac{g_m}{2\pi \left(C_{gs} + C_{gd} \right)}$$ (1)

Here, g_m is the transconductance of MOSFET and also C_{gs} and C_{gd}.

The inductor is tuned to match the transistor parasitic capacitance, and the resonant frequency of the path becomes a high-impedance state. Hence, the gain and reverse isolation are improved. Two inductor winding transformers (L_3 and L_4) further reduce the chip area. The mutual coupling of the transformers is used to eliminate Miller capacitance and improve reverse isolation.

The proposed K-band dual-feedback LNA achieves low voltage and power consumption. It uses double transformer feedback to reduce the chip area and improve the gain and reverse isolation, giving this LNA excellent performance.

Agilent Design System (ADS) software is used to simulate the circuit, and Taiwan Semiconductor Manufacturing Corporation (TSMC) provides a useful and accurate model. We use ADS Momentum to perform a full-wave electromagnetic simulation of the passive part. The circuit layout is also designed simultaneously. The difference between the results of a pre-layout simulation and a post-layout simulation is negligible. However, process variations still exist, although their impact is small. The simulated input and output return losses at 23 GHz are less than −10 dB. The reverse isolation at 23 GHz is below −50 dB. The gain at 23 GHz is below 10 dB. The noise at 23 GHz is below 5.2 dB. The −1 dB gain compression point in the simulation is −10.6 dBm. The parameters of the transistors and passive elements used in LNA design are shown in Table 1.

Table 1
Parameters of transistors and passive elements used in LNA design.

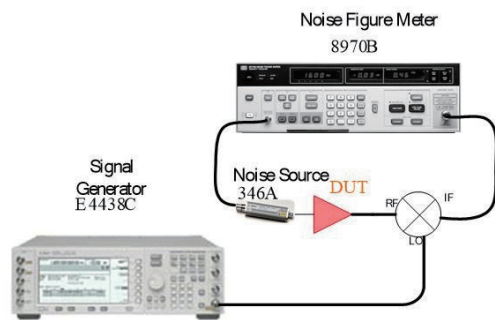| L_1	2 nH	R_1	7.9 kΩ
L_2	3.6 nH	C_1	245 fF
L_3	2.8 nH	C_2	20 fF
L_4	1.2 nH	C_3	20 fF
M_1	0.18 μm/2 μm/12	M_2	0.18 μm/2 μm/20

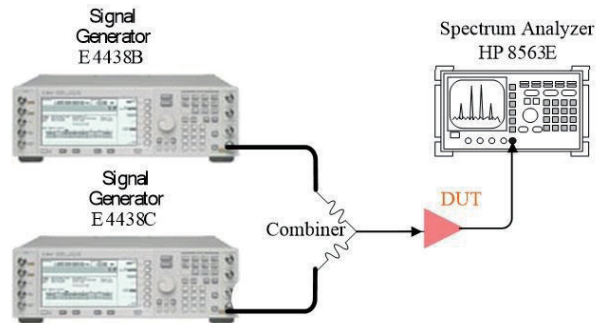Fig. 3.   (Color online) Schematic diagram of noise figure measurement.

Fig. 4.   (Color online) Schematic diagram of IIP3 measurement.

3.   Measurement and Experiment Results and Discussion

The proposed K-band LNA is fabricated for measurement. The PAD of the circuit satisfies the requirements for high-frequency measurement. A GSG probe and a PGP DC probe with a bypass capacitance are used for on-wafer measurement using a Cascade RF-1 measuring machine. In addition, the finished wafer with an AuSn die is attached to the high-frequency vehicle of a system to achieve good heat dissipation and grounding performance, and improve the accuracy of measurement. In DC voltage measurements, a gradually increasing voltage is applied to prevent the transistor from being burnt out by the sudden supply of too much current.

The instruments used for measurement are as follows:

• Network analyzer: gain and return loss
• Signal generator and spectrum analyzer: P_{1dB}, IIP3
• Noise figure meter: noise figure

Figures 3 and 4 show schematic diagrams of the noise figure and IIP3 measurement, respectively. A micrograph of the LNA chip is shown in Fig. 5. The transformer-based LNA occupies an area of 0.22 mm². The supply voltage is 1 V, and the power consumption is 5.4 mW.

S-parameter measurement results are shown in Figs. 6–9. The input return loss at 23 GHz is less than −10 dB, the output return loss at 23 GHz is less than −10 dB, and the reverse isolation at 23 GHz is below −50 dB. Both input and output return losses match the specifications. The measured gains at 23 GHz were 10 and 2dB lower than the simulated gain. This small difference may have been due to parasitic effects.
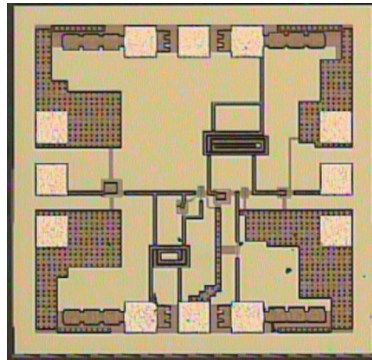
Fig. 5.   (Color online) Micrograph of fabricated LNA.
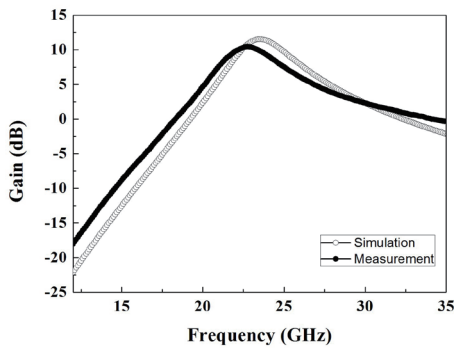

Fig. 6.   Measured and simulated gains of fabricated LNA as functions of frequency at 23 GHz.
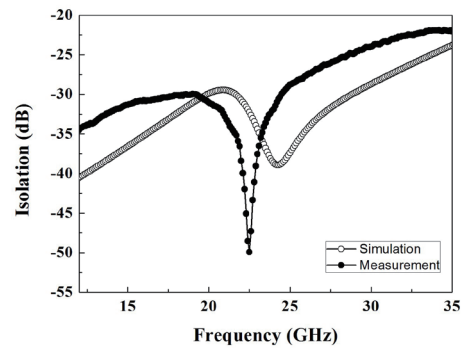

Fig. 7.   Measured and simulated isolation values of fabricated LNA as functions of frequency at 23 GHz.
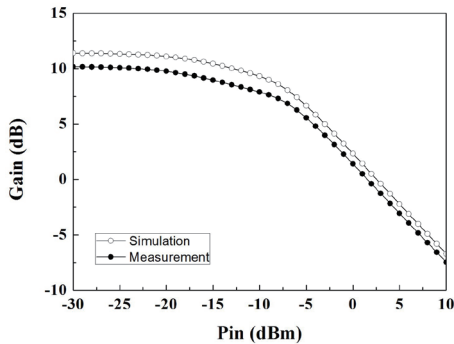

Fig. 8.   Measured and simulated P_{1dB} values of fabricated LNA as functions of frequency at 23 GHz.
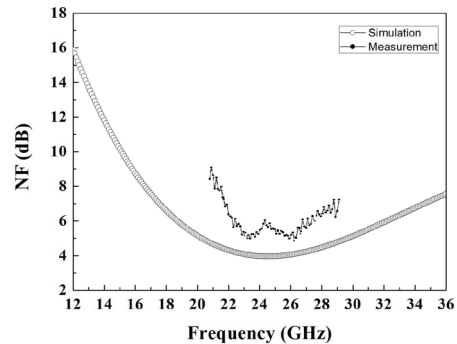

Fig. 9.   Measured and simulated noise figures of fabricated LNA as functions of frequency at 23 GHz.

Figure 9 shows the noise figure result. It can be seen that the minimum noise figure is approximately 5.2 dB. Figure 8 shows the measured and simulated P_{1dB} values as functions of frequency at 23 GHz; the P_{1dB} is about −10.6 dBm. Table 2 shows the performance characteristics of the proposed LNAs compared with those of other reported LNAs.[3−6] The proposed LNA has a small chip size with low power consumption.

Table 2
Performance characteristics of the reported LNAs.

Ref.	3	4	5	6	This work
Process	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	45 nm CMOS	0.18 µm CMOS
Freq. (GHz)	22	23.7	24	23	23
Gain (dB)	10.1	12.86	17	7.1	10.6
P_{1dB} (dBm)	NA	−11.1	−14	−9.5	−10.6
NF (dB)	4.3	5.6	5.9	4	5.2
IIP3 (dBm)	−1	2.04	−4	2.25	1
Chip size (mm^2)	0.13	0.74	0.39	0.81	0.22
P_{DC} (mW)	7.2	54	27	3.6	5.4

4. Conclusion

In this study, we successfully used a dual-feedback K-band LNA to obtain a high-performance 23 GHz LNA. The circuit consists of two cascaded common-source configurations composed of a LNA transistor gate source-side end and a joined transformer feedback mechanism. By using a transformer neutralization technique, the LNA achieves input and output return losses of less than −10 dB, a reverse isolation below −50 dB, a gain of 10.6 dB, a noise figure of 5.2 dB with a chip size of only 0.22 mm^2, and 5.4 mW power consumption. The transformer not only reduces the overall chip area but also improves the reverse isolation. This LNA is suitable for future K-band RF systems and sensor applications.

Acknowledgments

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