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Optimization of Ferroelectric Phase in Poly(vinylidene fluoride co-hexafluoropropylene) under Different Annealing Conditions

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Field-effect transistors (FETs) are considered promising devices for future development owing to their application in large-area electronics. In this research, we focus on the fabrication and optimization of the ferroelectric phase of an FET by utilizing poly(vinylidene fluoride co-hexafluoropropylene) [P(VDF-co-HFP)] as a gate insulator and pentacene as an organic semiconductor under different annealing conditions. The FET was fabricated by mixing P(VDF-co-HFP) with a preformulated concentration of methyl ethyl ketone and by spin coating this mixture onto the gate electrode. The obtained gate insulator was annealed for 1 h at temperatures ranging from 110 to 170 °C in increments of 20 °C for an analysis of the underlying effect of temperature on the properties of P(VDF-co-HFP). The results show that the FET fabricated at the optimized temperature of 150 °C exhibits significantly improved hysteresis loop and on/off ratio. This investigation led to the development of a simple method of designing and preparing an FET with excellent electrical characteristics.

1. Introduction

Current research pertaining to electronic devices has extensively focused on the development of memory devices that incorporate an organic moiety, which enables the fabrication of cost-effective thin flexible electronic devices.[1,2] Several researchers have been focusing on organic memory devices such as field-effect transistors (FETs),[3] light-emitting diodes (LEDs),[4] and flash memory,[5] characterized by high speed and low power dissipation. These appealing features have increased the demand for electronic applications such as sensors, actuators, and organic nonvolatile memories.[6] Indeed, FETs are the most promising memory devices for large-scale electronics. Recently, research studies of FETs using ferroelectric polymers have actively been conducted. However, most of them are based on poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)], and various materials should be studied in order to develop ferroelectric FET technology.

Most polymers are inert in terms of electronic application. However, a few polymers

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and copolymers are capable of undergoing structural deformations in the presence of an applied electric field and, interestingly, show a positive response towards conductivity. Examples of polymers with these properties are poly(vinylidene fluoride) (PVDF),[7] poly(vinyl cinnamate) (PVCi),[8] and polyvinyl alcohol (PVA).[9] Indeed, PVDF and its copolymer poly(vinylidene fluoride co-hexafluoropropylene) P(VDF-co-HFP) are remarkably active with outstanding features including excellent mechanical strength and electrical energy density. It is well recognized that ferroelectric polymers are advantageous for application in various sensors because the polarization in these polymers is affected by external conditions, including an electric field, mechanical deformation, temperature, and chemical and biological factors.[10] Furthermore, because these polymers can be processed at annealing temperatures below 200 °C, it has found widespread application in scientific research and industrial processes.[11–13] Hence, the demand for incorporating these polymers in lithium-ion batteries,[14] thin-film transistors (TFTs),[15] and radio-frequency identification (RFID) tags [16] had been growing. In fact, P(VDF-co-HFP) consists of both crystalline and amorphous phases, acquired from the monomers VDF and HFP, which exhibit excellent chemical stability and plasticity.[17]

On the other hand, annealing temperature is one of the most important factors for the fabrication of FETs because this temperature affects multiple crystalline phases, α, β, γ, δ, and ε.[18] Among these phases, the polar β-phase has an all-trans (TTTT) configuration with superior characteristics in terms of the ferroelectric, polarization, and piezoelectric effects, which has its origins in the dipole moments arising from the electronegativity of hydrogen and fluorine atoms.[19] Hence, to promote the formation of the ferroelectric β-phase in P(VDF-co-HFP), the fabricated FETs are annealed at different temperatures after film formation. The effect of the annealing temperature on the PVDF film can be analyzed by examining the surface morphology, degree of crystallinity, and molecular chain orientation.

In fact, the fabrication process plays a vital role in determining the ferroelectric nature of PVDF. The ferroelectric nature (β-phase) of PVDF films can be enhanced in various ways; for instance, it could be affected by the method used for film fabrication (spin coating,[6] solution casting,[7] or dip coating[20]). However, obtaining a uniform film that exhibits the β-phase in PVDF remains a great challenge. To date, ferroelectric FETs fabricated by spin coating and incorporating the P(VDF-co-HFP) copolymer have been studied extensively, but little information on their electrical performance based on the temperature effect has been reported. Therefore, in this study, as part of a comprehensive research effort, we examine the effect of temperature on the electrical characteristics of FETs, including the output, transfer, hysteresis, and memory window.

In the light of the above-mentioned reported results, the present research mainly focused on the points highlighted here: (1) fabrication of organic FETs by utilizing the P(VDF-co-HFP) copolymer via spin coating and (2) electrical characterizations within a certain temperature range to determine the optimal conditions. The on/off ratio and drain current were optimized by varying the temperature. Simultaneously, the resultant device exhibits nonvolatile memory characteristics that arise from the spontaneous polarization in ferroelectric materials.

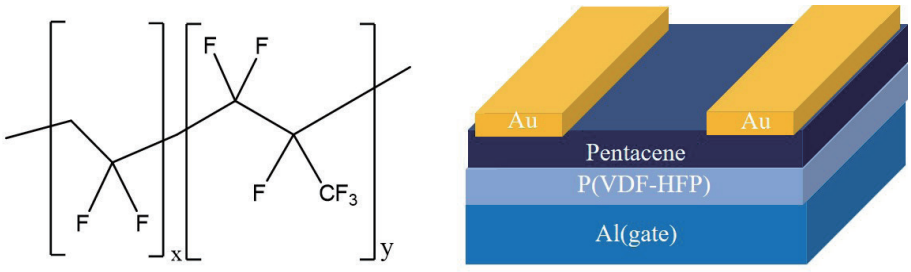
2. Experimental Methods

P(VDF-co-HFP) [average molecular weight (Mw) ~400000 g/mol], methyl ethyl ketone (MEK) (molar mass ~72.1 g/mol), and pentacene were supplied by Sigma Aldrich Korea. Figure 1(a) shows the chemical structure of the P(VDF-co-HFP) polymer.

2.1 Fabrication of P(VDF-co-HFP) FET

An FET with a bottom-gate/top-contact (BGTC) structure was fabricated on a glass substrate. The glass substrate was sequentially cleaned with acetone, isopropyl alcohol, and deionized (DI) water in an ultrasonic bath and subsequently dried with nitrogen gas. The structure of the FET comprising Al/P(VDF-co-HFP)/pentacene/Au layers is schematically depicted in Fig. 1(b). Then, a solution of the polymer was prepared by dissolving P(VDF-co-HFP) in solvent (MEK) at 7 wt% concentration. The resultant mixture was continuously stirred by using a magnetic stirrer for 3 h until polymeric pellets were dissolved completely.

Initially, the bottom-gate Al electrode was deposited on the glass substrate by thermal evaporation. The Al deposition rate was maintained between 0.6 and 1.0 Å/s, and the layer thickness was approximately 50 nm. Thereafter, a 7 wt% P(VDF-co-HFP) solution was spin-coated on the Al gate electrode at 4000 rpm for 35 s. The coated film was subsequently annealed at different temperatures of 110, 130, 150, and 170 °C at which the films had thicknesses of 822, 650, 646, and 625 nm, respectively; annealing at each of these temperatures was carried out for an hour to analyze the effect of temperature on the electrical characteristics. The capacitance values of the Al/insulator/Al capacitors were also measured by applying a small ac signal with an amplitude of 10 mV at 100 kHz. In our results, the capacitance per unit area values of the fabricated P(VDF-co-HFP) films annealed at 110, 130, 150, and 170 °C were approximately 2.47, 2.42, 2.49, and 2.06 nF/cm^2, respectively. The pentacene active layer was thermally deposited at a rate of 0.2 Å/s to attain a thickness of 40 nm. Finally, Au (source/drain) top contacts were formed by thermal evaporation with a thickness of 30 nm. All the depositions were carried out by controlling the chamber pressure at approximately 6×10^6 Torr or less. The channel length and width of the fabricated FETs are 100 and 800 mm, respectively.



(a) (b)

Fig. 1. (Color online) (a) Schematic structure of the fabricated BGTC FET and (b) chemical structure of the P(VDF-co-HFP) polymer.

2.2 Characterizations

2.2.1 Electrical characteristics

The electrical characteristics, i.e., current–voltage (I–V) characteristics, of FETs were measured under ambient conditions by using a semiconductor parameter analyzer (model: EL421C).

2.2.2 Atomic force microscopy (AFM)

AFM was used to analyze the surface morphologies of the fabricated P(VDF-co-HFP) and pentacene thin films. AFM images were obtained in air and at room temperature.

2.2.3 Fourier transform infrared (FTIR) spectroscopy

FTIR measurements were performed to confirm the β-phase in the P(VDF-co-HFP) films.

3. Results and Discussion

3.1 Electrical characteristics

The electrical properties of the fabricated pentacene FETs were analyzed at different temperatures to determine their optimal significant characteristics. The output characteristics of the FETs are shown in Figs. 2(a)–2(d). The maximum drain current (I_{dmax}) values obtained at 110, 130, 150, and 170 °C for the FETs are −0.08, −0.10, −0.18, and −0.009 μA, respectively.

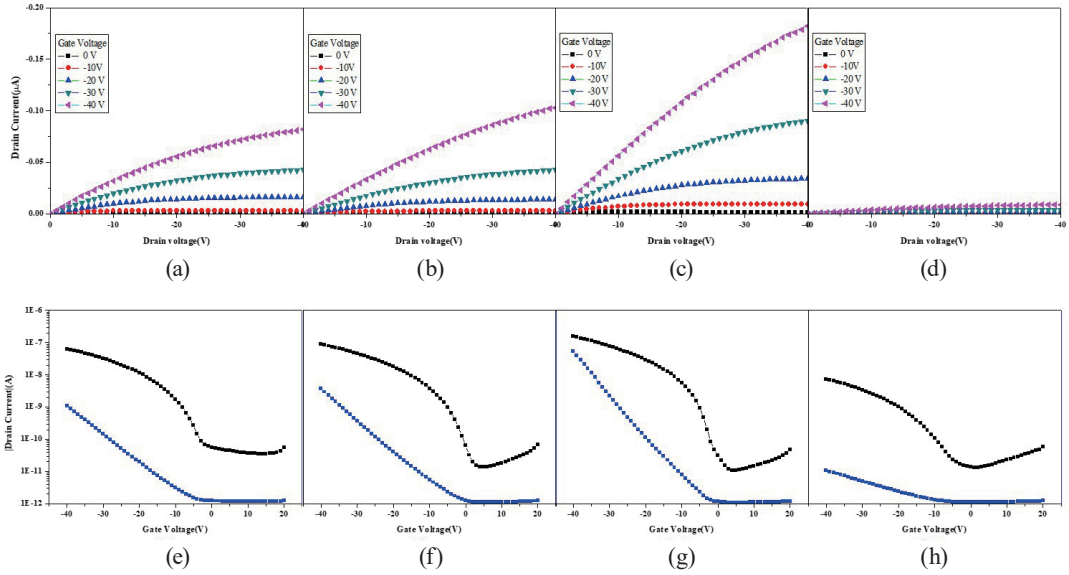


Fig. 2. (Color online) Output (I_D–V_D) characteristics of the FETs at (a) 110, (b) 130, (c) 150, and (d) 170 °C at an applied gate voltage of 0 to −40 V with a step of −10 V. (e)–(h) Corresponding transfer characteristics of the P(VDF-co-HFP) films at a gate voltage in the range from 20 to −40 V and drain voltage of −40 V.

A quadratic increase in drain currents (I_d) with an increase in negative gate bias is observed, and the obtained values saturate owing to a pinch-off behavior in the FET channel region. The drain currents of the FETs are shown to increase with temperature up to 150 °C and a sudden decrease in the current is observed when the temperature is raised to 170 °C. Nevertheless, the fact that the highest drain current is obtained at 150 °C implies a stronger current flow than under other conditions. This may result from the high dipole moment in the P(VDF-co-HFP) film annealed at 150 °C. The sudden decrease in drain current may be attributed to the polymer films undergoing a phase transition to the α-phase that is annealed above its melting temperature (*Tm*). Additional transfer characteristics are shown in Figs. 2(e)–2(h) and Table 1 shows the following electrical parameters: the on/off ratio, threshold voltage, and field-effect mobility under different annealing temperatures. All the parameters in Table 1 follow a trend similar to that of the drain current. The FET with the P(VDF-co-HFP) film annealed at 150 °C has superior characteristics with high on/off ratio and field-effect mobility of approximately 10^4 and 0.1 $cm^2/V{\cdot}s$, respectively, both of which result from the high surface charge densities at the interface of the P(VDF-co-HFP) insulator and the pentacene semiconductor.[21] Thus, the temperature can be concluded to play an important role in the electrical performance of the FETs with the P(VDF-co-HFP) insulators.

The memory window (ΔV_T) of the FETs with the P(VDF-co-HFP) films was investigated by examining the voltage width of hysteresis loops at different annealing temperatures. This property generally originates from the ferroelectric nature of polymer insulators, which is one of the most important parameters and is defined as the difference between the upward and downward threshold bias sweeps. The clockwise hysteresis loops of the FETs with the P(VDF-co-HFP) films at different temperatures, which have their origins in the ferroelectric polarization of the P(VDF-co-HFP) films, are shown in Figs. 3(a)–3(e). The memory windows (ΔV_T) extracted from the hysteresis loops at the annealing temperatures of 110, 130, 150, and 170 °C are 5, 15.8, 22.3, and 3.2 V, respectively, as shown in Fig. 3(f). However, the largest memory window (ΔV_T) of approximately 22.3 V is attained at 150 °C and might be due to the enhanced ferroelectric β-phase of the P(VDF-co-HFP) film. On the other hand, the sudden decrease in the size of the memory window to 3.2 V at 170 °C confirms the effect of the annealing temperature on the ferroelectric properties of the P(VDF-co-HFP) films.

3.2 AFM and FTIR characteristics of P(VDF-co-HFP) films

AFM was used to analyze the surface morphology of the P(VDF-co-HFP) films at various annealing temperatures, because it was obvious that temperature greatly affects the properties

Table 1
Electrical parameters of the fabricated FETs.

Temperature (°C)	I_{on}/I_{off}	V_{th} (V)	Mobility (μ)
110	1.2×10^2	−5.5	0.01
130	6.7×10^3	−4.7	0.08
150	1.5×10^4	−4.8	0.1
170	5.6×10^2	−8.2	0.003

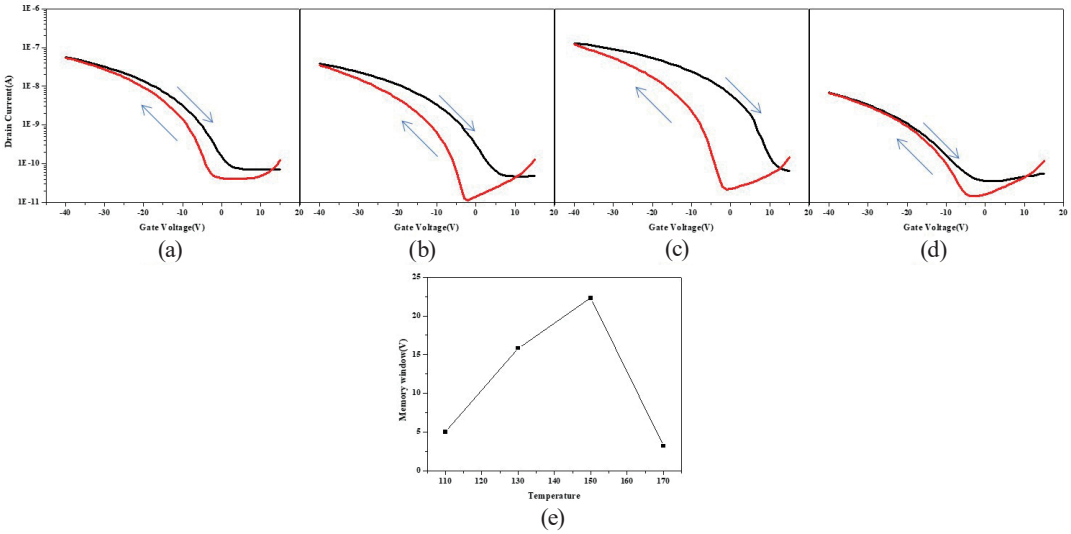
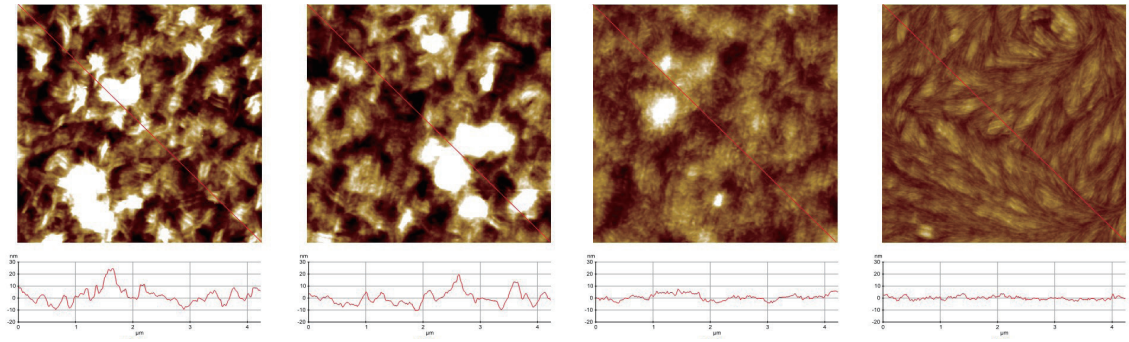


Fig. 3. (Color online) Hysteresis curves of P(VDF-co-HFP)-based FETs at (a) 110, (b) 130, (c) 150, and (d) 170 °C. (e) Memory window of the P(VDF-co-HFP) films annealed at different temperatures.

of the P(VDF-co-HFP) films, which also affects the FET performance. The AFM images of the P(VDF-co-HFP) films annealed at various temperatures are as shown in Figs. 4(a)–4(d). The root-mean-square (RMS) roughness values of the polymer films annealed at 110, 130, 150, and 170 °C were derived from the AFM images as 6.54, 6.43, 2.81, and 1.46 nm, respectively. The polymer films exhibit a coarse surface at 110 and 130 °C, whereas at 150 °C, the surface morphology significantly changed to a broadened structure with a uniform surface, indicating the optimal temperature. At temperatures above 150 °C, the surface of the P(VDF-co-HFP) polymer film loses its structure because of the effect of temperature. However, the surface roughness of the polymer film annealed at the optimized temperature (150 °C) is rather high (approximately 2.81 nm) compared with that of the film annealed at 170 °C (1.46 nm). This is mainly due to uniformly arranged polymer molecules that result in an all-trans configuration.[22]

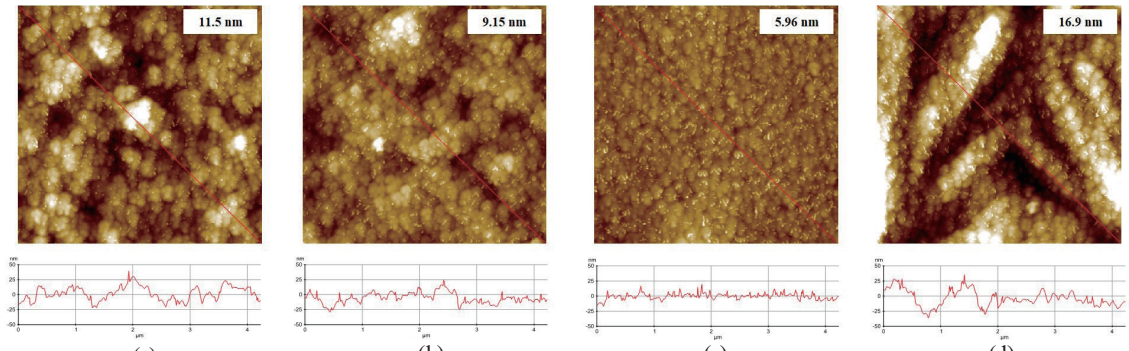
Similarly, AFM images of the surface morphology of pentacene films deposited on the polymer films annealed at different temperatures are shown in Figs. 5(a)–5(d). The RMS roughness values of pentacene films deposited on the P(VDF-co-HFP) films annealed at 110, 130, 150, and 170 °C are 11.56, 9.15, 5.96, and 16.9 nm, respectively. Clearly, the surface morphology of the pentacene film for the annealing condition of P(VDF-co-HFP) at 150 °C is smoothest, suggesting that pentacene molecules are arranged more uniformly. This possibly explains the superior performance characteristic, such as the highest drain current and field-effect mobility, of the pentacene FET with the P(VDF-co-HFP) film annealed at 150 °C in our results. These results suggest that the annealing temperature extensively affects the electrical characteristics of FETs with high drain current and on/off ratio.

FTIR measurements were carried out and the results are shown in Fig. 6. P(VDF-co-HFP) is known to be a semicrystalline polymer, indicating that FTIR spectra of the fabricated P(VDF-co-HFP) films contain some crystalline and amorphous phase-related peaks. In our results,



(a) (b) (c) (d)

Fig. 4. (Color online) AFM images (3 × 3 μm^2) of the P(VDF-co-HFP) films annealed at (a) 110, (b) 130, (c) 150, and (d) 170 °C.



(a) (b) (c) (d)

Fig. 5. (Color online) AFM images (3 × 3 μm^2) of corresponding pentacene films grown on P(VDF-co-HFP) films annealed at (a) 110, (b) 130, (c) 150, and (d) 170 °C.

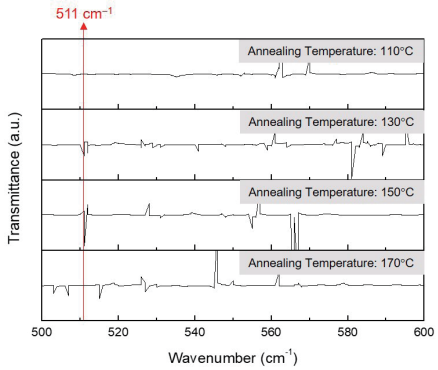


Fig. 6. (Color online) FTIR spectra of the P(VDF-co-HFP) films annealed at different temperatures.

the P(VDF-co-HFP) film annealed at 110 °C exhibits weaker and fewer peaks than other films. This is possibly due to the amorphous phase. On the other hand, the P(VDF-co-HFP) films annealed at 130 and 150 °C show a typical ferroelectric β-phase peak at a wavenumber of approximately 511 cm^{-1}.[23] Indeed, the ferroelectric β-phase peak is more remarkable in the P(VDF-co-HFP) film annealed at 150 °C. Therefore, the notable memory window property of the transistor having the P(VDF-co-HFP) film annealed at 150 °C can be attributed to the

ferroelectric β-phase. However, the ferroelectric β-phase peak is not observed in the P(VDF-co-HFP) film annealed at 170 °C. This may prove the change in film crystallinity, which is explained through a uniform arrangement of polymer molecules, i.e., all-trans configuration, in Fig. 4. Consequently, it is concluded that the annealing temperature significantly governs the morphological and crystalline properties of P(VDF-co-HFP) films.

4. Conclusion

This investigation led to the fabrication of a low-cost and nontoxic FET, which is based on an organic material and was obtained via a simple technique of spin coating. The thin film was fabricated by using pentacene as an active layer and 7 wt% P(VDF-co-HFP) in MEK as the ferroelectric polymer. The annealing temperature is an important parameter that affects the electrical properties of an FET. The polymer film was annealed at temperatures ranging from 110 to 170 °C in increments of 20 °C. A comparison of the electrical characteristics clearly shows that the output characteristics, memory window, and on/off ratio are significantly improved at the optimized annealing temperature of 150 °C. However, once the temperature is increased to 170 °C, the electrical characteristics start degrading. Similarly, the results of the surface morphology examination clearly showed the smooth surface of the pentacene film at the optimized temperature of 150 °C. In further studies, the crystallization behavior of thin P(VDF-co-HFP) films with annealing temperature should be investigated.

Acknowledgments

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