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Low-noise Analog Front-end with Chopper-stabilized Multipath Current-feedback Instrumentation Amplifier for Resistive Sensors

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A low-noise analog front-end (AFE) with chopper-stabilized multipath current-feedback instrumentation amplifier (CFIA) for resistive sensors is proposed. Low-noise techniques are essential for the operation of precise resistive sensors, and chopper stabilization techniques have been commonly implemented in previous studies. However, techniques that are only based on chopper stabilization suffer from the disadvantage of a low bandwidth. To address this problem, a multipath operational amplifier is implemented in this work. Also, the chopper stabilization technique is implemented in the low-frequency path of a multipath operational amplifier. This chopper stabilization technique causes the "ripple" generated by the offset voltage. A ripple rejection loop in the low-frequency path is utilized to remove this ripple. In addition, a successive approximation register (SAR) analog-to-digital converter (ADC) is used to convert the measured analog signal into a digital output. The converter has an effective number of bits (ENOBs) of 11.02 and a signal-to-noise and distortion ratio (SNDR) of 75.68 dB. The resistive AFE with SAR ADC is designed using a 0.18 μm complementary metal-oxide-semiconductor (CMOS) process with an active area of 8.6 mm^2. It operates at 2.56 mW with a 1.8 V supply and has an input-referred noise of 0.29 μV_{rms} in the range of 1 to 100 Hz.

1. Introduction

Recently, with the development of smart devices such as smart phones and autonomous vehicles, the importance of resistive sensors based on the Wheatstone bridge configurations and resistive analog front-end (AFE) has been gradually increasing.[1] Resistive sensors are utilized in a wide variety of applications such as pressure sensors,[2] gas sensors,[3,4] and touch screens.[5] There are two approaches to the resistive AFE design of these sensors.[6,7] One is resistance-to-

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frequency conversion,[8–10] and the other is resistance-to-voltage conversion.[1,11] The resistance-to-frequency conversion is a method of counting the number of oscillations according to the resistance. The architecture is simple but results in significant power consumption. Moreover, the process has a low conversion rate in a wide operating range.[11]

In contrast, the resistance-to-voltage conversion has a relatively large dynamic range but can produce nonlinear outputs owing to the effects of noise and the nonzero offset of the operational amplifier. To minimize this nonlinearity, a precise instrumentation amplifier (IA) with low noise and offset is required. In addition, the precise IA should have a large common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and fine noise efficiency factor.[12]

In recent years, current feedback instrumentation amplifiers (CFIAs) have been actively investigated. A conventional CFIA is composed of two stages.[13] However, these devices suffer from noise and offset. The chopper stabilization technique[1,12–14] and auto-zero technique [15,16] are commonly implemented for addressing these issues. Of the two methods, the auto-zero technique causes a switching noise problem due to sampling and increases in the baseband noise as a result of noise folding.[16] For this reason, the chopper stabilization technique is preferred for low-noise circuits. However, existing operational amplifiers that only use chopper stabilization have the disadvantage of a low bandwidth.

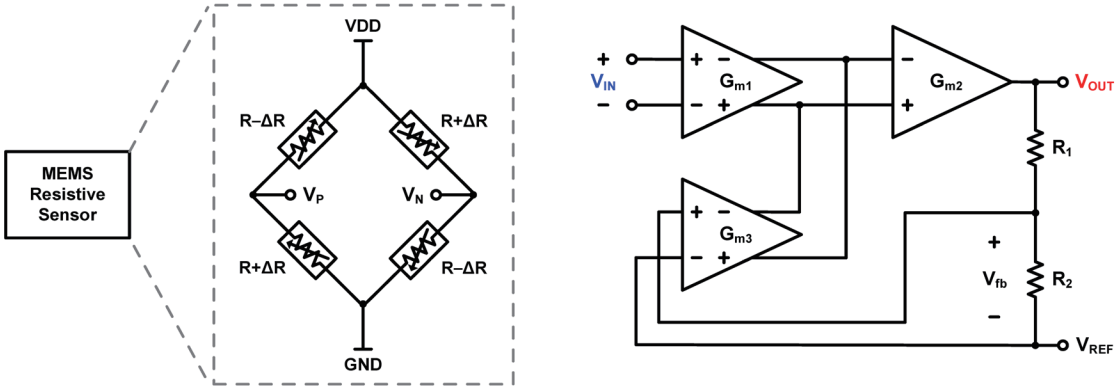
In this report, a multipath operational amplifier with high- and low-frequency paths is used for a higher bandwidth. A chopper stabilization technique within the low-frequency path results in a "ripple", in which the offset voltage of the IA is modulated to the carrier frequency, and a ripple rejection loop is applied to minimize this effect. A small input signal is amplified by the IA, which consists of multipath operational amplifiers and a fully differential amplifier. Also, a successive approximation register (SAR) analog-to-digital converter (ADC) is implemented to convert an analog signal to a digital output. The proposed 12-bit SAR ADC uses a resistor–capacitor (R–C) hybrid structure to reduce the size of the digital-to-analog converter (DAC). The resistive DAC (RDAC) determines the lower 4-bit, and the remaining upper 8-bit is determined by the capacitive DAC (CDAC). As a result, the total number of unit capacitors is reduced by 2^4 times compared with the conventional capacitive DAC. In the following sections, we discuss the structure of the proposed resistive AFE and multipath operational amplifiers in detail.

2. Proposed Resistive Analog Front-end with Multipath Operational Amplifier

The resistive AFE with the multipath operational amplifiers is presented in this section. In Sect. 2.1, we discuss the top schematic and the sub-blocks of the resistive AFE. In Sect. 2.2, we present the schematic and operation principle of a multipath operational amplifier used as a differential amplifier in the IA stage.

2.1 Architecture and operating principle of proposed resistive AFE

The conventional micro-electromechanical system (MEMS) sensors such as pressure sensors, gas sensors, and touch sensors have three-dimensional structures that can be converted to resistive sensors as shown in Fig. 1(a) when they are converted to electrical structures. These



(a) (b)

Fig. 1. (Color online) Conventional architecture: (a) MEMS resistive sensors and (b) CFIA.

resistive sensors typically consist of a Wheatstone bridge structure and the output voltage is expressed as

$$V_P = \left(\frac{R+\Delta R}{R+\Delta R+R-\Delta R}\right)V_{DD},\ V_N = \left(\frac{R-\Delta R}{R+\Delta R+R-\Delta R}\right)V_{DD},\ V_{OUT} = V_P - V_N = \frac{\Delta R}{R}V_{DD}. \quad (1)$$

According to Eq. (1), the voltage input of the IA is proportional to ΔR, which is the change in the input resistance. In the case of an IA, a typical CFIA structure is often used, as shown in Fig. 1(b), and the output voltage is expressed as[17]

$$V_{OUT} = V_{REF} + \frac{R1+R2}{R2}V_{IN}. \quad (2)$$

In this structure, when a variation in the input common mode voltage occurs, a small current is generated at the output of G_{m1}, but this is absorbed by the common mode feedback circuit and does not give rise to a change in the final output voltage.

Another structure is the IA, which consists of a 3-operational amplifier used in this paper and illustrated in a gray dashed box in Fig. 2. The transfer function of this circuit is expressed as

$$\frac{V_{OUTP}-V_{OUTN}}{V_{INP}-V_{INN}} = \left(1+\frac{2Rf1}{R1}\right)\left(\frac{Rf2}{R2}\right). \quad (3)$$

In this paper, for low noise, the IA has the multipath operational amplifiers A_1 and A_2 and applies chopper stabilization inside the fully differential amplifier A_3. The proposed IA consists of the first stage (A_1 and A_2) and the second stage (A_3). The gain of each stage is controlled by 5-bit programmable resistors (R_1, R_2). Also, as an important factor for the precise IA, the CMRR is the product of the finite differential gain of the first stage and the finite CMRR of the second stage.[17]

As shown in Fig. 2, the output of the IA enters the input of the 12-bit SAR ADC through the low-pass filter (LPF) and the buffer. An R–C hybrid structure is implemented to reduce the area of the DAC in the SAR ADC, and this structure is shown in Fig. 3. The lower 4-bit has the RDAC structure and the remaining 8-bit has the CDAC structure. As a result, the total number of unit capacitors is reduced by 2^4 times compared with a conventional capacitive DAC. Also, the offset cancellation technique is implemented in the comparator to achieve low offsets and high linearity.

The final architecture of the proposed resistive AFE is illustrated in Fig. 2. This device includes an IA, a Sallen–Key LPF, a buffer, and a SAR ADC, the IA of which is configured using a multipath operational amplifier.

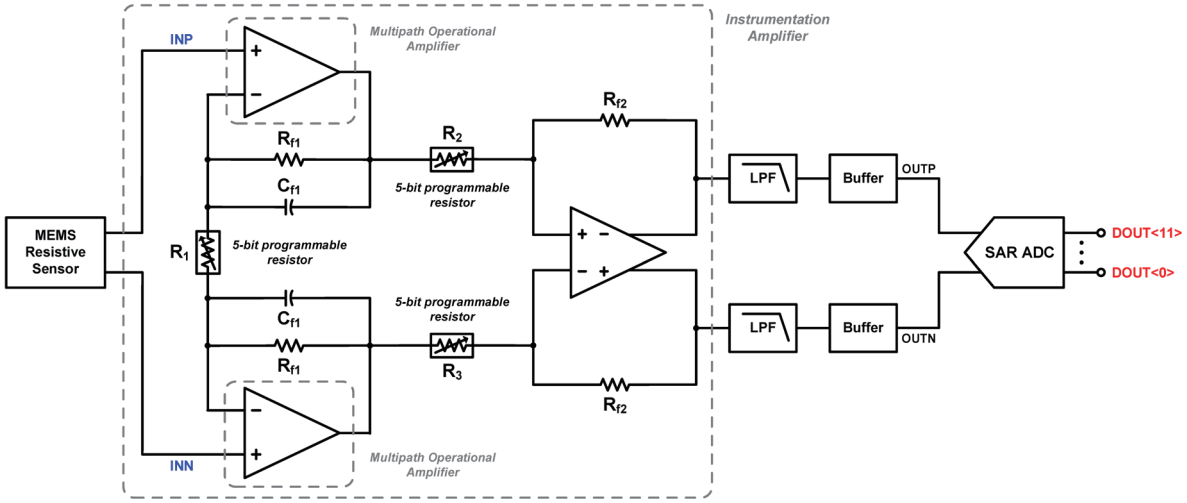


Fig. 2. (Color online) Architecture of the proposed resistive AFE.

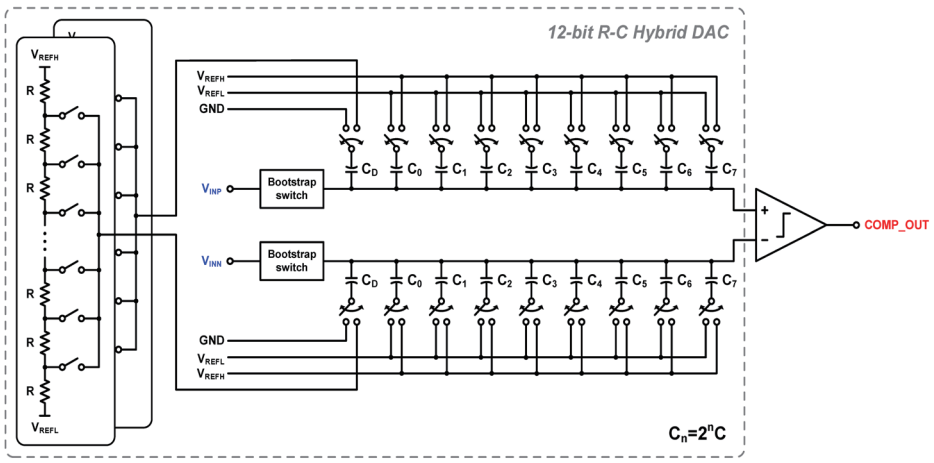


Fig. 3. (Color online) Proposed architecture of R–C hybrid DAC.

2.2 Architecture and operating principle of multipath operational amplifier

The architecture of the proposed multipath operational amplifier for low noise is shown in Fig. 4. A multipath operational amplifier is implemented to compensate for the low bandwidth, which is the primary disadvantage of a conventional amplifier implemented using only the chopper stabilization technique. This structure consists of a high-frequency path and a low-frequency path. Since a compensation method is generally implemented in operational amplifiers, it is difficult to control the high-frequency band poles because only two dominant poles generated in the two-stage amplifier can be controlled.[18] For this reason, the high-frequency bypass technique is often implemented for high-frequency and high-gain amplifiers, which are applied via G_{m1}, G_{m2}, and G_{m3}. Also, nested miller compensation is applied through C_5 to compensate for the high-frequency path. The schematic of G_{m1}, G_{m2}, and G_{m3}, which constitute the high-frequency path, is shown in Fig. 5. As shown in Fig. 5, the high-frequency path circuit consists of a PMOS input stage and a class AB output stage to ensure a small power and has a high slew rate.

The low-frequency path consists of G_{m4}, G_{m5}, and G_{m6}, and $1/f$ noise exists in the low-frequency band. Therefore, the chopper stabilization technique is implemented to lower it. The current output of the current adder of the low-frequency path is converted to a voltage through G_{m5}, which is then converted to a current through G_{m6}. The chopper stabilization technique in the low-frequency path generates a "ripple" where the input-referred offset is modulated at a high frequency. The ripple is suppressed by a ripple rejection loop consisting of G_{m7} and G_{m8}. The modulated ripple is demodulated by the ripple rejection loop, converted to a current by G_{m8}, and negatively fed back to the current adder.

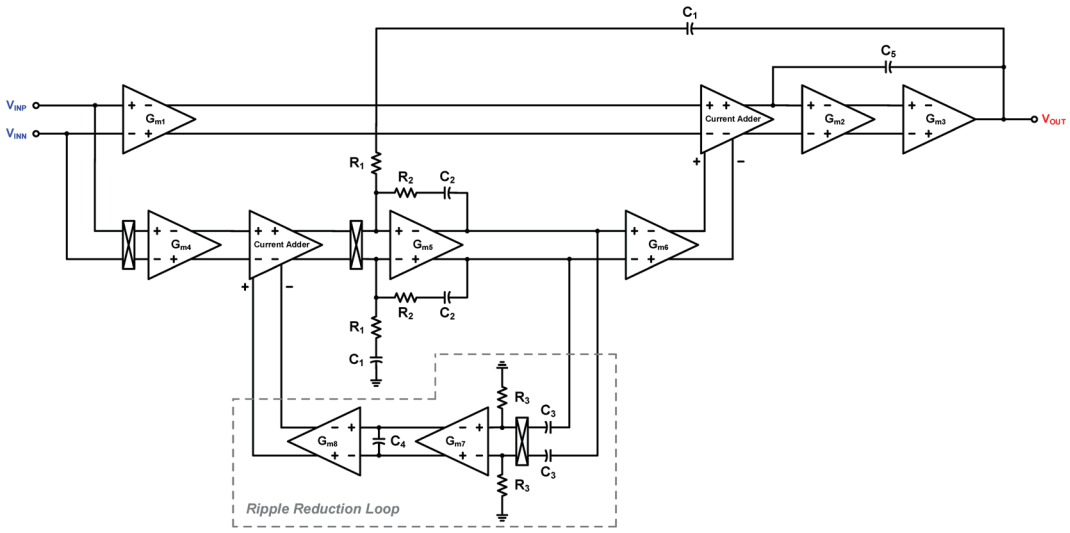


Fig. 4. (Color online) Architecture of the proposed multipath operational amplifier.

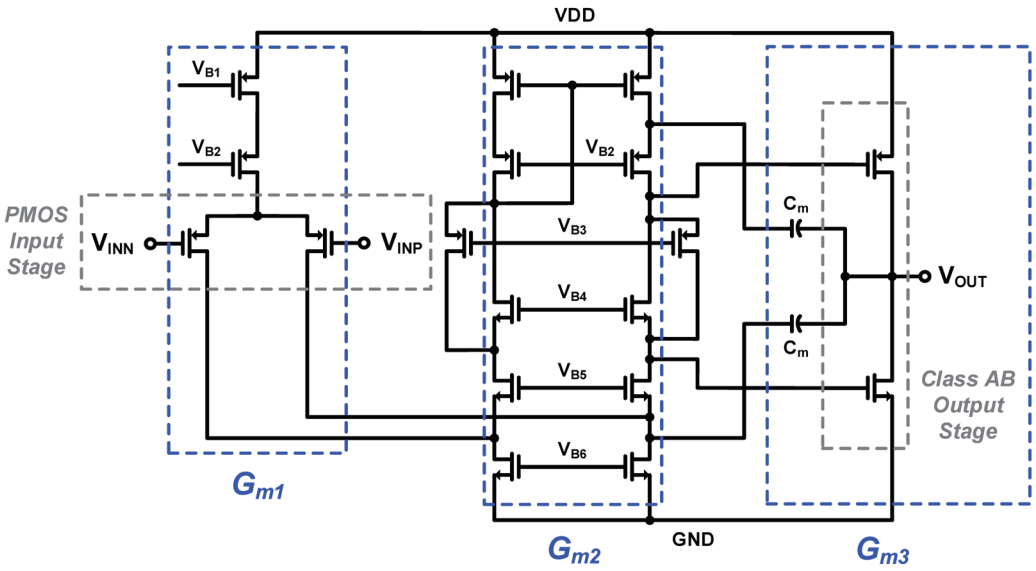


Fig. 5. (Color online) Schematic of G_{m1}, G_{m2}, and G_{m3} constituting the high-frequency path.

3. Simulation Results of Proposed Resistive Analog Front-end

The proposed resistive AFE is designed using a 0.18 μm one-polysilicon and six-metal layer (1P6M) complementary metal-oxide-semiconductor (CMOS) process with an active area of 8.6 mm^2. The layout of the designed resistive AFE is shown in Fig. 6. The open-loop gain and phase of the multipath operational amplifier in the IA are shown in Fig. 7. The DC gain of the multipath operational amplifier is 85 dB, the unit gain bandwidth (UGBW) is 1.32 MHz, and the phase margin is 72°.

Figure 8(a) shows the ripple results at the output when the ripple rejection loop is on and when it is off at an offset voltage of 1 mV. The preceding 1 mV offset voltage is modulated into the carrier frequency band owing to the chopper stabilization process and the ripple rejection loop is implemented to lower it. An output voltage of 25.03 mV_{pp} is obtained when the ripple rejection loop is not implemented, and 6.85 mV_{pp} when implemented. This shows that the ripple is effectively reduced when using the ripple rejection loop.

Figure 8(b) shows the transfer function of the IA. It has a gain that is adjustable by a 5-bit programmable resistor. The gain of the IA is inversely proportional to R_1 and R_2 according to Eq. (3). As a result, when the registers R_1 and R_2 are both high, the gain of the IA is minimized and measured at 38 dB. In contrast, when R_1 and R_2 registers are both low, the gain of the IA is maximized and measured at 96 dB. The gain of the IA needs to be adjusted appropriately according to the input voltage. This adjustable gain of the IA facilitates a wider input range.

Figure 9 shows the result of input-referred noise measurement according to chopper stabilization in the IA. The chopper stabilization in the IA is implemented in two places: the first is performed in the low-frequency path in the multipath operational amplifier and the second is executed in the fully differential amplifier. As shown in Fig. 9, the input-

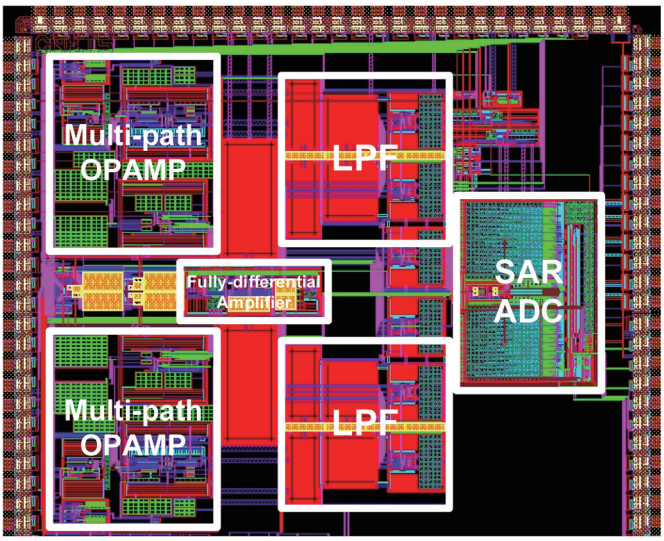
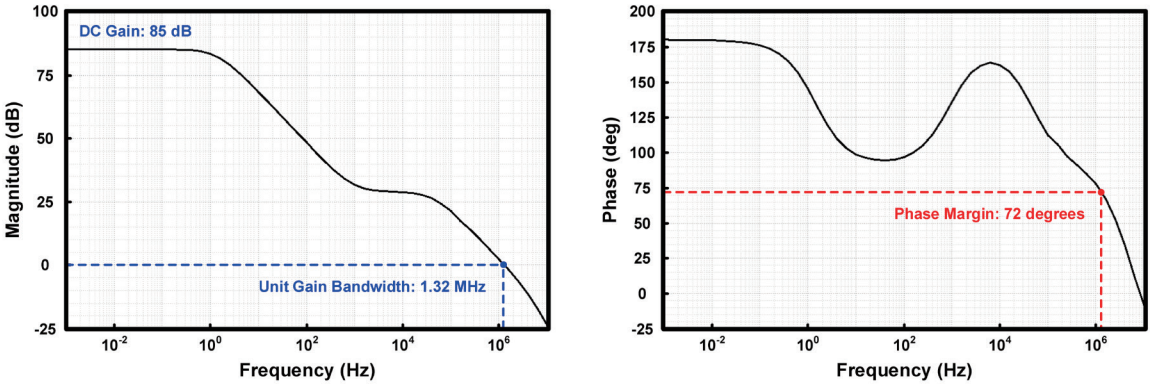
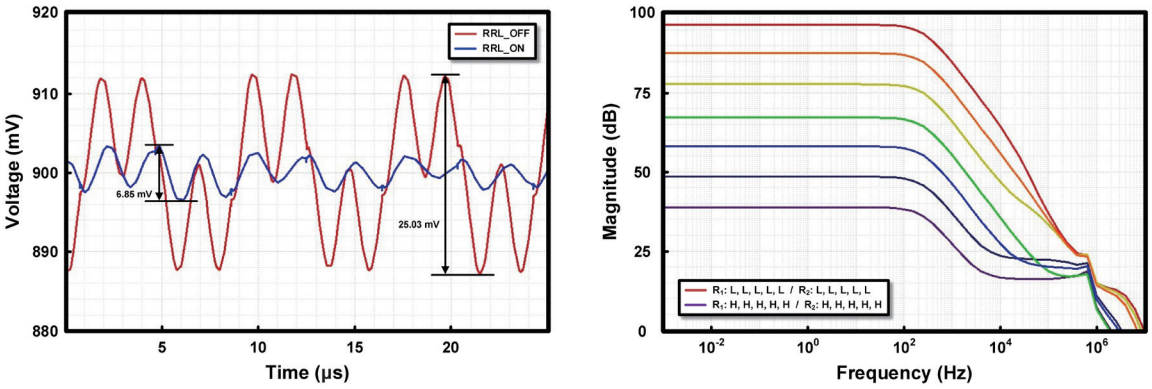


Fig. 6. (Color online) Layout of the designed resistive AFE.



(a) (b)

Fig. 7. (Color online) (a) Open-loop gain and (b) phase of the multipath operational amplifier.



(a) (b)

Fig. 8. (Color online) Simulation result of the proposed resistive AFE: (a) result of ripple when the ripple rejection loop is on and when it is off and (b) transfer function of the IA.

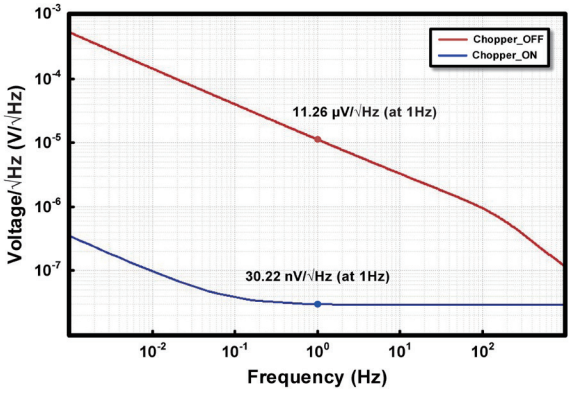


Fig. 9. (Color online) Input-referred noise measurement according to chopper stabilization.

Table 1
Comparison of performance of the resistive AFE with previous values.

	This work (Simulation)	Ref. 19	Ref. 11	Ref. 20
Year	2018	2016	2014	2013
Technology (μm)	0.18	0.065	0.18	0.18
Supply (V)	1.8	1	2.7	1.8
Power (μW)	2560	12.3	270	62
Gain (dB)	38–96	100	100	28.5
Input-referred noise (μV_{rms})	0.29	11	3.76	1.8
Techniques for IA	Chopper stabilization + multipath	Correlated double sampling	Chopper stabilization	Chopper stabilization
Ripple rejection loop	Y	N	N	N

referred noise is measured as 11.26 $\mu V/\sqrt{Hz}$ (at 1 Hz) without chopper stabilization, and as 30.22 $nV/\sqrt{Hz}$ (at 1 Hz) when chopper stabilization is implemented. The RMS noise density from 1 to 100 Hz is also measured as 0.29 μV_{rms} when chopper stabilization is performed and 22.58 μV_{rms} when chopper stabilization is not performed. As a result, it can be seen that the input-referred noise has a reduction effect of about 78 times when the chopper stabilization is performed, compared with the case when no chopper stabilization is performed.

The 12-bit SAR ADC implemented in this investigation achieves an effective number of bits (ENOBs) of 11.02 and a signal-to-noise and distortion ratio (SNDR) of 75.68 dB, and has a speed of 1 Ms/s for the conversion of the analog output from the IA to digital data. Comparison of the performance of the resistive AFE with previously reported values is summarized in Table 1.

4. Conclusions

A low-noise AFE with a chopper-stabilized multipath CFIA for resistive sensors is presented. The proposed resistive AFE with a SAR ADC is designed using a 0.18 μm 1P6M CMOS process with an active area of 8.6 mm^2. This resistive AFE operates at 2.56 mW with a 1.8 V supply. Simulation results show that the gain of the IA is adjustable from 38 to 96 dB

using a 5-bit programmable resister. In addition, it is confirmed that the chopper stabilization technique is effective in reducing the input-referred noise, and the ripple generated in the chopper stabilization process is also suppressed by the ripple rejection loop. As a result, the proposed resistive AFE has an input-referred noise of 0.29 μV_{rms} in the range of 1 to 100 Hz.

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