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Simulation on Junctionless Silicon Nanowire Devices for Implementation of Photodetection Circuit in Retinal Prosthesis

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Semiconductor nanowires have been studied owing to their excellent electrical properties. To implement an integrated system based on nanowires, well-aligned arrays of a nanowire are required for scalable and repeatable fabrication. In our previous results, a comparative study based on the current conduction mechanism of junctionless silicon nanowires was performed, and their characteristics were analyzed to offer a design guideline. Also, to implement a silicon-nanowire-based device, a top-down, wafer-level fabrication process of silicon-nanowire arrays on a flexible substrate was reported. The fabricated device consists of a voltage divider and a current driver in which silicon nanowires are used as a photodetector (PD) and field-effect transistors (FETs). The implemented silicon-nanowire-based circuit detects external light, generating a stimulation signal in proportion to the light intensity and transmitting the signal to a microelectrode. In this study, an analytical model based on a conduction mechanism of junctionless silicon nanowires is verified using a three-dimensional device simulator. Also, by applying the extracted electrical parameters of silicon-nanowire-based devices, the proposed photodetection circuit is simulated for the implementation of a photosensitive retinal prosthetic device. The results of this study can be applied to address novel silicon-nanowire-based neural stimulation devices and to guide the design of a high-resolution retinal prosthetic system.

1. Introduction

In the human eye, photoreceptor cells sense light and convert it into electrical signals that then stimulate optic nerves in the brain. The degeneration of the photoreceptors produces visual disorders such as retinitis pigmentosa (RP) and age-related macular degeneration (AMD), which affects more than 15 million people throughout the world.[1–3] Nevertheless, effective medical treatment methods for such diseases are not available. Even though the blind has irrecoverable photoreceptor degeneration, 78.4% of bipolar and 29.7% of retinal ganglion cells (RGCs) are still alive to transmit neural impulses.[4,5] Thus, through the electrical stimulation of the remaining neural network, vision can be restored.

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Several research groups worldwide have attempted to use electrical signals modulated by visual data obtained from external image acquisition devices.[6–8] For other approaches, integrating a solid-state photodiode into a microelectrode array (MEA) has been proposed.[9] For those devices, photodiodes are integrated with signal amplification circuits to increase and control the magnitudes of stimulation current at low light intensities. In our previous report, we have proposed light-responsive silicon-nanowire photodetectors (PDs) on a flexible substrate, which can convert visible light into electrical signals.[10] In the report, the devices using a top-down fabrication method have shown excellent potential for applications in retinal prosthetic systems with high photosensitivity, photoresponsivity, and mechanical flexibility. However, the proposed scheme generated insufficient photocurrents to stimulate RGCs, and the amplitude of the stimulation current had to be amplified. To achieve a sufficient current stimulus, a transimpedance amplifier has been integrated with silicon-nanowire PDs.[11,12] Despite the recent results, there remain problems to be resolved, such as the protection of electrodes from excessive charge injection, the avoidance of charge spreading due to a high-amplitude current stimulus, and cell necrosis due to the overheating of stimulator chips. Therefore, research on a gain-controllable scheme using silicon-nanowire devices to protect RGCs and electrodes is necessary. The gain-controllable scheme of the retinal prosthetic system using the silicon-nanowire-based photodetection circuit is shown in Fig. 1. The proposed method consists of a voltage divider and a current driver, and is implemented using silicon-nanowire PDs, silicon-nanowire field-effect transistors (FETs), and a microelectrode on a flexible substrate. The voltage divider with series-connected silicon-nanowire PD and FET generates control voltage (V_C) owing to the resistance variation from the external light intensity to the silicon-nanowire PD. In the current driver, where the silicon-nanowire FET and microelectrodes are connected in series, the current stimulus pulses can be delivered to the microelectrode by the amplitude-modulated driving current, which is proportional to the external light intensity.

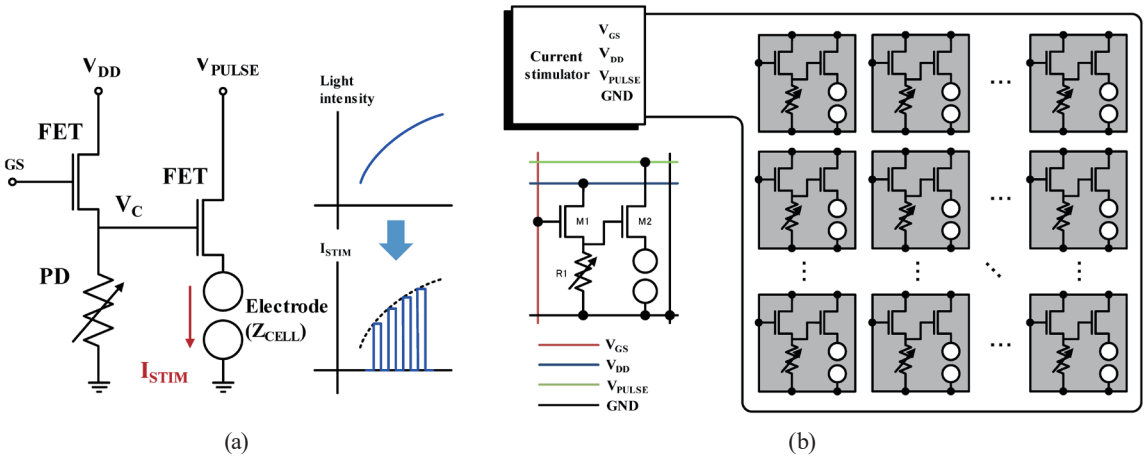


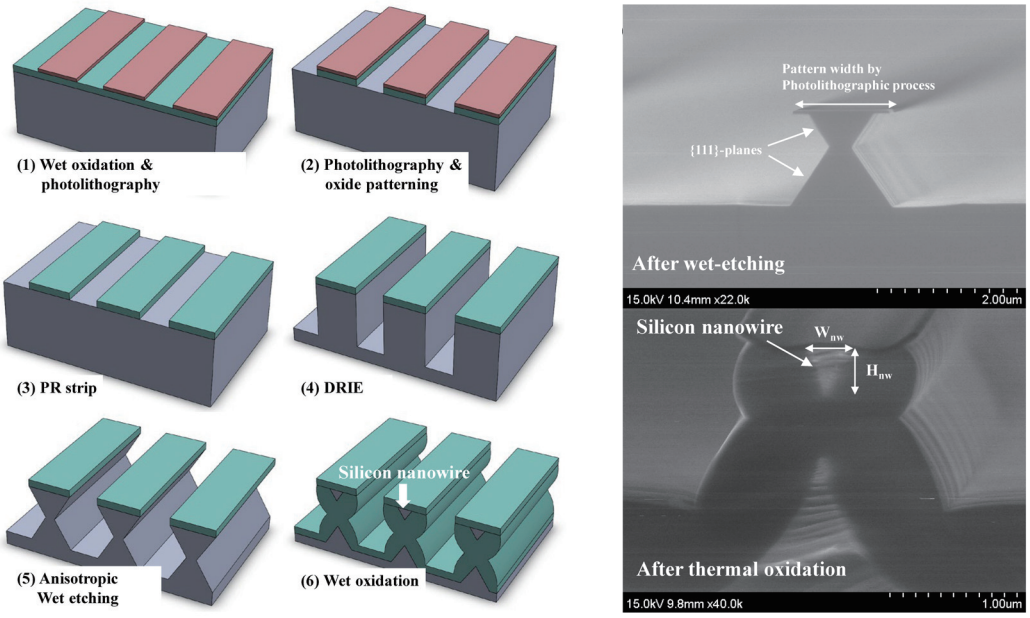
Fig. 1. (Color online) Schematic. (a) Operation of photodetection circuit. (b) Schematic of the PD-based retinal prosthetic system.

Although there has been much research on the development of various fabrication processes, few studies on the channel conduction mechanism and theoretical modeling have been conducted on top-down fabricated silicon nanowires. In this paper, an analytical model based on the conduction mechanism of junctionless silicon nanowires is verified using a three-dimensional device simulator. Also, by applying the extracted electrical parameters of silicon-nanowire-based devices, the proposed photodetection circuit is simulated for implementation in a photosensitive retinal prosthetic device.

2. Methods

2.1 Fabrication method

To derive the drain current conduction mechanism of the proposed silicon-nanowire device, the top-down fabrication process is described to explain the cross-sectional structure of the silicon nanowire.[10] The top-down fabrication processes of the (100)-silicon-nanowire array are shown in Fig. 2(a). The silicon nanowires are fabricated using a p-type, 4 inch, single-crystalline silicon wafer. For the fabrication process using (100)-oriented silicon, a 1000-Å-thick thermal oxide layer is grown on the silicon substrate by wet oxidation. After line and space patterns are defined by photolithography and dielectric etching, photoresists



(a) (b)

Fig. 2. (Color online) Fabrication. (a) Top-down process of (100) silicon nanowire. (b) Cross-sectional structure of (100) silicon nanowire.

are removed by O_2 plasma ashing. Then, rectangular silicon columns are fabricated by silicon deep-reactive-ion etching (DRIE). Subsequently, anisotropic silicon wet etching using tetra-methyl-ammoniumhydroxide (TMAH) solution is performed for 90 s. The exposed silicon surface is etched by exploiting the anisotropic wet etching properties of silicon in TMAH solution. After the fabrication of hourglass-shaped silicon structures, the silicon nanowire array is fabricated by thermal oxidation, which produces silicon dioxide from a chemical reaction between silicon and oxygen.

The fabrication results of the arrayed silicon nanowire are shown in Fig. 2(b). As shown in the figure, the height of the silicon nanowire (H_{nw}) is determined by the photolithographic pattern width, which is an inherent property of the (100)-single-crystalline-silicon wafer. The width of the silicon nanowire (W_{nw}) is precisely controlled by adjusting the processing time of the thermal oxidation process. The amount of drain current mostly depends on the accumulation current through the surface of the silicon nanowire, which can be increased by increasing the pattern width in the photolithographic process.[13] However, increasing the pattern width results in increased H_{nw}, which needs to be minimized to achieve a high current on/off ratio and low power consumption. Therefore, for enhanced device characteristics, increasing the number of silicon nanowires is necessary.

2.2 Current conduction model of silicon nanowires

To understand the operation mechanism of the silicon-nanowire FET, a quantitative current conduction model based on semiconductor theory is used.[14] As illustrated in Fig. 3(a), the cross section of (100)-silicon nanowires can be assumed to have a triangular shape. The source and drain are assumed to be P^+-doped, and the silicon nanowire is assumed to have a p-type channel. The gate material is N^+-doped polysilicon and is assumed to be uniform. As shown in Fig. 2(b), the drain current of the proposed p-type silicon nanowire consists of two components, hole accumulation current (I_{acc}) and bulk current (I_{bulk}). The total drain current in the device is given by the sum of the current in the accumulation channel and the current in the bulk of the device.

The proposed device is normally turned off; therefore, when zero bias is applied to the gate, the channel is fully depleted.[13] From the gradual channel approximation, the hole accumulation current (I_{acc}) in the channel can be expressed as

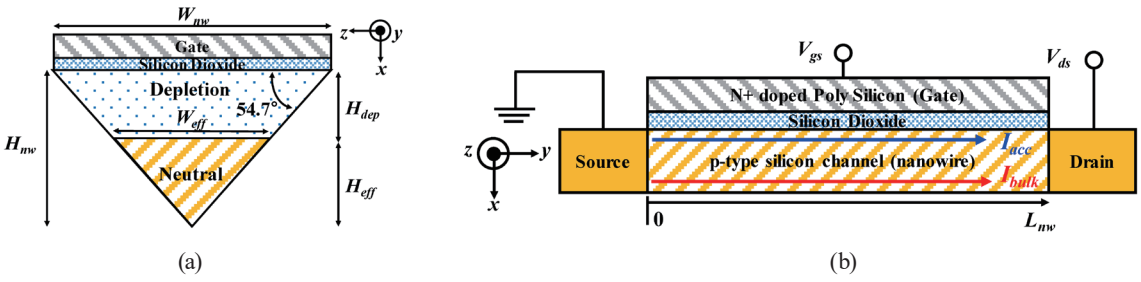


Fig. 3. (Color online) Schematic of silicon-nanowire device for quantitative analysis. (a) Cross-sectional view. (b) Lateral view.

$$I_{acc} = \mu_s \cdot \frac{W_{nw}}{L_{nw}} \cdot C_{ox} \cdot \int_0^{V_{ds}} \left(\left(V_{gs} - V_{fb} \right) - V_{cs} \right) \cdot dV_{cs} \ , \tag{1}$$

where μ_s is the hole surface mobility, L_{nw} is the length of the silicon nanowire, W_{nw} is the width of the silicon nanowire, C_{ox} is the gate oxide capacitance per unit area, V_{ds} is the bias voltage, V_{gs} is the gate-source voltage, V_{fb} is the flat-band voltage, and V_{cs} is the local potential along the silicon-nanowire channel. The bulk current (I_{bulk}) occurs when a nondepleted silicon region exists below the channel. When the voltage applied to the gate exceeds the flat-band voltage, the silicon-nanowire channel is fully depleted. Therefore, as illustrated in Fig. 3(a), the cross sections of arbitrary points along the silicon nanowire can be assumed to be a depletion region in the channel and a neutral region below the channel. The gate depletion height can be derived from solving the one-dimensional Poisson's equation. The bulk current in the neutral region (I_{bulk}) can be derived using the gradual channel approximation as

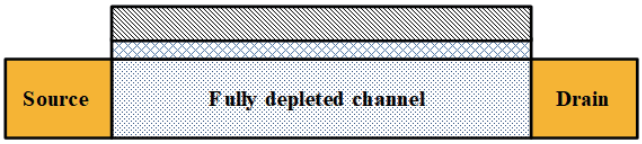
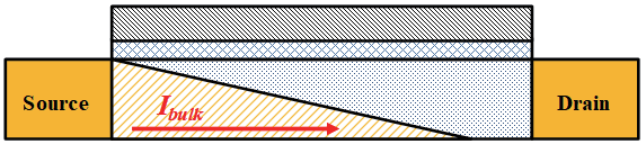
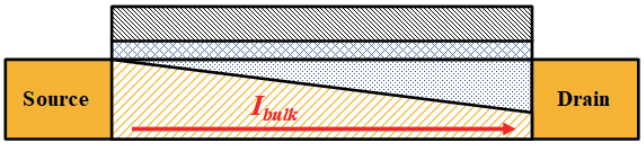
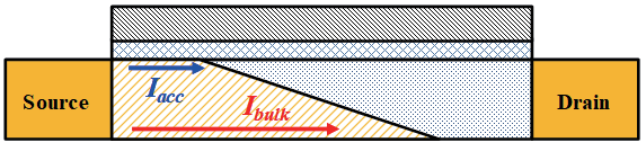
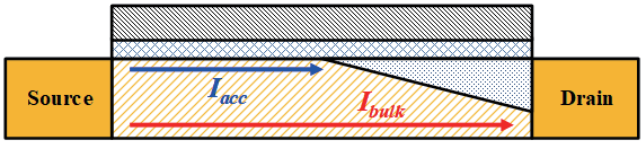
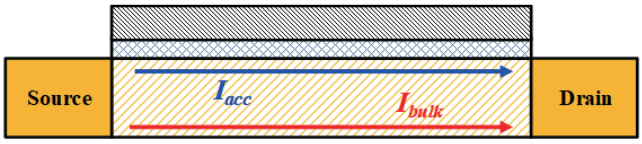
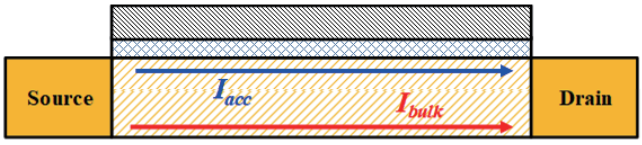
$$\begin{aligned}
&dR = \frac{1}{q \cdot N_A \cdot \mu_b} \cdot \frac{dy}{A_{eff}} = \frac{1}{q \cdot N_A \cdot \mu_b} \cdot \frac{dy}{\frac{1}{2} W_{eff} \cdot H_{eff}} = \frac{1}{q \cdot N_A \cdot \mu_b} \cdot \frac{\tan 54.7^\circ}{{H_{eff}}^2} dy, \\
&I_{bulk} \cdot dy = q \cdot N_A \cdot \mu_b \cdot \frac{1}{2} W_{eff} \cdot H_{eff} \cdot dV_{cs} = q \cdot N_A \cdot \mu_b \cdot \frac{{H_{eff}}^2}{\tan 54.7^\circ} \cdot dV_{cs}, \\
&I_{bulk} \cdot \int_0^{L_{nw}} dy = \frac{q \cdot N_A \cdot \mu_b}{\tan 54.7^\circ} \int {H_{eff}}^2 \cdot dV_{cs}, \\
&I_{bulk} = \frac{q \cdot N_A \cdot \mu_b}{L_{nw} \cdot \tan 54.7^\circ} \int \left(H_{nw} - H_{dep} \right)^2 \cdot dV_{cs} \ ,
\end{aligned} \tag{2}$$

where q is the elementary charge, N_A is the acceptor doping concentration, μ_b is the bulk mobility, A_{eff} is the area of the neutral region, W_{eff} is the width of the neutral region, H_{eff} is the height of the neutral region, H_{nw} is the height of the nanowire, and H_{dep} is the depletion height. From the fabrication process of (100)-silicon nanowires, the angle of the (111)-planes of the structure is 54.7°, which means that H_{nw} depends on W_{nw}. The summarized result of the quantitative drain current due to the integration range of V_{cs} is shown in Table 1. As shown in the table, the detailed drain current conduction mechanism can be distinguished in seven cases due to the applied gate voltage.

3. Results

To determine the electrical characteristics of the silicon-nanowire device, such as maximum on-current and current on/off ratio, the device simulation tool SENTAURUS (Synopsys, USA) is used. The drain current due to applied gate voltage is simulated for acceptor doping concentrations of 1×10^{16}, 1×10^{17}, and 1×10^{18} cm^{-3}, which have resistivities of approximately 1, 0.1, and 0.01 Ω·cm, respectively [Fig. 4(a)]. Also, simulation results of the drain currents

Table 1
(Color online) Summarized drain current conduction mechanism.

#	Condition	Drain conduction
1	$V_{gs} - V_{fb} > V_{dep}$	 Silicon nanowire structure is fully depleted.
2	$0 < V_{gs} - V_{fb} < V_{dep}$ $V_{gs} - V_{fb} - V_{ds} > V_{dep}$	 Neutral region is pinched off. No accumulation channel
3	$0 < V_{gs} - V_{fb} < V_{dep}$ $0 < V_{gs} - V_{fb} - V_{ds} < V_{dep}$	 Neutral region is not pinched off. No accumulation channel
4	$V_{gs} - V_{fb} < 0$ $V_{gs} - V_{fb} - V_{ds} > V_{dep}$	 Neutral region is pinched off. Accumulation channel at source end
5	$V_{gs} - V_{fb} < 0$ $0 < V_{gs} - V_{fb} - V_{ds} < V_{dep}$	 Neutral region is not pinched off. Accumulation channel at source end
6	$V_{gs} - V_{fb} < 0$ $V_{gs} - V_{fb} - V_{ds} < 0$	 Neutral region is not pinched off. Accumulation channel from source to drain (linear)
7	$V_{gs} - V_{fb} < 0$ $V_{gs} - V_{fb} - V_{ds} > 0$	 Neutral region is not pinched off. Accumulation channel from source to drain (saturation)

from the variations in the length of the silicon nanowire (5, 10, 15, and 20 mm), the width of the silicon nanowire (50, 100, 150, 200, and 250 nm), and gate oxide thickness (10, 20, 50, 100, 200, and 300 Å) are shown in Figs. 4(b)–4(d), respectively. The applied bias voltage (V_{ds}) is –3 V, and the gate voltage (V_{gs}) is applied from –3 to 0 V. During the drain current simulation, each parameter is fixed except the input parameter (N_A fixed to 1×10^{17} cm^{-3}, L_{nw} fixed to 20 mm,

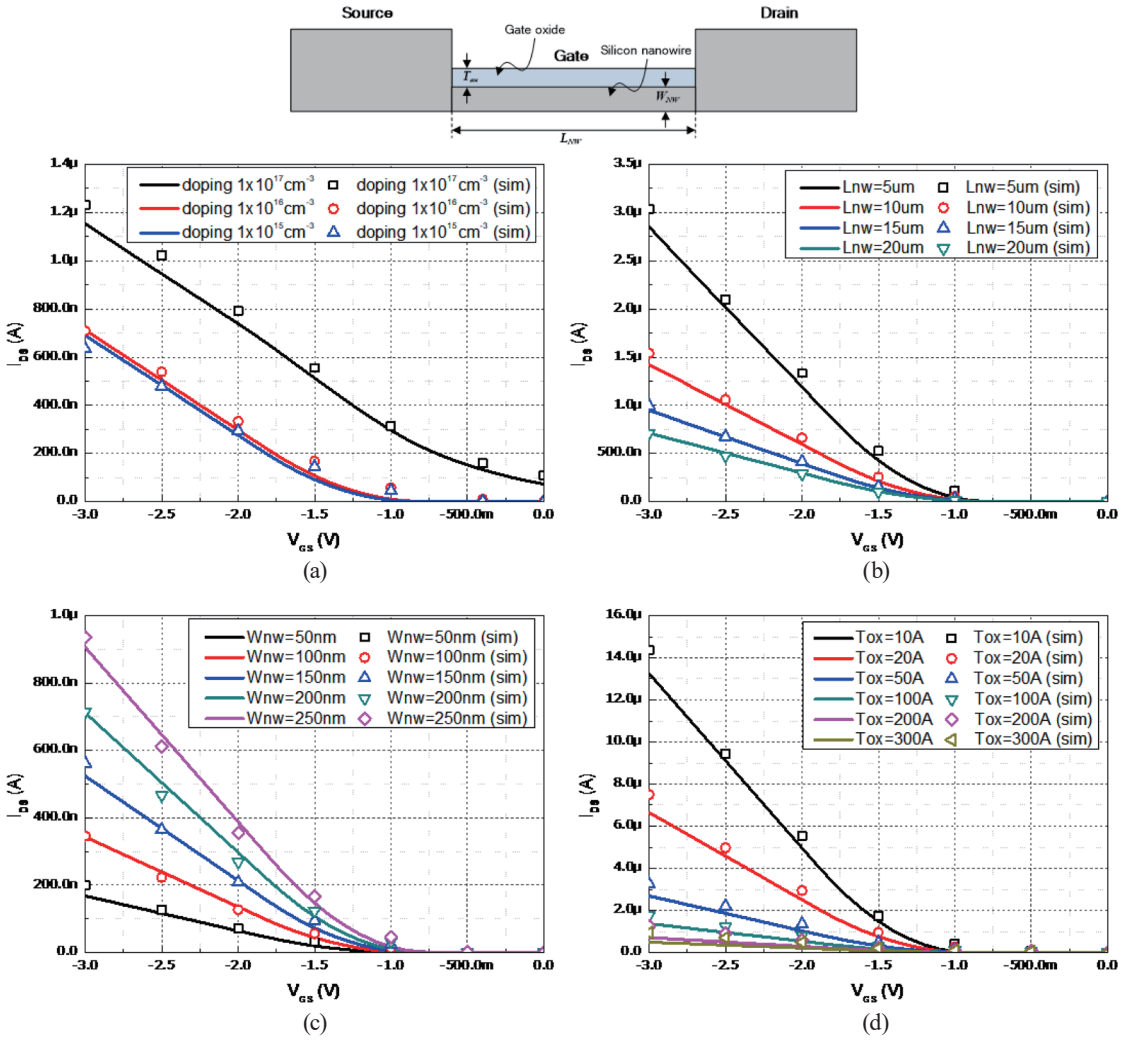


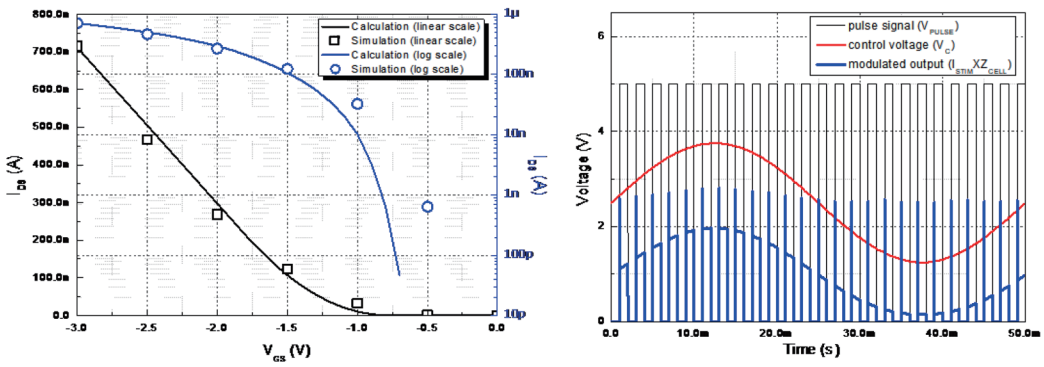
Fig. 4. (Color online) Simulation results compared with the quantitative calculation results. (a) Doping concentration. (b) Length of silicon nanowire. (c) Width of silicon nanowire. (d) Gate oxide thickness.

W_{nw} fixed to 200 nm, and T_{ox} fixed to 200 Å). In Table 2, the parameters for the drain current conduction model analysis of silicon nanowires for simulation and calculation are summarized. The compared results of device simulation using SENTAURUS and the quantitative analysis calculation are similar, indicating that the drain conduction mechanism of the silicon nanowire can be used for the parameterization of the silicon-nanowire devices.

From the results, the values of L_{nw}, W_{nw}, T_{ox}, and N_A are determined to be 20 μm, 200 nm, 200 Å, and 1×10^{17} cm^{-3}, respectively. The dimensions are derived by mainly considering the off-current level, which should be minimized, because of the unnecessary power dissipation. The simulation result for the above conditions is plotted in Fig. 5(a), where the maximum on-current and current on/off ratio for a single silicon nanowire are approximately 700 nA and

Table 2
Summarized parameters for drain current conduction model analysis of silicon nanowire.

Parameter	Value	Unit
Silicon band gap (E_g)	1.12	eV
Intrinsic carrier concentration (n_i)	1.50×10^{10}	cm^{-3}
Boltzmann's constant (k)	1.38×10^{10}	$J \cdot K^{-1}$
Absolute temperature (T)	300	K
Elementary charge (q)	1.60×10^{10}	C
Absolute permittivity (ε_0)	8.85×10^{10}	F/m
Relative permittivity of silicon dioxide (ε_{ox})	3.9	
Relative permittivity of silicon (ε_{si})	11.7	
Nanowire width (W_{nw})	300×10^{-9}	m
Nanowire height (H_{nw})	$H_{nw} = (W_{nw}/2) \times \tan 54.7°$	m
Nanowire length (L_{nw})	20×10^{-6}	m
Hole surface mobility (μ_s)	240	$cm^2/(V \cdot s)$
Hole bulk mobility (μ_b)	458	$cm^2/(V \cdot s)$



(a) (b)

Fig. 5. (Color online) (a) Results of silicon-nanowire device for gain-controllable scheme. (b) Verification of gain-controllable protocol using the silicon-nanowire-based retinal prosthetic system.

1×10^3, respectively. From the simulation result, increasing the number of silicon nanowires for device fabrication is necessary to drive sufficient current to stimulate retinal cells. Therefore, a fabrication process using a top-down method to achieve a highly densified silicon-nanowire array has many advantages compared with a bottom-up approach. Using the parameters of the silicon-nanowire FET, a circuit analysis tool [OrCAD PSpice Designer Lite (Cadence Design Systems, Inc., USA)] is used to verify the gain-controllable scheme. As shown in Fig. 5(b), the control voltage (V_C) is generated by the resistance variation of the silicon-nanowire PD due to external light intensity. Also, the current stimulus (I_{STIM}) is modulated with a pulse signal (V_{PULSE}) for amplification.

4. Conclusion

In this paper, a simplified and gain-controllable retinal prosthetic device with photosensitive silicon-nanowire PDs integrated with silicon-nanowire FETs is presented. An analytical model based on a conduction mechanism of junctionless silicon nanowires is verified using a three-dimensional device simulator. Also, by applying the extracted electrical parameters of the silicon-nanowire-based devices, the proposed photodetection circuit is simulated for implementation in a photosensitive retinal prosthetic device. The results are promising, with the current stimulus sufficiently amplified and controlled to evoke neural impulses. The results in this paper can be applied to a novel silicon-nanowire-based neural stimulation device and to guide the design of a high-resolution retinal prosthetic system.

Acknowledgments

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