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4.36 fJ/Conversion-step Ultralow-power 16-bit Successive Approximation Register Capacitance-to-digital Converter in 0.18 μm CMOS Process

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In this paper, we present an ultralow-power 16-bit successive approximation register (SAR) capacitance-to-digital converter (CDC) for capacitive sensors. To obtain ultralow power consumption, the CDC is designed using 0.7 V input voltage. Furthermore, the CDC employs a SAR algorithm to obtain low power consumption and a simplified structure. The proposed circuit uses a capacitive sensing amplifier (CSA) and a dynamic latch comparator to achieve parasitic capacitance-insensitive operation and energy efficiency. The CSA adopts a correlated double sampling (CDS) technique to reduce flicker (1/*f*) noise to achieve low-noise characteristics. The SAR algorithm is implemented in the dual operating mode, using an 8-bit coarse programmable capacitor array in the capacitance domain and an 8-bit R-2R digital-to-analog converter (DAC) in the charge domain. The R-2R DAC determines the lower 8-bit, and the remaining upper 8-bit is determined by the CDAC. To obtain ultralow power consumption, the minimum resistor of the R-2R DAC is 1.5 MΩ. The proposed CDC achieves a wide input capacitance range of 12.6 pF and a high resolution of 0.191 fF in simulation. The CDC is fabricated in the 0.18 μm 1P6M CMOS process with an active area of 0.63 mm^2. The total power consumption of the CDC is 0.254 μW with a 0.7 V supply in simulation. The SAR CDC achieves a simulated 16-bit resolution within a conversion time of 1.125 ms and an energy-efficiency figure-of-merit (FoM) of 4.36 fJ/conversion step.

1. Introduction

Micro-electromechanical systems (MEMS) sensors are receiving particular attention owing to their small size, high signal-to-noise ratio (SNR), and low cost. Among them, the capacitive sensor is widely used in accelerometers, liquid-level gauges, and pressure and humidity sensors owing to its low power, high accuracy, low-temperature dependence, and good compatibility with CMOS.[1–6] Furthermore, these sensors are used in products such as initial measurement

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units, smartphones, wearable devices, and smart houses.[1,2] To use a capacitive sensor, a capacitance readout IC is required. Conventionally, the capacitance readout IC converts the capacitance to voltage and subsequently to a digital code using an analog-to-digital converter (ADC). However, the addition of an ADC results in complex circuits, larger sizes, and higher power consumption.

Recently, to address these disadvantages, the capacitance readout IC has preferably been in the form of a capacitance-to-digital converter (CDC). Unlike conventional capacitance readout ICs, CDC can convert the capacitance directly into a digital code, eliminating the need for additional ADCs, which can be beneficial in terms of complexity, size, and power consumption.[22] Because a CDC is used in products operated using batteries, low power and high-resolution characteristics are important. For high resolution, the delta sigma (ΔΣ) CDC was proposed.[7,8] The ΔΣ CDC achieves high resolution through oversampling and noise shaping. However, power consumption is increased by oversampling and using the digital decimation filter, and the capacitance range is reduced to avoid a modulator overload. To achieve a wide capacitance range, a semidigital CDC that converts time to a digital code after first converting the capacitance to time was proposed.[9–11] The semidigital CDC expanded the capacitance range by converting the input capacitance to time. However, a fast digital counter and a high-frequency reference clock are required, thereby resulting in larger jitter noise and power consumption. To achieve good energy efficiency, a successive approximation register (SAR) CDC was proposed.[12] The schematic of the conventional SAR CDC is shown in Fig. 1. Because the sensor capacitance (C_s) is connected to the high-impedance node V_x, the sampled charge is redistributed to all capacitances connected to node V_x including that of the parasitic capacitor (C_p), which can be very large, especially for off-chip capacitive sensors. This offset voltage causes a conversion error that eventually leads to a reduction in resolution. To address the offset error limitation, a method using a charge amplifier before a comparator was proposed.[13] However, the architecture has reduced the energy efficiency owing to the use of the power-consuming operational transconductance amplifier (OTA).

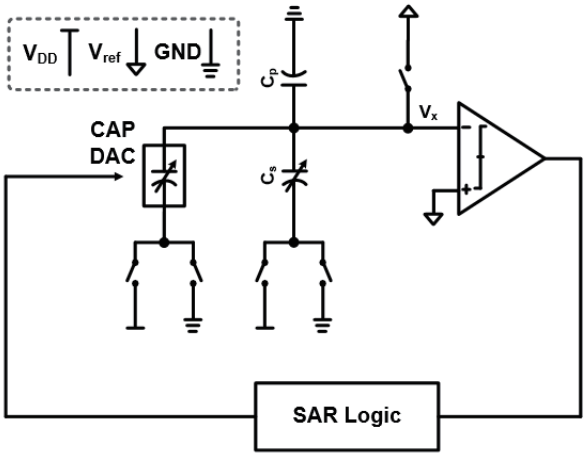

Fig. 1. Schematic of the conventional SAR CDC.

We herein present the ultralow-power SAR CDC for capacitive sensors. The proposed CDC increases the energy efficiency by applying the SAR algorithm and creates a more energy-efficient comparator by organizing the sensors in the capacitive sensing amplifier (CSA) and dynamic latch structures, thereby rendering them insensitive to offsets caused by the parasitic capacitor. In addition, the CSA implemented the ultralow power using the inverter-based amplifier. Furthermore, the CSA uses a designed correlated double sampling (CDS) technique to reduce the offset and flicker noise (1/*f*). The conventional SAR algorithm uses only the capacitor digital-to-analog converter (CDAC) using the cap array, and the resolution is limited owing to the parasitic cap that was generated by the cap array. To address this limitation, the proposed SAR algorithm is implemented in the dual operating mode, using an 8-bit coarse programmable capacitor array in the capacitance domain and an 8-bit R-2R DAC in the charge domain. The CDC is optimized and implemented in 0.18 μm CMOS technology and achieves an energy-efficiency figure-of-merit (FoM) of 4.36-fJ/conversion step.

2. Circuit Operation of Proposed SAR CDC

2.1 Architecture of the proposed SAR CDC

A schematic of the proposed 16-bit SAR CDC circuit and the timing diagram are shown in Fig. 2. It comprises a CSA, dynamic latch, SAR control logic, 8-bit coarse programmable capacitor array (CDAC), and 8-bit R-2R DAC.

To achieve energy efficiency, the CSA is a conventional inverter-based amplifier. The inverter-based amplifier can be implemented in the self-biased form. Furthermore, the sourcing current can be reused as the sinking current. This results in excellent noise efficiency factor (NEF) characteristics and good energy efficiency.

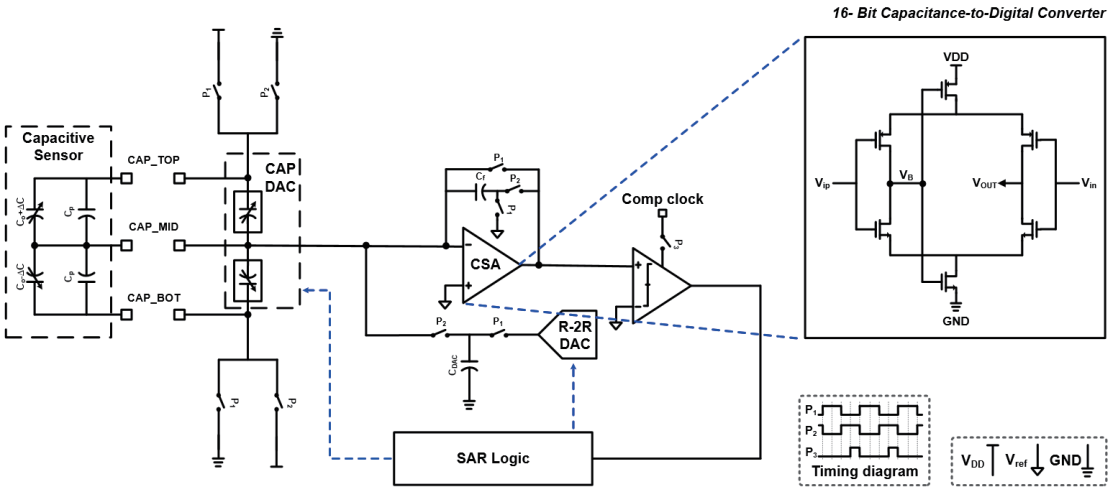

Fig. 2. (Color online) Schematic of the proposed ultralow power SAR CDC.

2.2 Operation of the proposed SAR CDC

The circuit operation is performed in two phases. The SAR CDC requires non-overlapping clocks, P_1 and P_2, as well as a SAR clock. The operation of the input stage of the proposed SAR CDC is shown in Fig. 3.

P_1 is the sampling phase in which the sensor capacitor and the DAC are charged. Subsequently, the CSA operates as a unit gain buffer. The stored charge is given by

$$P_1 : (C_0 + \Delta C)(V_{ref} - V_{DD}) + (C_0 - \Delta C) \cdot V_{ref} \,. \tag{1}$$

Furthermore, owing to the CDS technique, the feedback capacitor (C_f) is charged with low-frequency noise. P_2 is the amplifying phase in which the charge on the sensor capacitor and DAC is redistributed to the C_f. The charge is given by

$$P_2 : (C_0 + \Delta C) \cdot V_{ref} + (C_0 - \Delta C)(V_{ref} - V_{DD}) + C_f \cdot (V_{ref} - V_{OUT}) + C_{DAC} \cdot V_{DAC} \,. \tag{2}$$

Furthermore, the low-frequency noise stored in the C_f is subtracted. Because charge is conserved, from Eqs. (1) and (2), the output voltage (V_{OUT}) of the CSA is

$$V_{OUT} = \frac{2 \cdot \Delta C \cdot V_{DD} + C_{DAC} \cdot V_{DAC}}{C_f} + V_{ref} \,. \tag{3}$$

Thus, the differential voltage at the comparator input terminals (ΔV) is given by

$$\Delta V = V_{OUT} - V_{ref} = \frac{2 \cdot \Delta C \cdot V_{DD} + C_{DAC} \cdot V_{DAC}}{C_f} \,. \tag{4}$$

The comparator input terminals (ΔV) are subsequently converted to a digital code through the comparator. The comparator used in the proposed CDC is shown in Fig. 4. The comparator

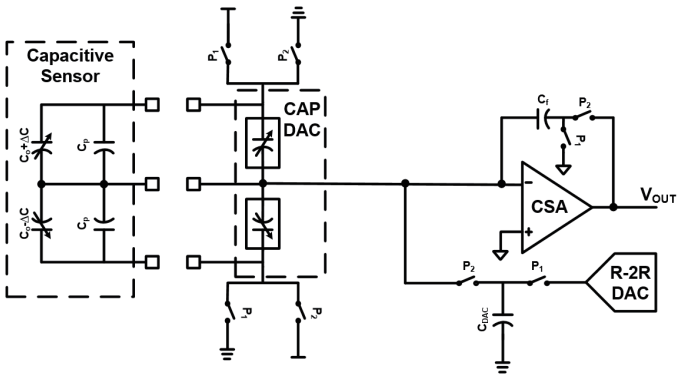

Fig. 3. Operation of the input stage.

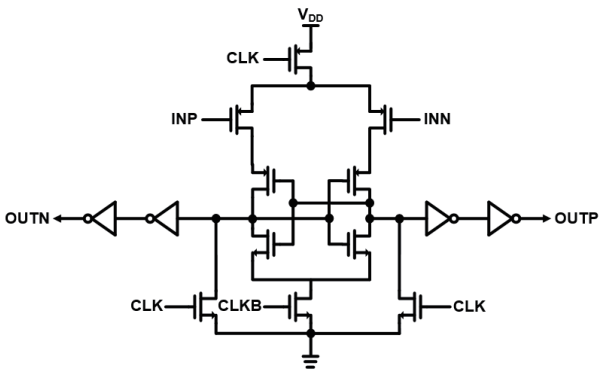

Fig. 4. Schematic of the dynamic latch comparator.

uses a dynamic latch structure to obtain good energy efficiency. The comparator output enters the SAR algorithm of the 16-bit SAR logic, with the top 8-bit controlling the CDAC and the bottom 8-bit controlling the R-2R DAC.

The CDAC operates in the capacitance domain with the upper 8-bit, and the R-2R DAC operates in the charge domain with the lower 8-bit. In the charge-domain operation, charge is stored to C_{DAC} in proportion to the output voltage of the R-2R DAC in the P_1 phase. Furthermore, the stored charge is redistributed to the CSA input in the P_2 phase. In the proposed CDC, the C_{DAC} is 49 fF, the input capacitance range is 12.6 pF, and the high resolution is 0.191 fF.

3. Design and Simulation Results of Proposed IC

3.1 Design of the proposed SAR CDC

The layout of the proposed ultralow-power SAR CDC is shown in Fig. 5. The entire layout consisted of the CSA, comparator, timing generator, CAP DAC, R-2R DAC, and SAR logic. The proposed SAR CDC is designed for the 0.18 µm 1P6M CMOS process with an active area of 0.63 mm^2.

3.2 Simulation results of the proposed SAR CDC

The simulation results of the proposed SAR CDC are shown in Fig. 6. Figures 6(a) and 6(c) show the change in input capacitance over time. The change in input capacitance was from 0 to 12.6 pF in the sine and ramp waveforms. Figures 6(b) and 6(d) show the digital output code of the proposed SAR CDC.

The energy efficiency of the proposed SAR CDC is evaluated using the energy-efficiency FoM. The FoM is given by

$$FoM = \frac{P_{avg} \times T_{conv}}{2^R}, \tag{5}$$

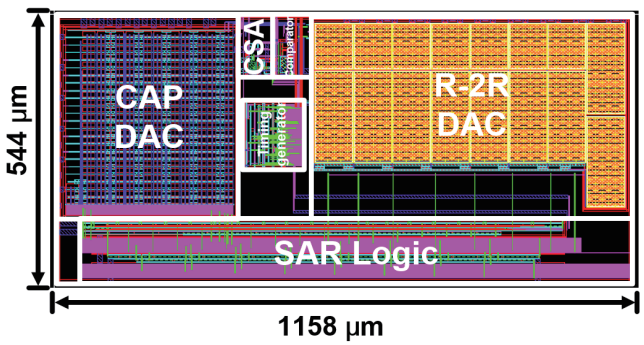

Fig. 5. (Color online) Layout of the proposed SAR CDC.

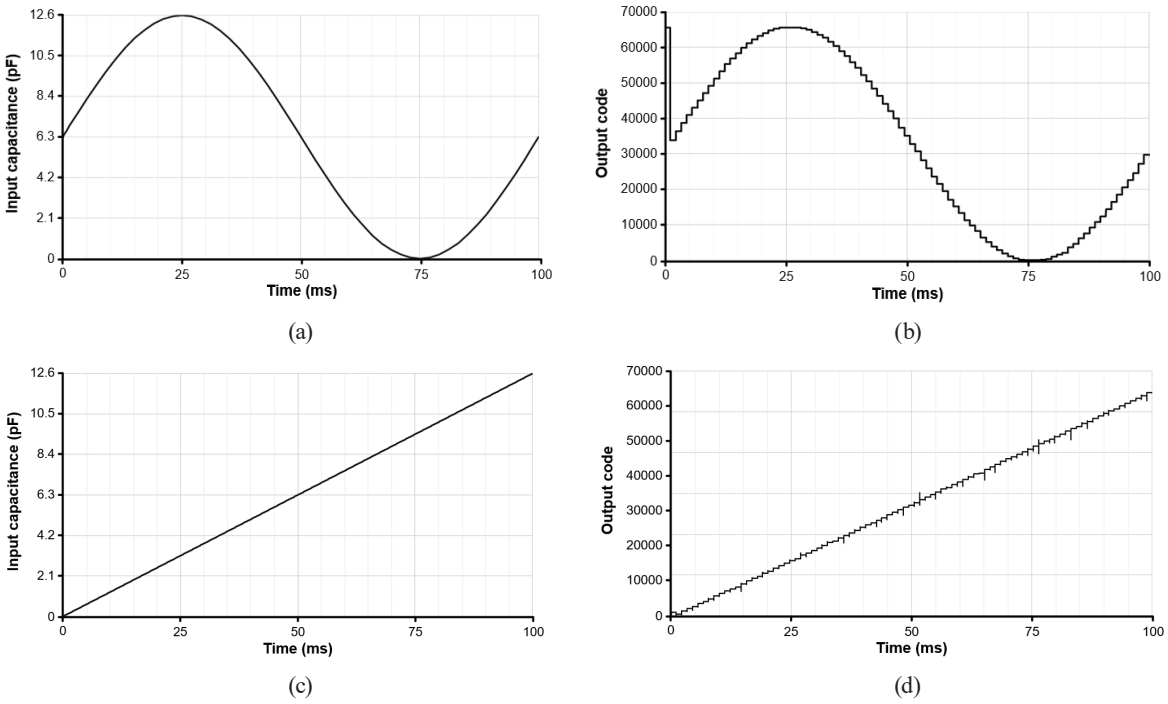

Fig. 6. Simulation result of the proposed SAR CDC: (a) input sine signal, (b) digital output code, (c) input ramp signal, and (d) digital output code.

where P_{avg} is the average power, T_{conv} is the conversion time, and R is the effective resolution in bit. Furthermore, the effective resolution is given by

$$R = \frac{SNR - 1.76}{6.02}, \tag{6}$$

where the SNR is given by

$$SNR = 20 \cdot \log\left(\frac{Capacitance\,Range / 2\sqrt{2}}{Absolute\,Resolution}\right). \tag{7}$$

The absolute resolution was obtained as the rms value of the output code after setting the input capacitance. When the transient noise was 10 mHz f min, 100 kHz f max, and 1 f seed, the digital output code is as shown in Fig. 7. The simulation results showed that the output noise was less than 1 least significant bit (LSB). Thus, the effective resolution was expressed in 16 bits.

The proposed SAR CDC has a power of 0.254 μW, a conversion time of 1.125 ms, and an effective resolution of 16 bits, resulting in a 4.36-fJ/conversion step in simulation. A performance summary of the simulated parameters and comparisons with state-of-the-art CDCs are shown in Table 1. In addition, Fig. 8 shows a comparison of the FoM and capacitance range,

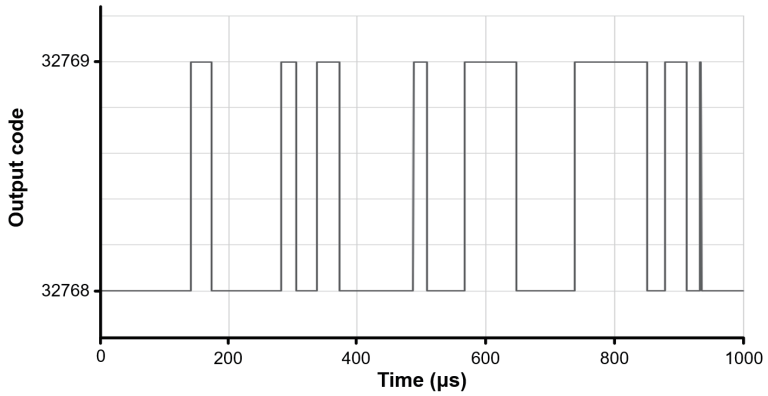

Fig. 7. Simulation result when setting the input capacitance.

Table 1
Performance comparison: summary of measured parameters.

Parameter	Ref. 7	Ref. 9	Ref. 14	Ref. 15	Ref. 16	Ref. 17	Ref. 18	Ref. 19	This work (sim.)
Architecture	ΔΣ	C2T	2nd-ΔΣ	SAR	SAR	ΔΣ+ ZCBC	SAR+ ΔΣ	SAR	SAR
Output format	Bit stream	PM	Bit stream	Digital code	Digital code	Bit stream	Digital code	Digital code	Digital code
Technology (μm)	0.16	0.35	0.18	0.35	0.18	0.18	0.18	0.18	0.18
Supply (V)	1.2	3.3	2.6	3.3	0.9/1	N/R	1.4	1.8	0.7
Power (μW)	10.3	211	2340	303	3.84	15	33.7	86.4	0.254
Active area (mm^2)	0.28	0.51	0.67	0.07	0.1	N/R	0.46	0.55	0.63
Conversion time (ms)	0.8	7.6	3.07	0.65	0.0425	0.128	0.23	1.125	1.125
Capacitance range (pF)	0.54 –1.06	6.8	10	16	16.14	1 –10000	24	29.4	12.6
ENOB (bit)	11.1	15	17.4	12.5	11.8	13	15.4	11.49	16
FoM (pJ/step)	3.754	49	37	34	0.045	0.23	0.179	31.6	0.00436

C2T = capacitance-to-time, PM = period modulation, ZCBC = zero-crossing-based circuits

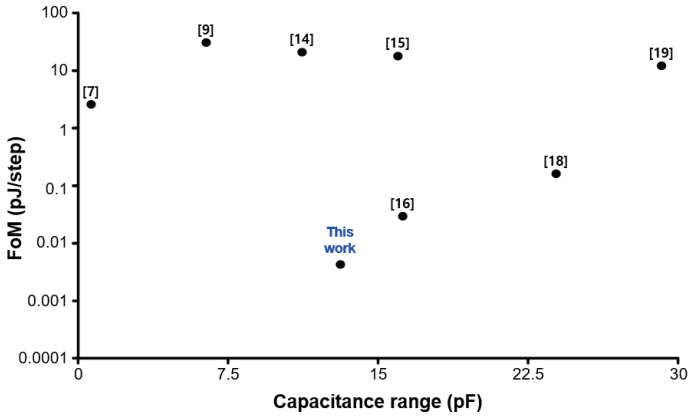

Fig. 8 (Color online) Comparison of capacitance ranges and FoMs.

which represents the energy efficiency. In Table 1, the power consumption of the proposed SAR CDC is 0.254 μW, which is much lower than that of the SAR structures. As shown in Fig. 8, the proposed SAR CDC achieves a FoM of 4.36 fJ/conversion step, which is much lower than those in previous works, resulting in excellent energy efficiency in the reasonable capacitance range.

4. Conclusion

We herein presented the ultralow-power 16-bit SAR CDC for the capacitive sensor. The proposed SAR CDC used the inverter-based CSA, dynamic latch comparator, and SAR algorithm for energy efficiency. The CSA also used CDS techniques to reduce the offset and the flicker noise (1/*f*). Additionally, the SAR algorithm was implemented in the dual operating mode, using an 8-bit coarse programmable capacitor array in the capacitance domain, and an 8-bit R-2R DAC in the charge domain to reduce the offset caused by the parasitic cap on the CDAC. The proposed CDC was designed for the 0.18 μm 1P6M CMOS process with an active area of 0.63 mm^2. The total power consumption of the proposed CDC was 0.254 μW with a 0.7 V supply in simulation. Furthermore, the proposed CDC achieved an energy-efficiency FoM of 4.36-fJ/conversion step in simulation.

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