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Low-noise 16-bit First-order Delta-sigma Capacitance-to-digital Converter for Capacitive Humidity Sensor

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In this paper, a low-noise 16-bit capacitance-to-digital convertor (CDC) for a capacitive humidity sensor is proposed. The proposed sensor interface circuit is implemented as a first-order incremental delta-sigma structure and directly converts the capacitance change of the humidity sensor to a 16-bit digital code. A switched capacitor (SC) integrator of the delta-sigma modulator is adopted in the chopper stabilization technique for a low-noise characteristic. The chopper stabilization technique can avoid the offset and low-frequency flicker noise of an amplifier. The offset cancellation programmable capacitor array of the input stage is used for eliminating the mismatched capacitance from the parasitic capacitor and process variations. The proposed delta-sigma CDC has an accumulator with a simple 16-bit dual counter that converts the delta-sigma modulator output to a 16-bit digital code for reducing the power consumption of the back-end digital processing. The proposed sensor interface circuit is fabricated using the standard 0.18 μm complementary metal-oxide-semiconductor process with an active area of 0.66 mm^2. The effective resolution of the worst case is 14.4 bits, and the active power consumption of the proposed delta-sigma CDC is 376 μW with a 1.8 V supply.

1. Introduction

Humidity is an important parameter in environmental control systems in many fields such as printers, automobiles, medical devices, and semiconductor manufacturing. Humidity sensors can be made small and highly reliable through micro-electromechanical system (MEMS) technology. Humidity sensors are capacitive and resistive depending on the humidity sensing method used.[(1)] A resistive humidity sensor can yield a high resolution. However, a resistive humidity sensor requires correction in accordance with the temperature change, and a low relative humidity is difficult to detect. A capacitive humidity sensor does not require temperature compensation, has relatively linear characteristics according to the relative

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humidity change from all the relative humidity ranges, and provides a fast response owing to its thin-film structure. With these advantages, capacitive humidity sensors are typically used for relative humidity sensing.[1,2] To use the capacitive humidity sensors in precise environmental control applications, a high-performance sensor interface circuit is required to sense small capacitance variations in the humidity sensor.

Conventional sensor interface circuits convert the capacitance to a voltage signal through a capacitive sensing amplifier (CSA) and subsequently convert the voltage signal from an analog-to-digital converter (ADC) to a digital signal. In previous studies, some direct convertible circuit schemes without voltage signal conditioning were proposed. The direct convertible circuit schemes, which are, among others, successive approximation register (SAR) capacitance-to-digital convertors (CDCs), capacitance-to-frequency convertors, and delta-sigma CDCs, can reduce the power and area required for the CSA.[3–11] The SAR CDC consisting of a digital-to-analog convertor (DAC), a comparator, and some digital blocks can yield a low power, a fast conversion, and a small area. However, its resolution is limited owing to the capacitance mismatch and the noise from the comparator.[3] The capacitance-to-frequency (or period) convertor has a simple structure, is suitable for a small area, and consumes a low power. However, the frequency (or period) output is an incomplete digital signal. The frequency (or period) requires an additional conversion to a digital code for back-end digital systems. The additional conversion implies further power consumption.

The delta-sigma CDC is used to obtain a low noise and a high resolution through its noise-shaping characteristic. The higher the order of the modulator, the better the low-noise characteristics; however, the higher the order of modulation, the more power is consumed.

In this paper, a capacitive humidity sensor interface circuit using an incremental delta-sigma CDC scheme is proposed. The proposed delta-sigma CDC adopts a first-order delta-sigma modulator for a low power consumption and a high resolution. The low-noise characteristics of the proposed delta-sigma CDC are obtained using other low-noise techniques instead of higher-order modulators. The dominant noise is primarily caused by a low-frequency flicker ($1/f$) noise and the parasitic input capacitance. The proposed first-order delta-sigma modulator reduces the low-frequency $1/f$ noise using a chopper stabilization technique. Furthermore, the parasitic input capacitance is reduced by the parasitic cancellation capacitance of the input stage. The proposed delta-sigma CDC is designed to adjust the input range to cover the various ranges of capacitive humidity sensors.[12,13] The 1-bit modulated signals of the delta-sigma modulator are finally output by a 16-bit code by the accumulator.

2. Operation of Proposed Capacitive Humidity Sensor Interface Circuit

The architecture of the proposed 16-bit delta-sigma CDC is shown below in Fig. 1. The proposed 16-bit delta-sigma CDC consists of a voltage reference, a relaxation oscillator, a timing generator, an offset cancellation input stage, a delta-sigma modulator, and an accumulator.

The reference voltage and timing clock for operating the delta-sigma CDC are generated by the internal blocks. The timing generator has a 4 MHz internal relaxation oscillator and uses the clock by dividing it. The mismatch and parasitic capacitances of the input humidity sensor

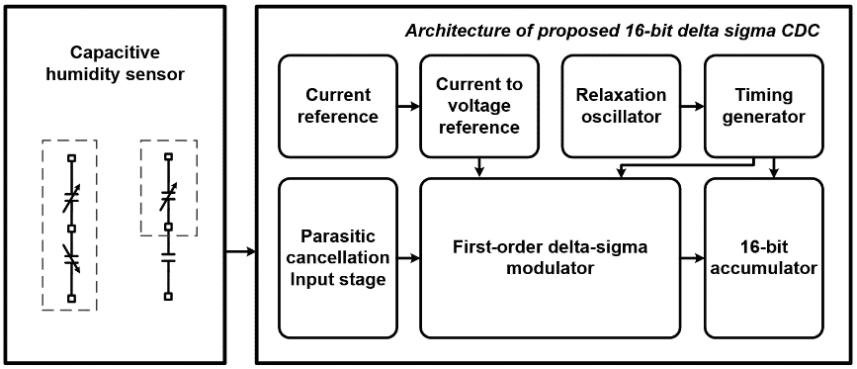


Fig. 1. Architecture of the proposed 16-bit delta-sigma CDC.

are cancelable with the parallel-connected programmable capacitors at the input stage of the proposed delta-sigma CDC. The first-order delta-sigma modulator outputs a 1-bit modulated signal. The accumulator counts the 1-bit modulated signal as a 16-bit code and outputs it.

The schematic of the proposed first-order delta sigma modulator for the capacitive humidity sensor is shown in Fig. 2. The first-order delta-sigma modulator consists of a switched capacitor (SC) integrator, a comparator, and programmable capacitors. The first-order delta-sigma modulator directly converts a capacitance change to digital signals using the SC integrator. The chopper stabilization technique was applied to the integrator of the delta-sigma modulator for low-noise characteristics. The chopper stabilization technique can modulate the 1/*f* noise of a low-frequency signal band to a high-frequency out band. The chopping clocks of the integrator used the nonoverlapped phases P3 and P4.

The first-order delta sigma modulator is operated in two nonoverlapped phases (P1 and P2). The capacitive humidity sensor drives the internal or external voltage. The input range is determined by the reference capacitor and driving voltage. In P1, the charges are stored in the sensor and reference capacitors. During P2, the amplifier integrates the charges through a feedback capacitor. The comparator output signal adjusts the driving voltage of *CREF* to generate the integrator output *VREF* in each phase. When the output of the comparator is high, *CREF* carries a negative charge to the integrator, while it transfers a positive charge when the output is low. Subsequently, the amount of integrated charge, delivered by the sensor and reference capacitor, becomes increasingly closer to zero. The input range was calculated using the charge equation and the saturation operation of the integrator when switching between P1 and P2. The charge equation when switching from P1 to P2 is shown as

$$\Delta V = \frac{(VTOP1 - VTOP2)\cdot(C_0 + \Delta C)}{CF} + \frac{(VBOT1 - VBOT2)\cdot(C_0 - \Delta C) + 2\cdot COMP\cdot VREF\cdot CREF}{CF}. \quad (1)$$

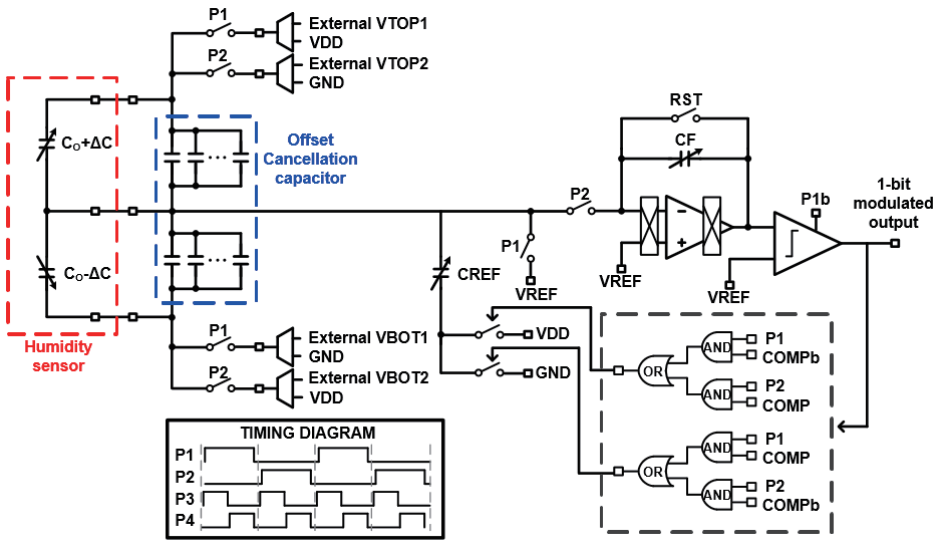


Fig. 2. (Color online) Schematic of the proposed first-order delta-sigma modulator.

The sensor input capacitance when the integrator output saturates indicates the input range. If the comparator output continues to be high, the output of the integrator saturates. The level of the modulated signal is always high even if the charge delivered by *CREF* is negative. Thus, the maximum capacitance is obtained as

$$\Delta C < \frac{\{(VTOP1 - VTOP2) + (VBOT1 - VBOT2)\} \cdot C_0 + 2 \cdot VREF \cdot CREF}{(VTOP1 - VTOP2) - (VBOT1 - VBOT2)}. \tag{2}$$

If the comparator output continues to be low, the output of the integrator saturates. The level of the modulated signal is always low even if the charge delivered by *CREF* is positive. Thus, the minimum capacitance is obtained as

$$\Delta C > \frac{\{(VTOP1 - VTOP2) + (VBOT1 - VBOT2)\} \cdot C_0 - 2 \cdot VREF \cdot CREF}{(VTOP1 - VTOP2) - (VBOT1 - VBOT2)}. \tag{3}$$

When driving voltages are used as internal voltages, the input range is expressed as

$$-\frac{CREF}{2} < \Delta C < \frac{CREF}{2}. \tag{4}$$

CREF is designed to be a programmable 7-bit capacitor. The programmable *CREF* can be applied to humidity sensors of various input ranges. The input range can be increased using external voltages. The internal relaxation oscillator outputs 4 MHz at the main clock. The timing generator divides the main clock to generate the clocks used at the circuit The divided

clocks are designed with nonoverlapping edges and output to the circuit. Figure 3 shows an accumulator for obtaining a 16-bit digital code. The accumulator of the proposed 16-bit delta-sigma CDC has a simple structure consisting of dual 16-bit up-counters and some digital logics. The dual 16-bit up-counter of the proposed accumulator counts the comparator output and clock P1. One of the 16-bit up-counters counts the clock P1 and outputs the end-of-conversion (EOC) signal and a reset signal (RST) at every 16 bits. Another 16-bit up-counter counts the comparator output until the EOC signal increases. When the EOC signal increases, the accumulator outputs a 16-bit digital code. The RST is used in the dual up-counter and integrator of the delta-sigma modulator. The output digital code resolution can be determined to be 12 or 16 bits by selecting the period of the RST. When a fast response and a low resolution are required, the 12-bit resolution should be used.

3. Measurement Results of Proposed IC

A fabricated die photograph of the proposed 16-bit delta-sigma CDC is shown in Fig. 4(a). The 16-bit delta-sigma CDC was designed using the standard 0.18 μm complementary metal-oxide-semiconductor (CMOS) process with an active area of 0.66 mm^2 excluding the I/O pads. The total power consumption for the 16-bit delta-sigma CDC is 376 μA with a 1.8 V supply. The digitally controlled 10-bit capacitor array, which is used in our experiment, is also integrated in the die.

Figure 5 shows the measurement environment and the equipment for measuring the proposed circuit. The fabricated chip was implemented on a printed circuit board for the measurement of the circuit. To evaluate the performance of the proposed circuit, the 10-bit digital controlled capacitor array in the chip was used. The humidity sensor used the CL-MC-02 sensor that is a polymer relative humidity capacitor. The digital output is acquired through an Arduino and a PC.

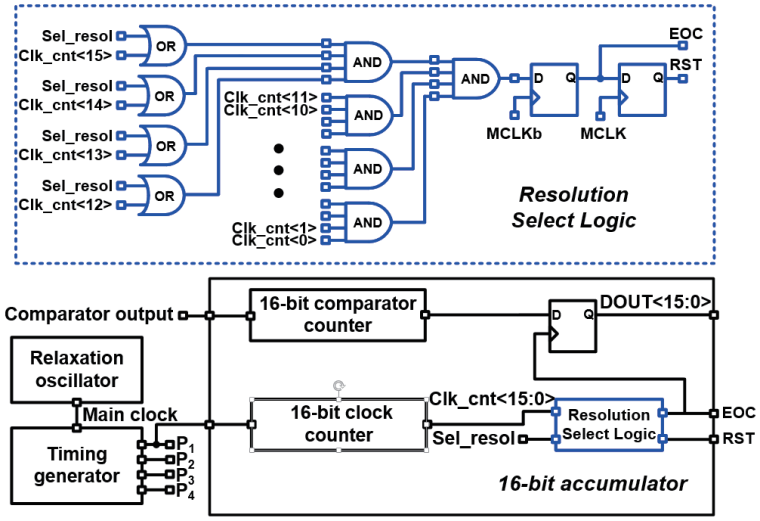
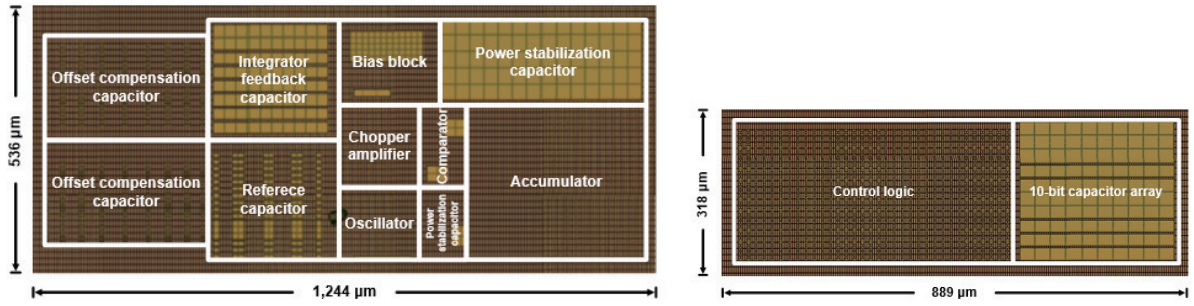


Fig. 3. (Color online) Accumulator for obtaining 16-bit digital code output.



(a) (b)

Fig. 4. (Color online) (a) Die photograph of the 16-bit delta-sigma CDC. (b) Die photograph of the digital controlled 10-bit capacitor array.

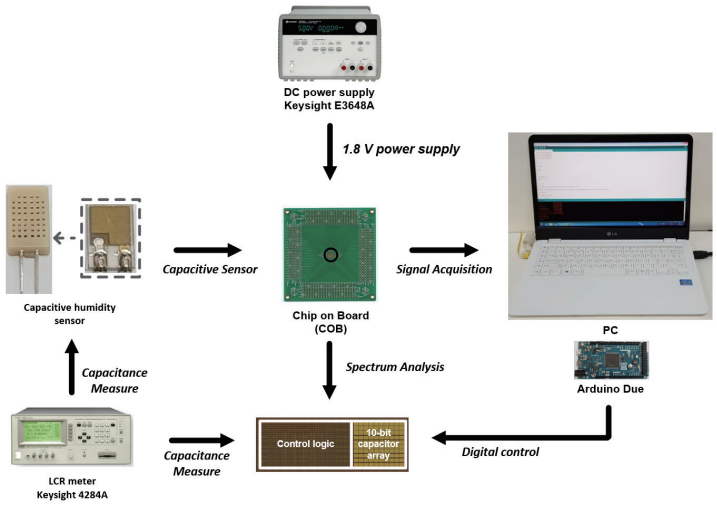


Fig. 5. (Color online) Measurement environment for the 16-bit delta-sigma CDC.

Figure 6 shows the measurement result for the input capacitance changes. To measure linearity, the input capacitor used is a chip capacitor, and the digitally controlled 10-bit capacitor array is used to control the capacitance range from 8.5 to 24.5 pF. The external chip capacitor is used as an offset capacitor for the input range setting. In the input range of 10 pF, the nonlinearity is calculated to be equal to 1.83% FSO. Figure 7 shows the standard deviations for 500 samples of each fixed input capacitance. The spot points are the results of using the chopper stabilization technique and the square points turn off the chopper stabilization. The effective resolution is calculated as

$$Effective\ resolution = \log_2\left(\frac{Fullscale\ capacitance\ input\ range}{RMS\ noise}\right). \tag{5}$$

When the chopper stabilization technique is used, the effective resolution in the best case is 14.4 bits in the 10 pF input capacitance range. When the chopper stabilization technique is not

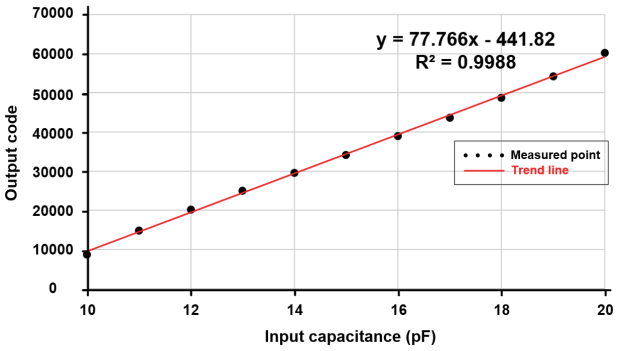


Fig. 6. (Color online) Linearity for the input capacitance changes.

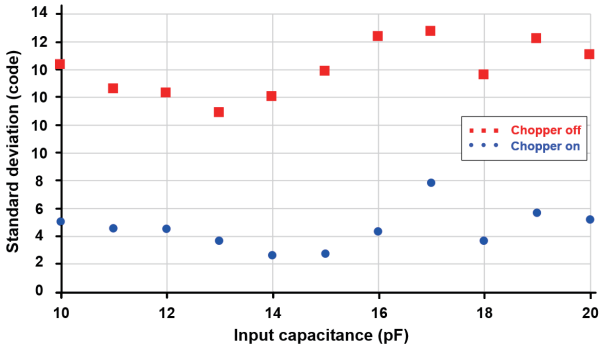


Fig. 7 (Color online) Standard deviation of each fixed input capacitance.

Table 1
Technical specifications of the humidity sensor.

Model	MC02
Power supply	10 V AC (max)
Operating range	Humidity 0–100% RH
Nominal capacitance	120 ± 10 pF (25 Celsius, 60% RH)
Average sensitivity	0.05 pF/% RH
Humidity effects	+1 Celsius, +0.025 pF
Return difference of humidity hysteresis	<1% RH
Linear error	<±2% RH
Operating frequency	5–100 kHz

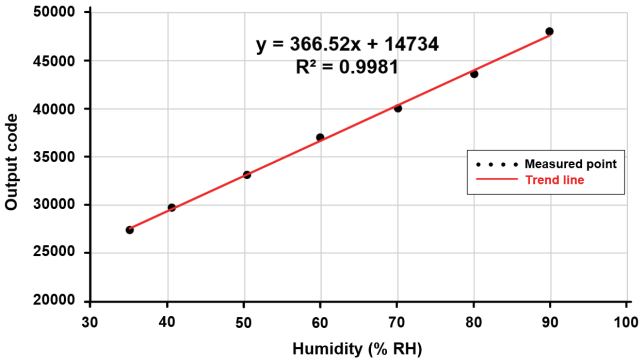
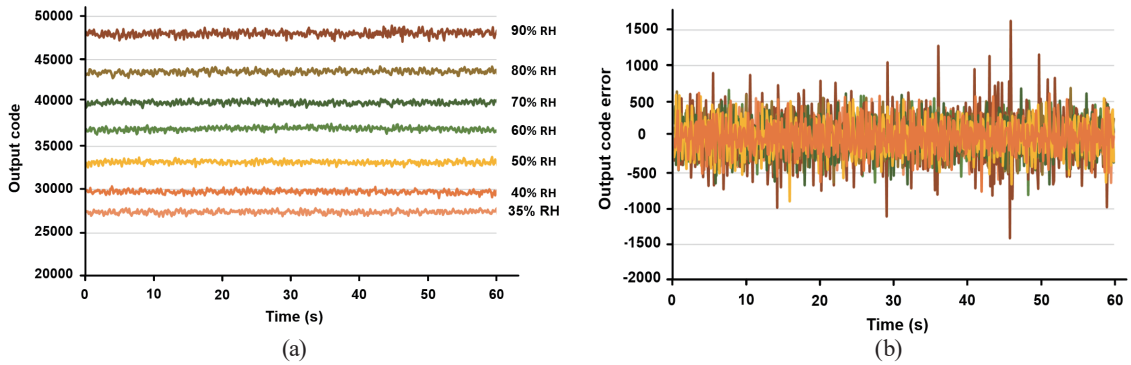


Fig. 8. (Color online) Measurement results for the relative humidity changes.

used, the effective resolution in the best case is 12.16 bits in the 10 pF input capacitance range. When using chopper stabilization techniques, the best resolution in the best case is 2.24 bits more than if it were not.

The proposed delta-sigma CDC with a humidity sensor was measured using a humidity chamber. The technical specification of the humidity sensor is shown in Table 1. Owing to the limited available humidity range of the humidity chamber, the relatively humidity was measured from 35 to 90% RH at 25 °C. The measured code outputs increasing with the relatively humidity are shown in Fig. 8.

When the humidity changes from 35 to 90% RH, the output code is changed to the 20627 code. The 20627 code change means a change of 3.8 pF in capacitance. The sensitivity of the 16-bit delta-sigma CDC with a humidity sensor was measured to be 58 fF/% RH. The conversion time of the delta-sigma CDC using the 16-bit accumulator is 120 ms. The number of code samples obtained is 500 at each RH point. Figure 9(a) shows the code variations for each RH change in 60 s. The standard deviation for each RH change is shown Fig. 9(b). In the results of the experiment with a humidity sensor, larger noise was measured than in the experiment with the programmable capacitor. Because the humidity chamber maintains the humidity with the circulation of wind, much noise was measured together.



(a) (b)

Fig. 9. (Color online) (a) Output code variations and (b) output code error for each relative humidity change.

Table 2
Performance comparison and summary of parameters.

	This work	Ref. 3	Ref. 8	Ref. 9	Ref. 10	Ref. 11
Architecture	1st ΔΣ CDC	SAR CDC	2nd ΔΣ CDC	3rd ΔΣ CDC	2nd ΔΣ CDC	3rd ΔΣ CDC
Technology (μm)	0.18	0.35	0.16	0.16	0.18	0.35
Supply (V)	1.8	3.3	1.8	1.2–1.8	2.6	3.3
Power (μW)	376	303	10.53	10.32 (at 1.2 V)	2340	15000
Area (mm^2)	0.66	0.07			0.67	5.58
Effective resolution (bit)	14.4	12.5	13.3	12.85	17.4	17.2
Capacitance range (pF)	20 (programmable)	16	0.8 ± 0.4	0.8 ± 0.26	10	10

A performance summary of the parameters and comparisons is shown in Table 2. The effective resolution from Refs. 8 and 9 was calculated and is shown in Table 2 for comparison. The effective resolution of the 16-bit delta-sigma CDC is 14.4 bits with a 10 pF input capacitance range. In Table 2, the proposed 16-bit delta-sigma CDC uses a simple first-order modulator architecture to obtain a low power and small-area characteristics, and has a high effective resolution of 14.4 bits by obtaining low noise characteristics. Also, the widest programmable input capacitance range among previous studies can be used in the humidity sensor applications of various input ranges.

4. Conclusions

A low-noise 16-bit delta-sigma CDC for sensing a capacitive humidity sensor was presented. The proposed 16-bit CDC used the delta-sigma modulator that adopted a chopper stabilization technique. The proposed delta-sigma CDC yielded a small area and a low power consumption by using a simple first-order delta-sigma modulator. As the chopper stabilization technique improved the effective resolution by 2.24 bits, the proposed delta-sigma CDC had a high effective resolution of 14.4 bits. To reduce the back-end digital processing power, the proposed delta-sigma CDC was fully integrated with the accumulator. For use with various capacitive humidity sensors of different input ranges, the proposed delta-sigma CDC was designed to

demonstrate a programmable wide input capacitance range. The chip was fabricated using the 0.18 μm CMOS process with an active area of 0.66 mm^2. The total power consumption of the proposed CDC was 376 μW with a 1.8 V supply.

Acknowledgments

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