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Supersteep Retrograde Channel on FinFET

Yong-Syuan Dai and Yu-Hsien Lin*

Department of Electronic Engineering, National United University,
1, Lienda Road, Miaoli 36003, Taiwan, R.O.C

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Supersteep retrograde (SSR) technology can improve the short-channel effects (SCEs) when device size is reduced. Additionally, it can reduce the leakage current of a device. We investigated the optimal process conditions for SSR technology. We determined whether the electromagnetic parameters of N-type and P-type fin field-effect transistors (FinFETs) can be improved using SSR technology through technology computer-aided design (TCAD) simulation. After the simulation, the transfer characteristic curve (I_D–V_G), I_{on}, I_{off}, drain-induced barrier lowering (DIBL), subthreshold swing (SS), and mobility parameters were employed to determine the advantages and disadvantages of using SSR technology for a FinFET. The results revealed that when SSR technology is used for a FinFET, superior characteristics are observed even when the width and length of the FinFET are reduced. The SSR simulation results reveal that, as the doping concentration in SSR technology increases, the electrical properties of the device improve.

1. Introduction

To follow Moore's law and resolve the short-channel effects (SCEs) attributable to the size reduction of two-dimensional (2D) transistors, the three-dimensional (3D) transistor was invented.[1,2] In this study, we used supersteep retrograde (SSR) technology to improve the SCEs in fin field-effect transistors (FinFETs).[3–5] SSR technology is a vertical heterogeneity doping technology used in channel engineering.[6] We aimed to identify the optimal size of FinFETs to which SSR technology is applied. Because of simulation software limitations, uniform doping was conducted in this research. We compared a FinFET before using SSR technology with one after using SSR technology by referring to the 7 nm process structure of the Taiwan Semiconductor Manufacturing Company (TSMC).[7] By referring to the 2015 International Technology Roadmap for Semiconductors (ITRS) 2.0, we determined that, for a FinFET, the gate voltage (V_G) is 0.8 V and the drain voltage (V_D) is 0.7 V.[8]

*Corresponding author: e-mail: yhlin@nuu.edu.tw
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2. Materials and Methods

We used technology computer-aided design (TCAD) simulation to compare the structure of a FinFET before and after SSR doping (the FinFET in the present study is referred to as the SSR FinFET after SSR doping).[9] The structure of the SSR FinFET is displayed in Fig. 1. The red characters in the figure are the SSR doping variables used in this study.

The experimental steps are as follows.

Step 1: We use a 3D mesh plot to ascertain the optimal height and width of the FinFET structure. The FinFET heights (*FH*s) in this study are 40, 45, and 50 nm. FinFET widths (*FW*s) are 3, 4, and 5 nm.

Step 2: The size of the optimal structure obtained after Step 1 is used to plot the I_D–V_G curve. Then, the optimal SSR doping concentration is obtained.

Step 3: We plot the I_D–V_G curve to ascertain the optimum SSR depth (doping range).

Step 4: Using the optimization results, the characteristics of the voltage and current of the FinFET and SSR FinFET are compared.

Tables 1 and 2 present the optimal electrical property simulation parameters and variables of doping adjusted with reference to the 2015 ITRS 2.0.

3. Simulation Result

3.1 FinFET structure of the optimal electrical properties through FinFET simulation

Figure 2 displays the simulation results for the N-type FinFET. Figure 2(a) shows that *Ion* is higher when *FH* and *FW* are higher. Figure 2(b) reveals that I_{off} is smaller when *FW* and *FH*

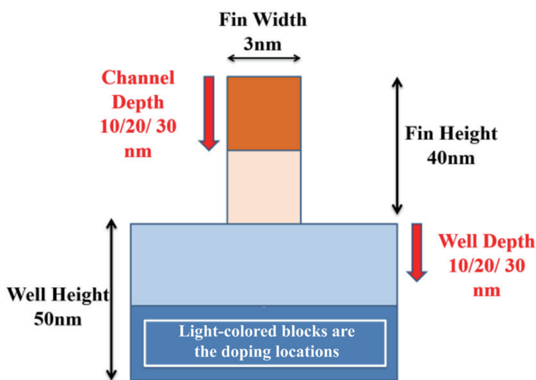


Fig. 1. (Color online) Structure of the SSR doping position and variables (orange: channel, blue: well).

Table 1
Doping variations of N-type and P-type FinFETs.

SSR doping concentration (cm^{-3})	SSR doping depth (nm)
5×10^{17}	10
10^{18}	20
10^{19}	30

Table 2
Simulation parameters of N-type and P-type FinFETs.

S/D doping (cm^{-3})	Channel doping (cm^{-3})	Channel height (nm)	Channel width (nm)	Gate length (nm)	Gate oxide thickness (nm)	Gate work function (eV)
10^{19}	10^{17}	40	3	14	4	4.63

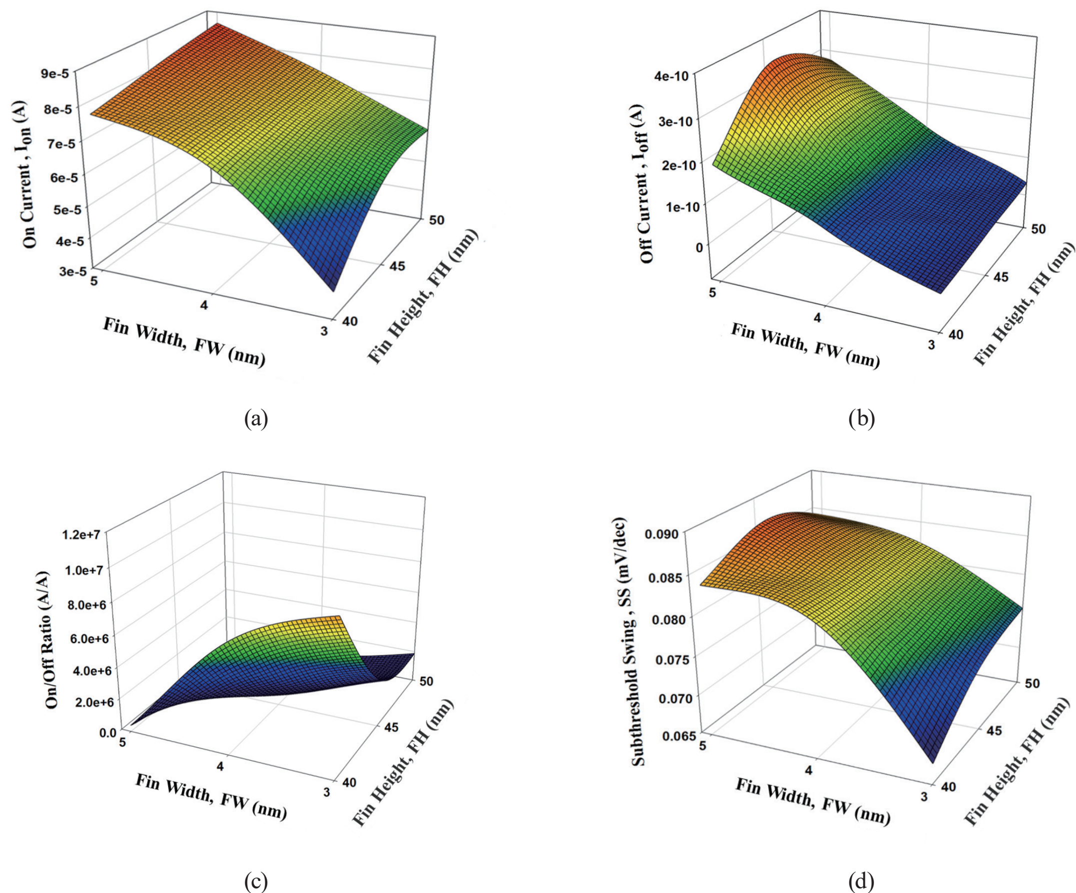


Fig. 2. (Color online) Simulation plots of the electrical properties of the N-type FinFET: (a) I_{on}, (b) I_{off}, (c) I_{on}–I_{off} ratio, and (d) *SS*.

are smaller. Figure 2(c) indicates that the on–off current ratio (I_{on}–I_{off}) is higher when *FW* and *FH* are smaller. Figure 2(d) shows that subthreshold swing (*SS*) is higher when *FW* and *FH* are smaller. The results for a P-type FinFET are presented in Fig. 3 and are similar to those for the N-type FinFET. Therefore, the optimal Fin structure has an *FH* of 40 nm and an *FW* of 3 nm.

3.2 Optimal depth of SSR doping

In Figs. 4 and 5, on the basis of the principle of I_{on}/I_{off}, the I_{on} and I_{off} at the retrograde depth (*Re.depth*) of 10 nm are the lowest. The I_{off} at the *Re.depth* of 20 nm is the second lowest, and I_{on} is the highest. After analyzing I_{on} and I_{off}, determining whether the electrical properties are more favorable at the *Re.depth* of 10 or 20 nm is difficult. The SS curve is steeper and the SS value is smaller when I_{on} is larger according to the on–off current ratio. Thus, optimal electrical properties are observed at the *Re.depth* of 20 nm. Table 3 shows the electrical properties of our structures.

Subsequently, we use the same SS principle to determine the electrical properties (Fig. 6). The *Re.depth* of 20 nm is optimal for obtaining superior electrical properties. Moreover, the

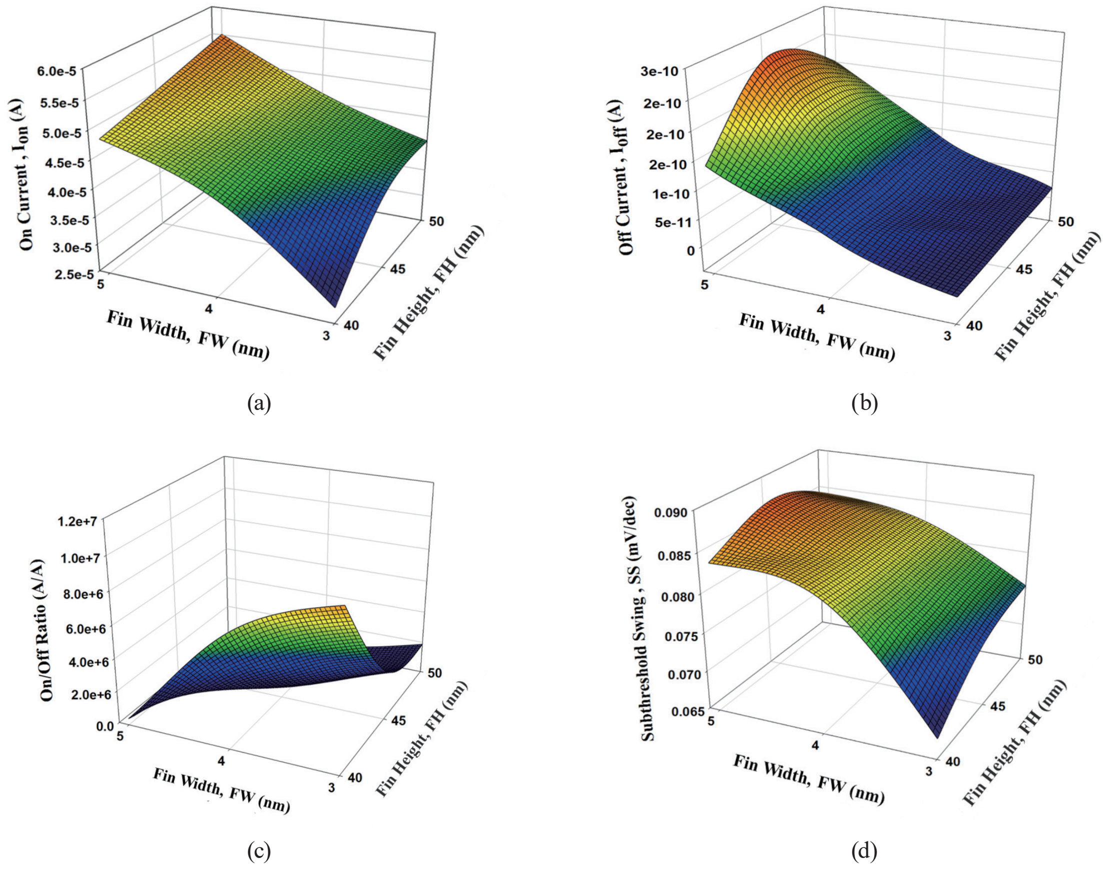


Fig. 3. (Color online) Simulation plots of the electrical properties of the P-type FinFET: (a) I_{on}, (b) I_{off}, (c) I_{on}–I_{off} ratio, and (d) *SS*.

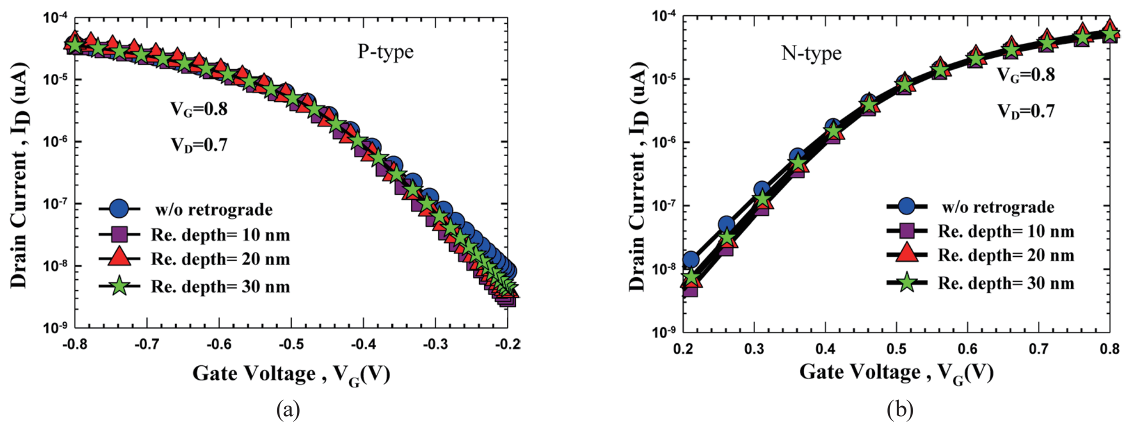
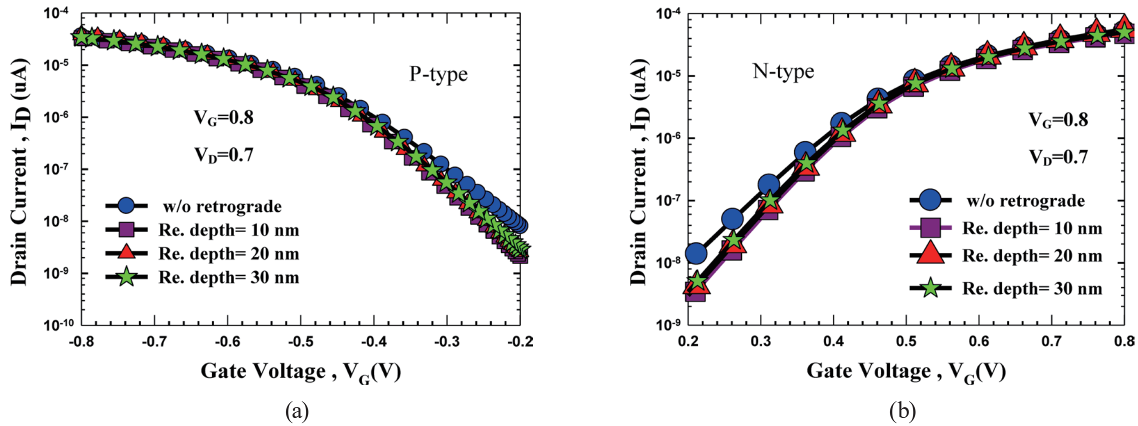


Fig. 4. (Color online) I_D–V_G graph for a fixed doping concentration of 5×10^{17} at three *Re.depths* of 10, 20, and 30 nm. (a) P-type and (b) N-type FinFETs.



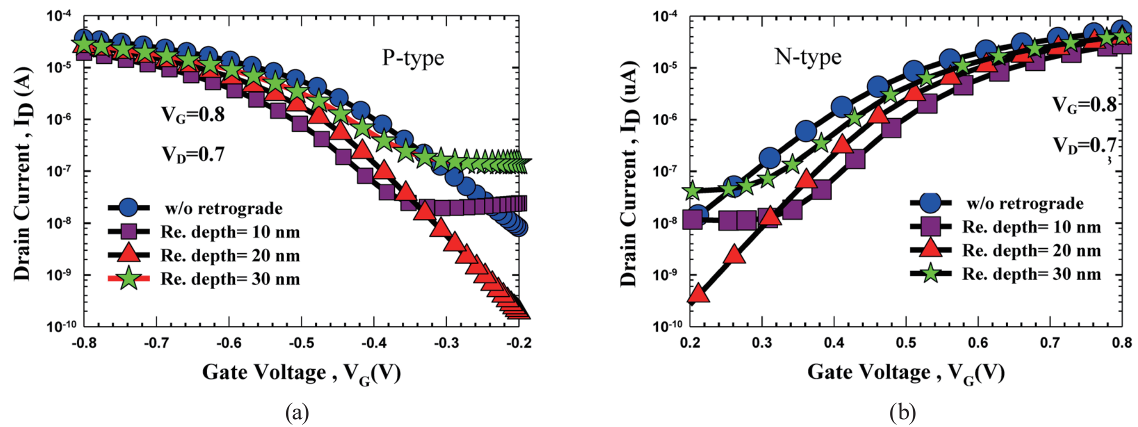
(a) (b)

Fig. 5. (Color online) I_D–V_G graph for a fixed doping concentration of 10^{18} at three *Re.depths* of 10, 20, and 30 nm. (a) P-type and (b) N-type FinFETs.

Table 3
(Color online) Electrical properties (Structure of max–min *FH*, *FW*).

N-type & P-type	I_{on}	I_{off}	On/off current ratio	SS
Fin Height ↑ Fin Width ↑	☺	—	—	—
Fin Height ↓ Fin Width ↓	—	☺	☺	☺

☺ represents the optimal combination of height and width for the same electrical properties.



(a) (b)

Fig. 6. (Color online) I_D–V_G graph for a fixed doping concentration of 10^{19} at three *Re.depths* of 10, 20, and 30 nm. (a) P-type and (b) N-type FinFETs.

*Re.depth*s of 10 and 20 nm have high I_{off} values even when the device is in the off state. This implies that the device produces some leakage current. Therefore, the *Re.depth* of 20 nm is optimal at a fixed doping concentration.

3.3 Optimal SSR doping concentration

On the basis of the conclusion drawn in Sect. 3.2, the *Re.depth* is 20 nm, and three doping concentrations, 5×10^{17}, 10^{18}, and 10^{19} cm^{-3}, are employed to identify the optimal doping concentration. By analyzing the on–off current ratio in Fig. 7, we observe that the lowest I_{on} is obtained at the doping concentration of 10^{19} cm^{-3}. Moreover, the I_{off} obtained when the doping concentration is 10^{19} cm^{-3} is considerably lower than those obtained at the other two concentrations. The electrical properties at the doping concentration of 10^{19} cm^{-3} are optimal. That is, the optimal doping concentration is 10^{19} cm^{-3} when the optimal *Re.depth* is 20 nm.

3.4 Device structure

Figure 8 displays the structure and electrical properties observed after TCAD simulations for the FinFET and SSR FinFET. The leakage current was significantly reduced, and the current was uniform in the SSR FinFET, as presented in Figs. 8(b) and 8(d).

3.5 I_D–V_G curve of FinFET and SSR FinFET

A significant decrease in I_{off} is observed in the N-type and P-type FinFETs after SSR doping, as presented in Fig. 9. This implies that the SSR FinFET has an optimal I_{off} and that SS is superior.

3.6 Drain-induced barrier lowering (DIBL)

Figure 10 demonstrates that the DIBL values are small and that the ability of the device to control the gate voltage is superior. We can observe that the difference in V_t, where V_D

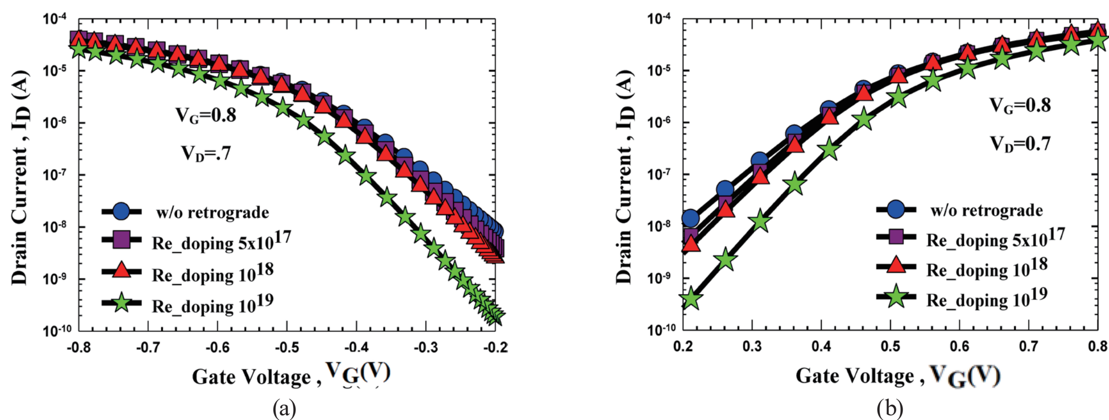


Fig. 7. (Color online) I_D–V_G graph for a fixed Re.depth of 20 nm at three doping concentrations of 5×10^{17}, 10^{18}, and 10^{19} cm^{-3}. (a) P-type and (b) N-type FinFETs.

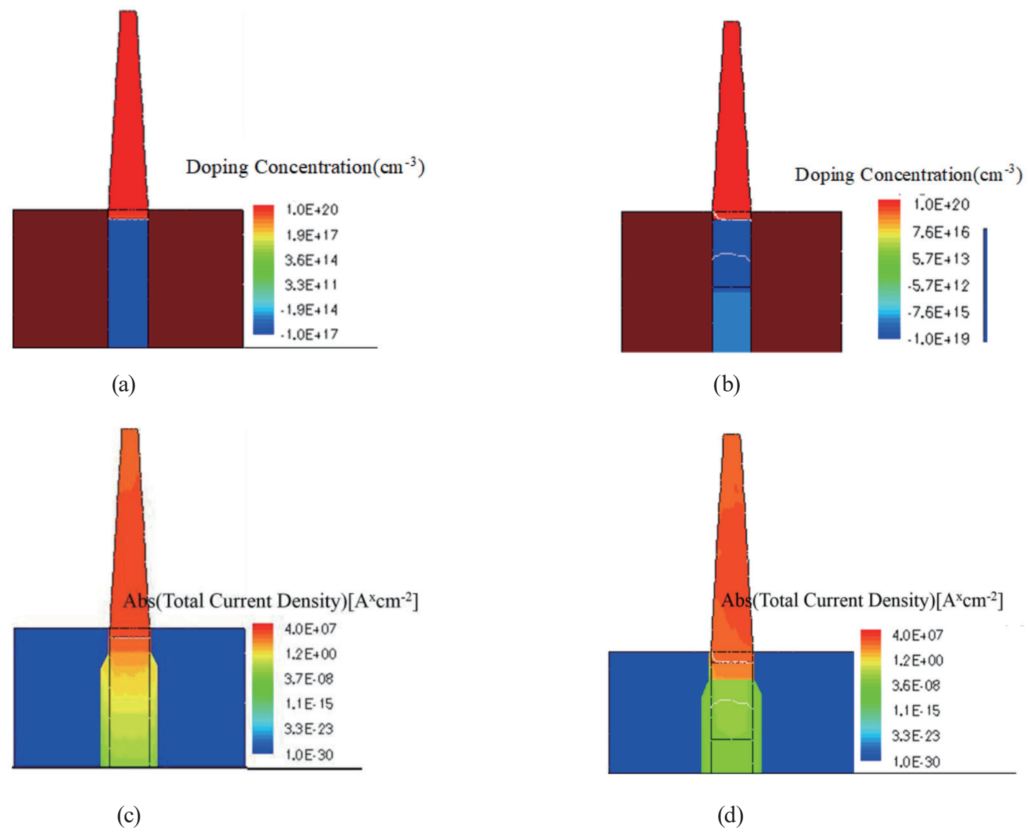


Fig. 8. (Color online) Structural and electrical property diagrams obtained after TCAD simulation. (a) Structure of the FinFET. (b) Structure of the SSR FinFET. (c) Electrical properties of the FinFET. (d) Electrical properties of the SSR FinFET.

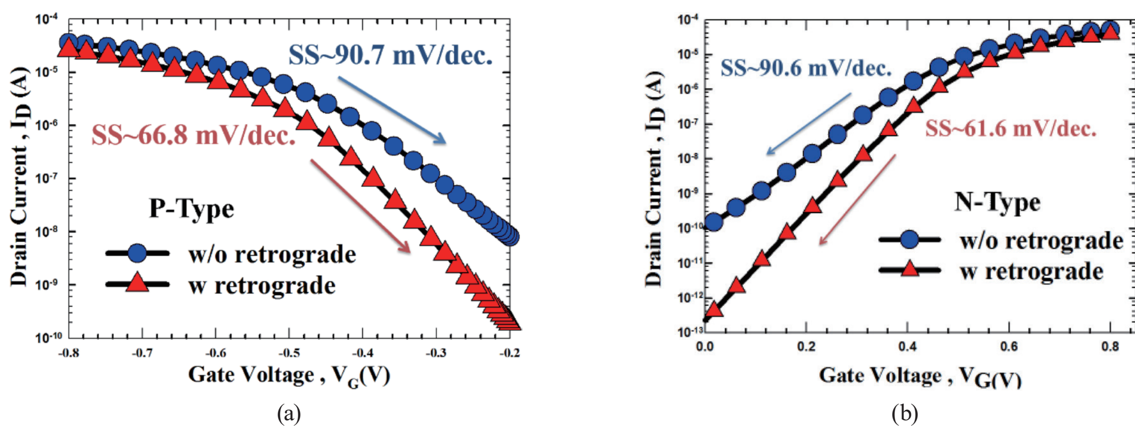


Fig. 9. (Color online) I_D–V_G graphs of FinFET and SSR FinFET. (a) P-type and (b) N-type FinFETs.

is between 1 and 0.05 with retrograde doping, is small after SSR doping. Therefore, the gate voltage control of the SSR FinFET is superior to that of the FinFET. Table 4 shows the summary table of DIBL (FinFET vs SSR FinFET) characteristics.

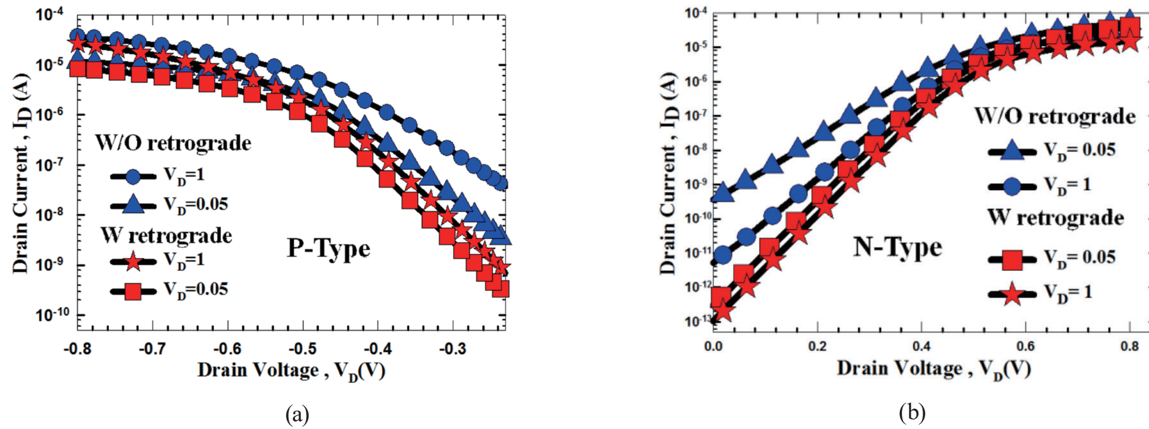


Fig. 10. (Color online) DIBL values of FinFET and SSR FinFET. (a) P-type and (b) N-type FinFETs.

Table 4
Characteristics of DIBL (FinFET vs SSR FinFET).

	N-type		P-type	
V_D = 0.05 V	FinFET	SSR FinFET	FinFET	SSR FinFET
SS_{avg}	77.6	64.3	78.9	66.4
V_{th} (V)	0.38	0.36	0.35	0.40
DIBL (mV/V)	74	21	74	21

4. Conclusions

SSR technology has been used for a long time,(10) and this study was conducted to identify the optimal parameters for using SSR technology, including the optimum SSR doping depth and concentration under an optimized structure. We are aware that SSR technology can overcome SCEs. In a previous study, SSR technology was used for a larger device and doping in the well.(11) In this study, we employed SSR technology for a small device using a channel. The most crucial finding from the simulation results is that SSR technology can effectively inhibit leakage current, as presented in Fig. 8.

The simulation results in Sect. 3 indicate that the electrical parameters, such as I_{off}, DIBL, SS, and mobility,(12) of the components of the N-type and P-type FinFETs improve after using SSR technology.

In summary, although I_{on} was reduced after SSR doping, I_{off} decreased considerably. Thus, some sacrifice of I_{on} is acceptable. Additionally, the DIBL values decreased considerably to 0.28 times less than those before SSR doping. *SS* decreased to a certain degree. In terms of mobility, SSR elements have superior electron mobility because the lattice scattering can be reduced effectively using SSR technology.

The TCAD simulation results revealed that the N-type and P-type FinFETs have a superior electrical performance when the width and height are small before using SSR technology. To identify the optimal component sizes, we compared the electrical properties before and after using SSR technology. We determined that the overall electrical performance is superior when the SSR doping concentration is high, and that the optimal doping depth is located at the median position for an optimal structure.

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