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Top-down Fabrication of Silicon Nanowires Using Thermal Oxidation and Wet Etching for Inertial Sensor Applications

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In this paper, we present a new top-down fabrication method of silicon nanowires (SiNWs) for inertial sensor applications. Recently, SiNW piezoresistive inertial sensors have attracted much attention because they can provide high sensitivities and high signal-to-noise ratios. For manufacturable inertial sensors based on SiNWs, the dimensions of SiNWs need to be reproducible and controllable. SiNWs should also be integrated with microscale structures and circuits. In the developed method, the width and thickness of SiNWs were controlled by thermal oxidation and silicon wet etching, respectively. SiNWs can be integrated with microscale structures, which were also fabricated by deep reactive ion etching and silicon wet etching. The width and thickness of the fabricated SiNWs were in the range of 65–163 and 56–131 nm, respectively. The reproducibility of SiNWs was also evaluated. The maximum standard deviation of the width of SiNWs was 30 nm, and that of the thickness was 46 nm. These results show that the SiNW dimensions are reproducible and that they can be accurately controlled.

1. Introduction

Because of their outstanding mechanical, electrical, and optical properties, silicon nanowires (SiNWs) have been widely used for sensing applications.[1–4] Recently, SiNWs have attracted much attention in inertial sensor applications owing to their high piezoresistance (PZR). Although the causes for outstanding PZR of SiNWs are unclear, the PZR of SiNWs is reported to be superior to that of bulk silicon.[5–7] Piezoresistive transduction based on SiNWs can provide high sensitivity and reduce the sizes of sensor structures. Therefore, SiNWs are expected to be a potential breakthrough candidate for transduction methods.

For inertial sensors based on SiNWs, sensor characteristics determined by the dimensions of SiNWs need to be controllable within the tunable range of electronics. Also, SiNWs have to be integrated with microscale structures for a proof mass and spring. In the bottom-up fabrication methods of SiNWs, the vapor-liquid-solid growth mechanism has widely been employed.[8–10]

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By using metal catalysts and reactants, SiNWs are grown via chemical vapor deposition (CVD). The dimensions of SiNWs depend on the catalyst particle size. SiNWs with a diameter of a few nanometers can be fabricated. However, metal contamination in SiNWs occurs during the bottom-up fabrication. In addition, the dimension, orientation, and position of SiNWs cannot be precisely controlled by this method, which is the main challenge for inertial sensor applications.

In the top-down fabrication methods, SiNWs can be easily fabricated by lithography and dry etching, without the orientation or alignment issues. SiNWs are generally fabricated on a silicon-on-insulator (SOI) wafer with a thin silicon top layer and by electron beam lithography (EBL).[11,12] However, the dimensions of SiNWs are limited by the top layer of a thin SOI wafer. Also, the thin SOI wafer and EBL process are expensive. SiNWs are also reported to be fabricated by wet etching with (100) silicon wafers and thermal oxidation.[13–15] The control of etch dimensions is difficult because fast etching (100) planes are at vertices of convex corners, which have high etching rates. More recently, SiNWs have been fabricated using scallops inherent in deep reactive ion etching (DRIE).[16] The width and thickness of SiNWs are defined by EBL and DRIE, respectively. However, it is a challenge to control the thickness of SiNWs because the characteristics of the DRIE vary considerably with loading effects and equipment conditions.[17]

Several sensor applications based on SiNWs have also been studied. SiNW piezoresistive inertial sensors have been proposed.[18,19] Similar to previous studies,[11,12] SiNWs are formed on a thin SOI wafer, and the epitaxy silicon process is performed to form microscale sensor structures. Since SiNWs are buried at the bottom of microscale structures, additional processes are required to access the SiNWs. In addition, cantilever air flow sensors based on SiNW using a thin SOI wafer have been proposed.[20,21] A backside DRIE and focused ion beam are used to form sensor structures such as flow channels and cantilevers.

In this paper, we present a new top-down fabrication method of suspended SiNWs for inertial sensor applications. The developed method has the following advantages. First, the orientation and position of SiNWs can be easily controlled by top-down patterning. Second, by using the developed method, the width and thickness of SiNWs can be controlled independently, which are determined by thermal oxidation and silicon wet etching, respectively. Last but not the least, SiNWs integrated with microscale structures are easily fabricated by the ensuing DRIE and silicon wet etching. As schematically shown in Fig. 1, inertial sensors based on highly sensitive SiNWs can be developed using the developed method. Inertial sensors based on SiNWs consist of a proof mass suspended by springs and SiNWs, and the motion of the proof mass can be detected by changing the resistance of the SiNWs.

The rest of this paper is organized as follows. The detailed fabrication process of SiNWs for inertial sensors is explained in Sect. 2. The results of SiNWs fabricated by the developed method are described in Sect. 3. Conclusions are drawn in Sect. 4.

2. Fabrication of SiNWs

The developed top-down fabrication of SiNWs is derived from the sacrificial bulk micromachining process developed by our group.[22,23] The detailed fabrication process is

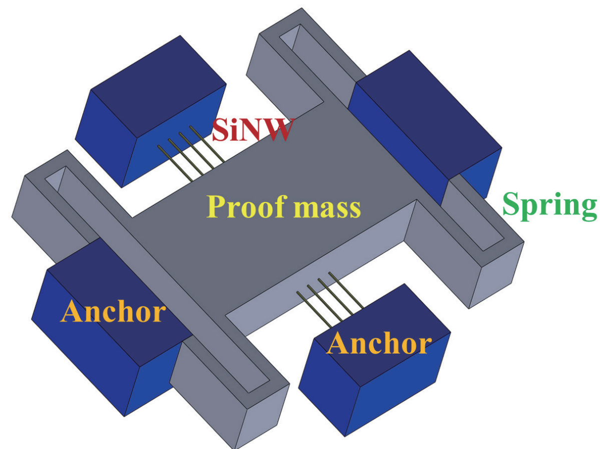


Fig. 1. (Color online) Conceptual schematic of piezoresistive inertial sensor based on SiNWs.

illustrated in Fig. 2. A (111) silicon wafer was first prepared. As shown in Fig. 2(a), a 0.5-μm-thick oxide was deposited onto the wafer using a plasma-enhanced CVD (PECVD) with a power of 350 W. The flow rates of both tetraethyl orthosilicate (TEOS) and O_2 were 150 sccm. Figure 2(b) shows that the GXR-601 photoresist (PR) was patterned by photolithography. The PR was spin coated at 4000 rpm and was exposed to an ultraviolet light source of 365 nm wavelength. Following the exposure, the PR was developed in an AZ 300 MIF developer. As shown in Fig. 2(c), the oxide was patterned by an inductively coupled plasma etching. CHF_3 was used with a flow rate of 90 sccm. Platen radiofrequency (RF) power and coil RF power were 75 and 2700 W, respectively. Subsequently, silicon blocks of 1.5 × 1 μm^2 size were formed by a DRIE [Fig. 2(d)]. The DRIE was a cyclic process, which consisted of deposition and etching steps. C_4F_8 with a flow rate of 100 sccm and SF_6 with a flow rate of 100 sccm were used in the deposition and etching steps, respectively, while platen RF powers were 1 and 13 W for the respective steps. In both steps, the coil RF power was 825 W. As shown in Fig. 2(e), a 700-nm-thick thermal oxide was generated by oxidation, which defined the widths of SiNWs. The oxidation was performed at 1000 °C for approximately 2 h. H_2 with a flow rate of 7000 sccm and O_2 with a flow rate of 6500 sccm were used. Next, the oxide was dry etched to expose the silicon at the trench bottom [Fig. 2(f)], and the exposed silicon was etched to a depth of 30 μm by the DRIE [Fig. 2(g)]. Finally, as shown in Fig. 2(h), the silicon wet etching was performed using a 45 wt% potassium hydroxide solution at 90 °C to define the thicknesses of SiNWs. No convex corners were exposed to the wet etch solution, and only the bottom (111) plane was etched. Therefore, the thickness of SiNWs can be easily controlled.

3. Fabrication Results and Discussion

The results of SiNWs fabricated by the developed method are presented. The width and thickness of the SiNWs can be controlled by the thermal oxidation and silicon wet etching independently. Figure 3 shows the fabricated SiNW with the width and thickness of 65 and 56

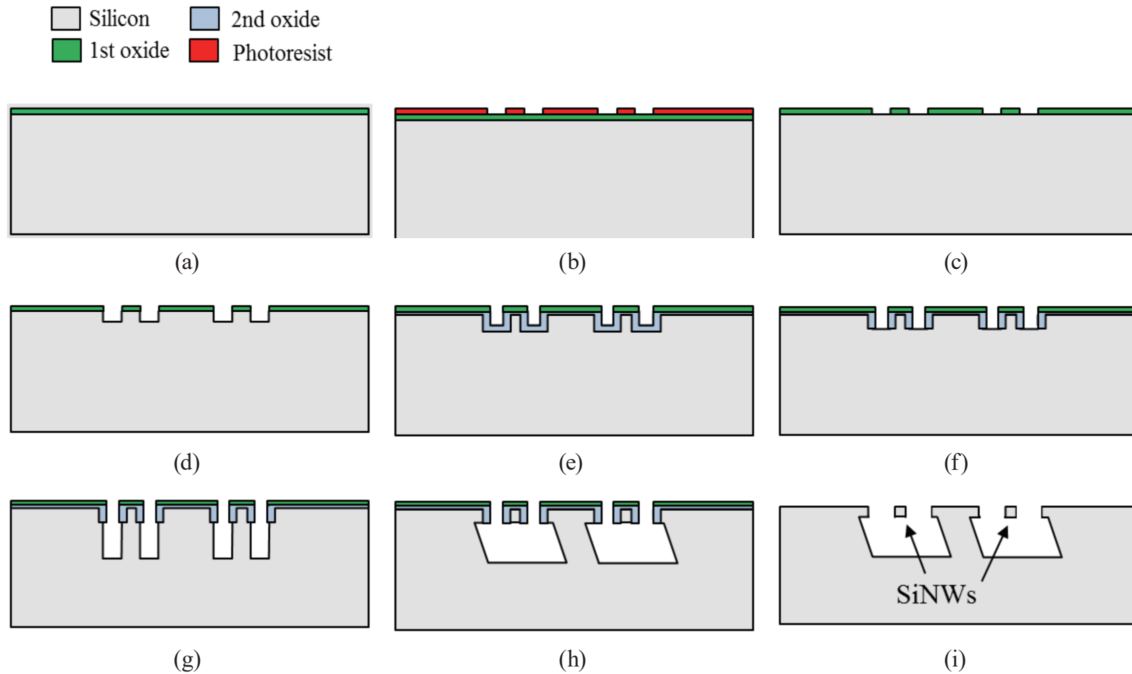


Fig. 2. (Color online) Fabrication process of SiNWs on (111) silicon. (a) Oxide deposition, (b) photolithography, (c) oxide patterning, (d) silicon etch using DRIE, (e) thermal oxidation, (f) oxide dry etch, (g) silicon etch using DRIE, (h) silicon wet etch, and (i) oxide wet etch (optional).

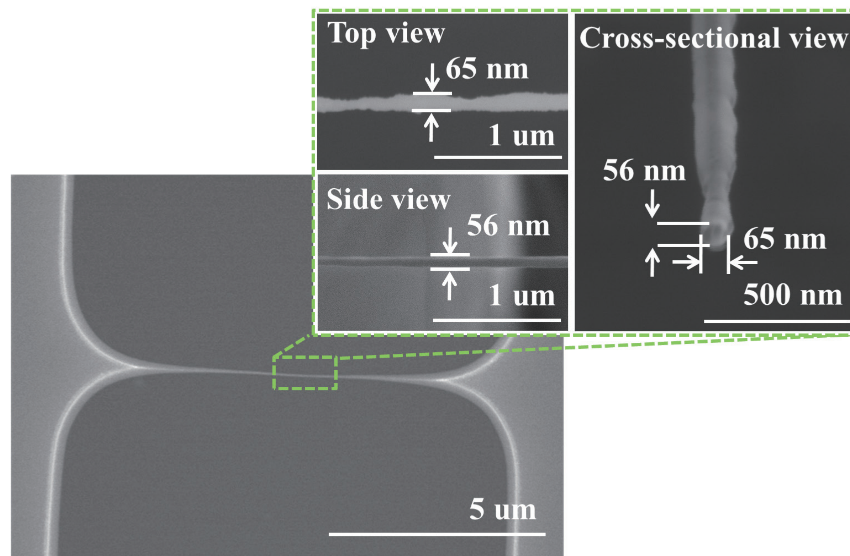
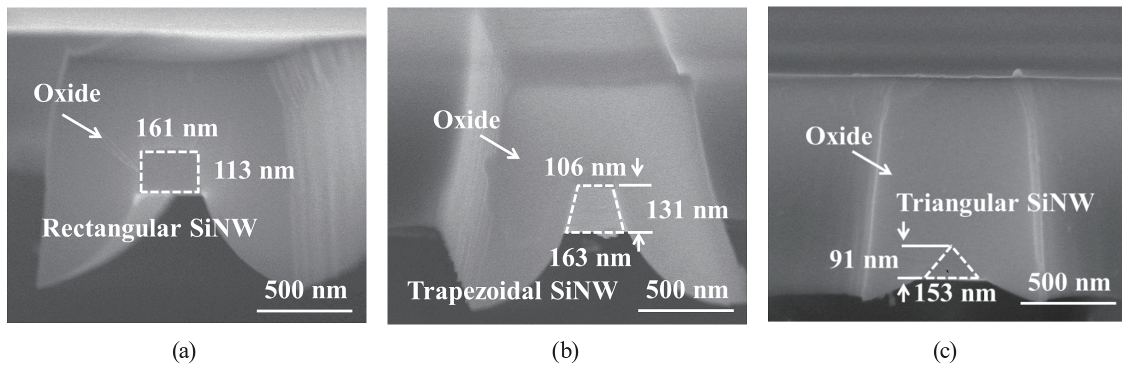


Fig. 3. (Color online) SEM image of SiNW.

nm, respectively; this is the smallest fabrication result in the present work. The length of the SiNW is 7 μm, and the length/width ratio is 108.

SiNWs having various shapes can also be fabricated by the developed method. Figure 4(a) shows a rectangular SiNW with the width and thickness of 161 and 113 nm, respectively. In



(a) (b) (c)

Fig. 4. Various shapes of SiNWs: (a) rectangular SiNW, (b) trapezoidal SiNW, and (c) triangular SiNW.

addition, a fabricated trapezoidal SiNW is shown in Fig. 4(b); the SiNW has upper and lower bases and heights of 106, 163, and 131 nm. The shape of the SiNW is determined by the silicon block shape, which is affected by the etch depth and scallop of a DRIE. Figure 4(c) shows a triangular SiNW having a base and height of 153 and 91 nm, respectively. By increasing the thermal oxidation time, a thermal oxide is fully grown at the top part of the silicon block, and a triangular shape can be formed at the bottom part of the silicon block.

Figure 5 shows SiNWs suspended by two anchors with a depth of 30 μm. The depth of these anchors is two or three orders of magnitude larger than the dimension of SiNWs, suggesting that the developed method can provide monolithic integration of SiNWs and microscale structures. Furthermore, SiNWs can easily be accessed on ensuing processes because they are formed on the surface of a silicon wafer.

The reproducibility of SiNWs was evaluated with respect to the process conditions as shown in Fig. 6. Five SiNWs were measured under each condition. Figure 6(a) shows the width variation of SiNW with respect to the thermal oxidation time under the mask pattern having a width of 1.5 μm. The width of SiNW was inversely proportional to the thermal oxidation time. The maximum standard deviation of the width was 21 nm. Figure 6(b) shows the thickness of SiNW as a function of silicon wet etching time. The thickness of SiNW decreased with increasing silicon wet etching time. The maximum standard deviation of the thickness was 46 nm. These results show that the dimensions of SiNWs fabricated using the developed method are relatively reproducible and controllable.

Controlling the dimensions of SiNWs is an important issue in SiNW fabrication. The PZR of SiNW is reported to be enhanced when its dimension is reduced.[5,6] However, SiNW having a small dimension can be vulnerable to disturbance such as external shock. In inertial sensors based on SiNW, minimizing the dimension of SiNW can improve sensitivity but reduce robustness. Therefore, a small SiNW with a dimension of less than 100 nm is not always required for SiNW-based inertial sensors.[12,13] The trade-off between sensitivity and robustness should be considered for determining the dimension of SiNW, and optimizing the dimension with respect to the abovementioned sensor parameters is currently in progress.

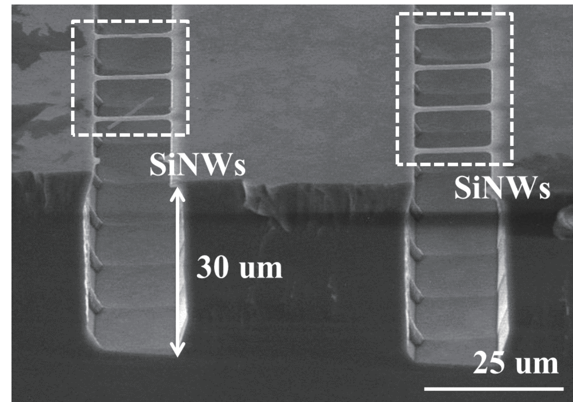


Fig. 5. Suspended SiNWs integrated with two silicon anchors with a trench depth of 30 μm.

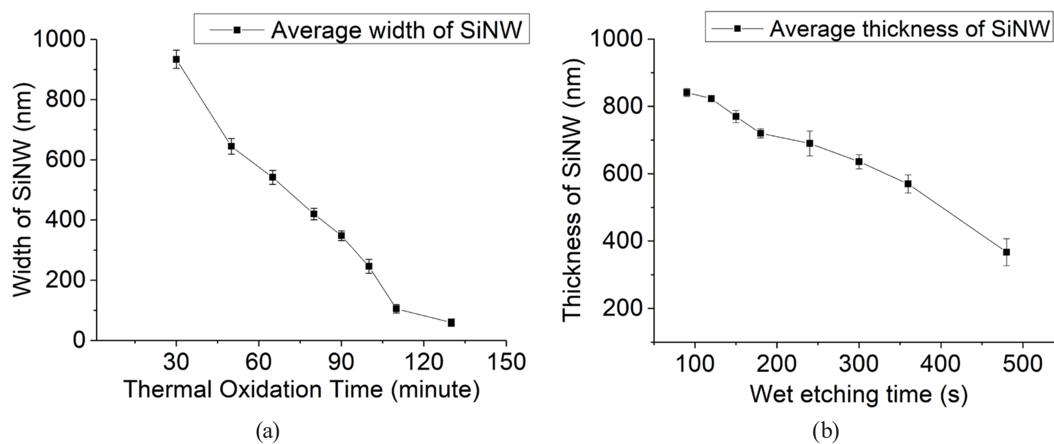


Fig. 6. Evaluation of the reproducibility of SiNW: (a) width of SiNW with respect to thermal oxidation time and (b) thickness of SiNW with respect to silicon wet etching time.

4. Conclusions

A new top-down fabrication process of SiNWs for inertial sensors is presented. The width and thickness of SiNWs were controlled by thermal oxidation and silicon wet etching, respectively. The SiNWs integrated with microscale structures were also fabricated by the ensuing DRIE and silicon wet etching. The reproducibility of SiNWs fabricated by the developed method was evaluated. These fabrication results clearly show that SiNW dimensions were reproducible and controllable, and the monolithic integration of SiNWs and microscale structures was allowed. The developed method is potentially expected to be used for the fabrication of highly sensitive, reproducible, and low-cost inertial sensors based on SiNWs. Improvements to reduce fabrication tolerance and optimization of the dimensions of SiNWs suitable for inertial sensors are currently being studied and will be reported in the future.

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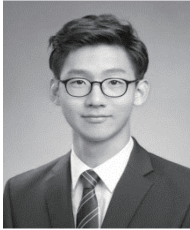

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