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Low-noise Reconfigurable 12- to 16-bit Delta-Sigma Capacitance-to-digital Converter with Chopper Stabilization Technique

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This paper presents a first-order delta-sigma (ΔΣ) capacitance-to-digital converter (CDC) with low noise characteristics and a reconfigurable resolution of 12 to 16 bits. The proposed ΔΣ CDC is implemented as a first-order ΔΣ modulator with switched capacitor (SC) integrator and comparator. The resolution can be reconfigured by the accumulator using the reconfigurable 12- to 16-bit up-counter. ΔΣ schemes are widely used for low-noise applications owing to the ability of the ΔΣ modulator to reduce in-band white noise through its inherent noise-shaping characteristic. Low-frequency colored noises such as flicker (1/*f*) noises still remain. In order to reduce the low-frequency colored noise component, a chopper stabilization technique is exploited using the SC integrator of the ΔΣ CDC. The proposed ΔΣ CDC also controls the offset calibration capacitors that adjust the DC offset. This is caused by a capacitor mismatch owing to process variation and the parasitic capacitance of the input capacitive sensor. The ΔΣ CDC is fabricated by using the standard 0.18 μm 1P6M complementary metal-oxide-semiconductor (CMOS) process with an active area of 0.66 mm^2. The total current consumption for the 16-bit ΔΣ CDC is 141 μA with a 1.8 V supply.

1. Introduction

Capacitive sensors are widely used in variable sensor applications for measuring pressure, humidity, and acceleration. Recently, many applications have begun to require sensor interface circuits of simple structure and high performance to allow enhancements such as increased resolution. Conventional capacitive sensor interface circuits consist of a capacitance-to-voltage converter and an analog-to-digital converter (ADC).[(1)] These interface circuits have disadvantages in terms of area, power consumption, and complexity of the circuit. In order to achieve the above requirement, a directly conversable capacitance-to-digital converter (CDC) can be used. Several interface circuits have been studied that demonstrate a directly conversable CDC such as a successive approximation register (SAR) or delta-sigma (ΔΣ) CDC.[(2–8)] SAR

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CDCs have a high speed and low power consumption. However, they are limited in obtaining a high resolution. ΔΣ CDCs have an advantage in obtaining a high resolution with shaped white noise. The noise-shaping characteristic of the ΔΣ modulator allows for the removal of white noise. Higher-order ΔΣ modulators can more effectively reduce the in-band white noise and allow for more precise readings of capacitance difference. However, with these enhancements, the circuit becomes increasingly complicated and requires a larger area.[5] This paper presents a first-order ΔΣ CDC with low noise characteristics. Improving the resolution of the first-order ΔΣ CDC can be achieved by reducing other in-band noises.

The DC offset and low-frequency colored noise are additional degradation factors to consider. The DC offset is caused by capacitor mismatch owing to the process variation and parasitic capacitor of the input capacitive sensor. The DC offset can be removed by applying calibration capacitors in parallel with the capacitor of the sensor.[4,6] The white noise and DC offset are thereby reduced, but low-frequency colored noises such as flicker (1/*f*) noise still remain. The proposed ΔΣ CDC use the first-order ΔΣ modulator with switched capacitor (SC) integrator and comparator. By applying the chopper to the SC integrator, inband 1/*f* noise to the outband is modulated.[9] The outputs of the comparator are accumulated by the reconfigurable 12- to 16-bit accumulator. The fully integrated accumulator can reduce back-end digital processes.

2. Operation of Proposed First-order ΔΣ CDC

2.1 Architecture of the proposed ΔΣ CDC

The architecture of the proposed first-order ΔΣ CDC is shown below in Fig. 1. The proposed first-order ΔΣ CDC consists of the parasitic capacitance cancellation input stage, SC integrator, comparator, and accumulator. At the input stage of the ΔΣ CDC, the programmable capacitor array, added in parallel to the sensor capacitors, is used for DC offset control. The sensor driving voltages can be connected through internal voltage VDD and GND. The SC integrator using chopper stabilization and the comparator are operated by the first-order ΔΣ modulator. The outputs of the comparator are accumulated by the reconfigurable 12- to 16-bit accumulator. The internal relaxation oscillator, current reference, and IVREF generate the 1 MHz main clock and the bias voltage used in the ΔΣ CDC.

2.2 Operation of proposed first-order ΔΣ CDC with chopper stabilization

Figure 2 shows the schematic of the proposed first-order ΔΣ CDC for the capacitive sensor. By using the SC integrator, the proposed first-order ΔΣ CDC directly converts the capacitance difference of the capacitive sensor to digital codes. The frequencies of the nonoverlapping clocks, P_1 and P_2, are 512 kHz, which is half the main frequency. When switching from P_1 to P_2, the charges stored in the sensor and reference capacitors are delivered to the integrator. If the charge is delivered by the sensor capacitor and C_{ref} is balanced, then the output of the integrator is V_{ref}.[2] The polarity of the charge delivered by C_{ref} is adjusted to obtain the

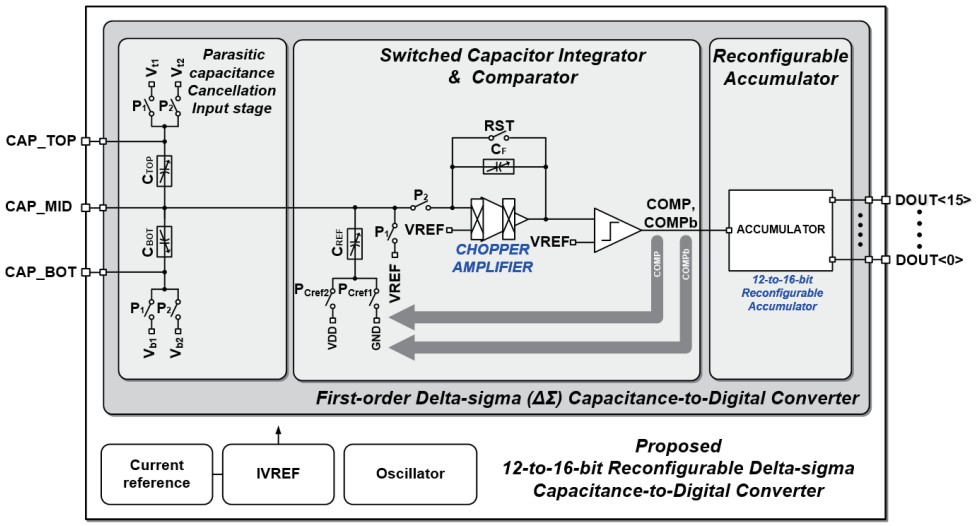


Fig. 1. (Color online) Architecture of the proposed first-order ΔΣ CDC.

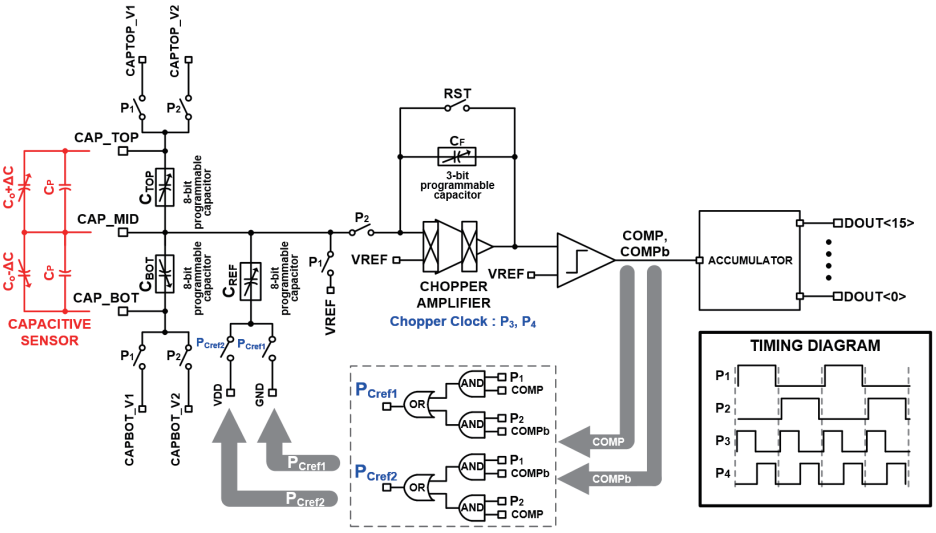


Fig. 2. (Color online) Schematic of the proposed first-order ΔΣ CDC.

integrator output V_{ref}. The polarity of the charge to be stored in C_{ref} is then determined on the basis of the output of the comparator. The capacitor sensors operate using a voltage driving method. The driving voltage can use internal voltage VDD and GND, or external arbitrary voltages Cap_top_v1 (V_{t1}), Cap_top_v2 (V_{t2}), Cap_bot_v1 (V_{b1}), and Cap_bot_v1 (V_{b2}) are used.

Equation (1) is the result of the charge equation when switching from P_1 to P_2. A positive polarity is applied when the comparator output is high, and a negative polarity is applied when the comparator output is low.

$$\Delta V = \frac{(V_{t1} - V_{t2})(C_o + \Delta C) + (V_{b1} - V_{b2})(C_o - \Delta C) + 2COMPV_{ref}C_{ref}}{C_f} \quad (1)$$

The input capacitance range can be obtained using Eqs. (2) and (3). When ΔV_{OUT} and *COMP* are low, the minimum ΔC is obtained.

$$\Delta C > \frac{\{-(V_{t1} - V_{t2}) + (V_{b1} - V_{b2})\}C_o - 2V_{ref}C_{ref}}{(V_{t1} - V_{t2}) - (V_{b1} - V_{b2})} \quad (2)$$

When $\Delta Vo < 0$ and *COMP* remains high, the maximum ΔC is obtained.

$$\Delta C < \frac{\{-(V_{t1} - V_{t2}) + (V_{b1} - V_{b2})\}C_o + 2V_{ref}C_{ref}}{(V_{t1} - V_{t2}) - (V_{b1} - V_{b2})} \quad (3)$$

The driving voltages V_{t1}, V_{t2}, V_{b1}, and V_{b2} are used to adjust the input range and offset capacitance. Using internal voltage VDD and GND, the input range is given by

$$-\frac{C_{ref}}{2} < \Delta C < \frac{C_{ref}}{2}, \quad (4)$$

where C_{ref} is an 8-bit programmable capacitor of 100 fF unit capacitance. As such, C_{ref} has a maximum range of 25.6 pF.

The proposed accumulator has dual 16-bit up-counters that count the comparator output and clock P_1 (Fig. 3). The first 16-bit up-counter counts the 12 or 16 bits of clock P_1. This is

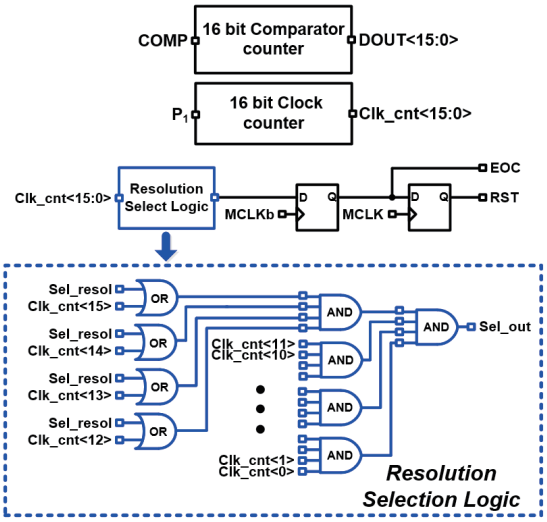


Fig. 3. (Color online) 12- to 16-bit reconfigurable accumulator with dual 16-bit up-counter.

according to the resolution selection and outputs end-of-clock (EOC) and reset (RST) signals. The EOC and RST signals are output when all 16 outputs of the clock counter are high. If the 12-bit resolution is selected, bits 13 to 16 are set high. The second 16-bit up-counter counts the comparator output until it is reset.

To obtain low noise characteristics, the chopper stabilization technique was applied to the SC ΔΣ modulator. The integrator is of the single-ended folded cascade amplifier type. The chopper was applied inside the integrator. The chopper frequency is twice the sampling frequency. The integrator 1/*f* noises of the inband are modulated to the outband.

2.3 Modeling of ΔΣ modulator using MATLAB Simulink

The effect of chopper stabilization is shown through simulation results using MATLAB Simulink. Figure 4 shows the structure of the MATLAB model of the ΔΣ modulator. The MATLAB model of the ΔΣ modulator consists of a signal generator, an integrator, a 1-bit quantizer, a zero-order hold, a decimation filter, and band-limited white noise.

3. Design and Simulation Results of Proposed IC

3.1 Design of proposed first-order ΔΣ CDC

The layout of the proposed first-order ΔΣ CDC is shown in Fig. 5. The ΔΣ CDC was designed by using the standard 0.18 μm 1P6M complementary metal-oxide-semiconductor (CMOS) process with an active area of 0.66 mm^2. The total current consumption for the 16-bit ΔΣ CDC is 141 μA with a 1.8 V supply. The current consumption of the analog parts is 68 μA.

3.2 Operation of proposed first-order ΔΣ CDC with chopper stabilization

The proposed ΔΣ CDC was simulated using Spectre. The capacitive sensor was modeled as a voltage-controlled variable capacitor for simulation. The input signal is a 1 kHz sine wave, and Δ*C* sweeps the minimun-maximum range of 25.6 pF. Figure 6(a) shows the change in capacitance with time. Figure 6(b) shows that the voltage-controlled capacitance and the number of the comparator output "high" is proportional to Δ*C*.

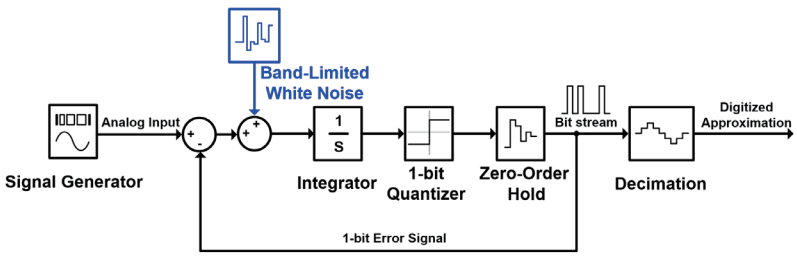


Fig. 4. (Color online) Structure of the MATLAB model of the ΔΣ modulator.

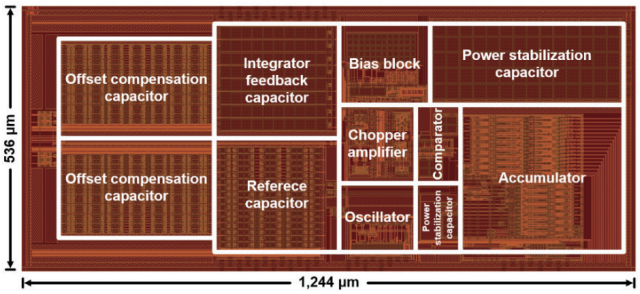
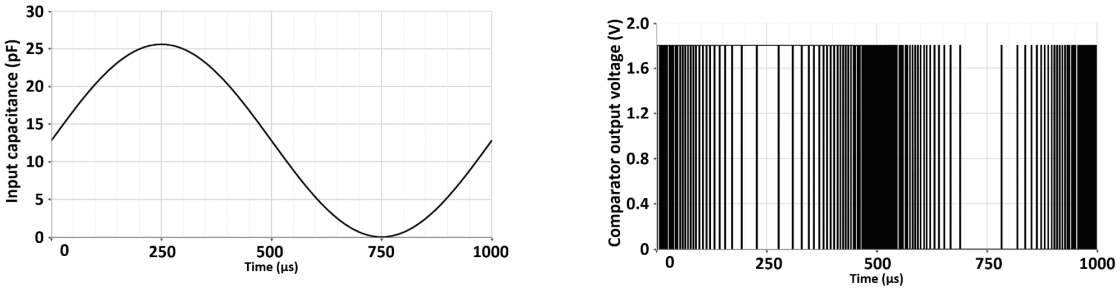


Fig. 5. (Color online) Layout of proposed first-order ΔΣ CDC.



(a) (b)

Fig. 6. (a) Change in capacitance with time and (b) comparator output of the proposed ΔΣ CDC.

Figure 7 shows the input-referred noise of the integrator caused by chopper on/off. The effect of chopper stabilization reduces the input-referred 1/*f* noise of the SC integrator. The integrated input-referred noises from DC to 100 kHz of chopper on/off are 35 and 147 nV/$\sqrt{\text{Hz}}$.

The fast Fourier transform (FFT) result of the zero-order hold output is shown in Fig 8. The input signal is a 3.1 Hz sine wave. The input-referred noise results of the proposed integrator are used for MATLAB simulation. In the FFT result of simulation, the signal-to-noise and distortion ratio (*SINAD*) as well as the effective number of bits (*ENOB*) are calculated in Eqs. (5) and (6), respectively.

$$SINAD = 20\log 10(\frac{signal}{nad}) \tag{5}$$

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{6}$$

When calculating *SINAD*, the chopper improved from 72.72 to 85.18 dB. The *ENOB* of the proposed ΔΣ CDC is calculated as 13.8 bits. Without chopper stabilization, the *ENOB* is 11.8 bits.

A performance summary of parameters and comparisons are noted in Table 1. The proposed first-order ΔΣ CDC achieved an *ENOB* of 13.8 bits with low noise characteristics. The accumulator for digital code outputs consumes some power but effectively reduces the back-end computing power.

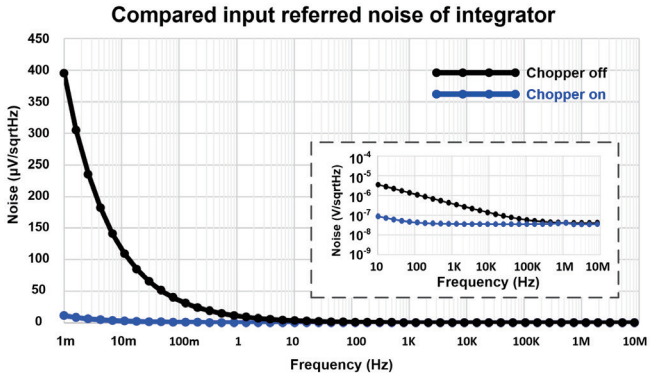


Fig. 7. (Color online) Compared input-referred noise of integrator caused by chopper on/off.

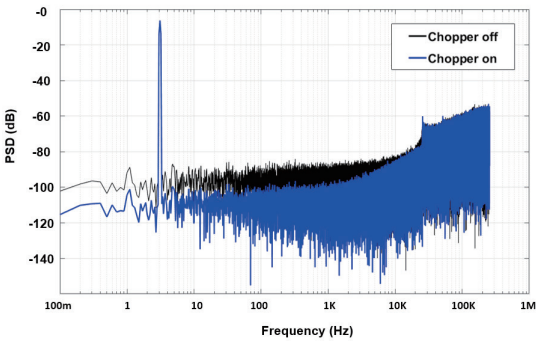


Fig. 8. (Color online) FFT result of comparator output.

Table 1
Performance comparison and summary of parameters.

	This work	Ref. 5	Ref. 6	Ref. 7	Ref. 8
Architecture	1st ΔΣ	3rd ΔΣ	1st ΔΣ	3rd ΔΣ	3rd ΔΣ
Output format	Digital code	Bit stream	Bit stream	Bit stream	Bit stream
Technology (μm)	0.18	0.35	0.35	0.16	0.35
Supply (V)	1.8	3.3	3.3	1.2–1.8	1.8–2.5
Power (μW)	252	15000	1440	10.3	828@1.8 V
Active area (mm^2)	0.66	5.58	0.048	0.28	0.391
Capacitance range (pF)	25.6	10	−0.5–0.5	0.54–1.06	—
ENOB (bit)	13.8 (Simulated result)	17.2 (Measured result)	10.2 (Measured result)	12.5 (Measured result)	12.2 (Measured result)

4. Conclusions

The low-noise first-order ΔΣ CDC is presented for the capacitive sensor. The proposed ΔΣ CDC reduces in-band white noise with noise shaping characteristic as well as low-frequency colored noise with chopper stabilization. Through simulation results, the *ENOB* of the proposed ΔΣ CDC is 13.8 bits. The chopper stabilization has improved the resolution by 2 bits. The proposed first-order CDC directly converts the capacitance to reconfigurable 12- to 16-bit digital codes and outputs them. To reduce the computing power required for back-end digital processing, the proposed interface circuit fully integrates the 12- to 16-bit reconfigurable accumulator. The layout of the proposed interface circuit occupies an area of 0.66 mm^2 in a 0.18 μm 1P6M CMOS process. The total current consumption is 141 μA with a 1.8 V supply.

Acknowledgments

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