Sensors and Materials, Vol. 30, No. 4 (2018) 833–843
MYU Tokyo

S & M 1542

Characteristics of Lock-in Thermography Signal from Solder Bump Cracking in Wafer-level Chip Scale Packaging for Internet of Things Applications

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(Received October 23, 2017; accepted December 20, 2017)

Keywords: lock-in thermography, indium-antimonide, infrared, WLCSP, fault location

Internet of Things (IoT) devices are increasingly incorporating miniature multilayered integrated architectures. However, the localization of faults in the interconnection of solder bumps remains challenging. The problem of solder bump cracking (SBC), which causes failure of interconnections subjected to evaluation of board-level reliability (BLR) in wafer-level chip scale packaging (WLCSP) for IoT applications, is studied. Lock-in thermography (LIT) monitoring is a promising method for failure analysis (FA) of SBC. This method makes use of indium-antimonide (InSb) as the infrared (IR) sensor. In this study, we characterized the drop test behavior of WLCSP and the critical units located at the printed circuit board (PCB) center. LIT is shown to enable the detection of the fault location between the IoT chip and PCB in complex daisy chain interconnections, and more accurate detection as a result of applying LIT to thermal imaging for the resistive openings of SBC is discussed. The experimental results show that the employment of LIT enhances the visibility of the resistive openings. The analysis method can also be extended to shorts or leakage currents in thermally active failures, especially in packaged semiconductors.

1. Introduction

While people are increasingly aware of the Internet of Things (IoT) and the promise of connecting billions of things together, many system designers are not aware of the packaging changes that are required to achieve this innovation.(1) These technologies support the following features: sensing multifunction, a smaller form factor, higher integration density, higher bandwidths, lower power, lower production cost, and higher reliability.(2) The semiconductor industry is well known for meeting the packaging needs related to the product development cycle time of new, innovative products based on available package technologies.

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http://dx.doi.org/10.18494/SAM.2018.1784

ISSN 0914-4935

The packaging for IoT devices is transitioning from quad flat no-lead (QFN) packages to wafer-level chip scale packaging (WLCSP). This type of packaging has a high risk of incurring damage due to mishandling or carelessness that leads to their being dropped. To guarantee product quality, IoT devices must be certified with the board-level drop test before hitting the market. WLCSP is one kind of package technology used for an integrated circuit at the wafer-level. It follows the traditional process of assembling individual units in packages after cutting them from a wafer and then placing the solder bumps directly on the chip to yield a complete package. The package scale has been greatly reduced to comply with the use requirements of IoT products. Also, new types of failures arising in the fabrication and assembly process can occur. Consequently, fault location (FL), reliability tests or failure analysis (FA) tasks for the identification of defects in integrated circuits (ICs) have become more complicated for IoT applications.

The major types of faults possible in multilayered integrated circuit packaging may be caused by electrical short circuits, solder bump cracks, highly resistive openings, or other kinds of internal faults,[3,4] and X-ray methods can be a very useful tool for FA. Lock-in thermography has been developed by incorporating either sensing algorithms or the use of simulation methods.[5–7] Lock-in thermography (LIT) can reveal the effective spatial and temperature resolutions that need to be improved due to its dynamic and averaging nature. Therefore, it facilitates the detection of exothermic faults by providing the location of the faults in packaging interconnections.[8]

The drop impact in the board-level reliability test is used to evaluate the performance of surface-mounted electronic components in an accelerated test environment. The high strain rate of printed circuit boards with packages may cause failure in either the package or interconnections.[9] The board-level reliability (BLR) drop test is a destructive test, and the method is most relevant between the printed circuit board (PCB) and the package through a path consisting of a daisy chain structure.[10,11] Any defect must be found after the drop test for evidence of failure. However, it is difficult for the FA to detect faults using a resistance measurement in the case of wafer-level packaging.

The experiments conducted in this study provided an approach to the localization of a thermally active defect using the LIT results of a nondestructive method after the BLR drop test. LIT reveals inner electrical defects such as shorts or resistive openings using thermal imaging on the package surface.[12] In addition, a high-speed camera including a CCD sensor can be used to verify the bending behavior at the moment of the strike, lending support to prove the critical units are located at the center of the test board. This study provides a discussion of the application of LIT to the thermal imaging of resistive openings due to solder bump cracking (SBC) to obtain more accurately detection than is possible using alternative methods. The experimental results show that the employment of LIT enhances the resistive openings. The analysis method can also be extended to the shorts or leakage currents in thermally active failures.

2. Materials and Methods

2.1 LIT technique

LIT has been used extensively in nondestructive testing of the surfaces of solid objects. It is based on the application of a periodic input energy wave that is amplitude-modulated onto the surface of the object being examined and for analyzing the resulting surface temperature modulation on the surface of the test sample. The signal effect of LIT is the same as it would be if each pixel of the infrared (IR) image were to be connected with a two-phase lock-in amplifier. The captured signals are weighted using two different correlation functions (sin/−cos), resulting in a separation of the part of the thermal response that has no phase shift to the excitation signal ($S^{0°}$) and the part that is 90° phase shifted ($S^{90°}$). This so-called two-phase correlation process is done pixelwise and enables the calculation of both the amplitude and the phase signal of the thermal response.[13] The amplitude A and the phase Φ are calculated using Eqs. (1) and (2). The heating power is 50% of the duty cycle, which basically switches the device between two different voltage states. Pulsing a specific lock-in frequency to the device under test (DUT) and taking the thermal response at the DUT with a higher camera frequency are the basis for the on-line correlation process, as shown in Fig. 1.[14]

$$A = \sqrt{(S^{0°})^2 + (S^{90°})^2}, \tag{1}$$

$$\Phi = \arctan\left(\frac{S^{90°}}{S^{0°}}\right)\left(-180° \text{ if } S^{0°} \text{ is negative}\right), \tag{2}$$

where $S^{0°}$ is variable 1, and $S^{90°}$ is variable 2.[14]

IR is electromagnetic radiation with longer wavelengths than visible light that is emitted from the surface of every substance. LIT is one kind of sensor application. It used an indium-

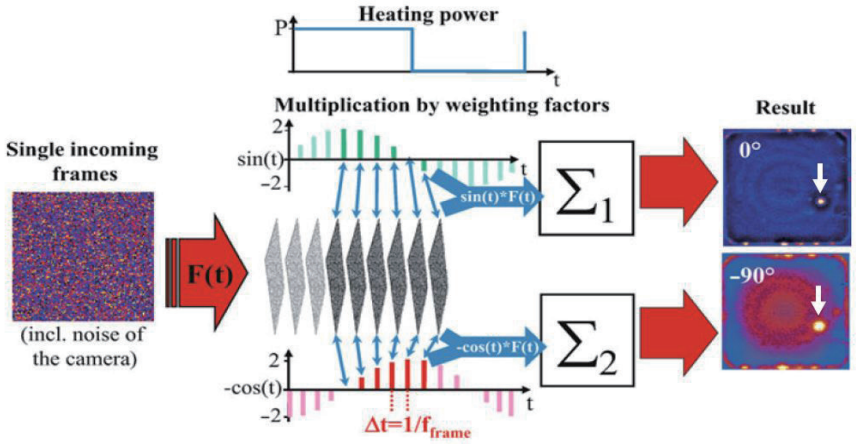


Fig. 1. (Color online) Schematic of the LIT on-line correlation process.[6]

antimonide as an IR sensor.[15,16] The chip dimension of this indium-antimonide (InSb) sensor is 9.6 × 7.7 mm^2, and it offers a maximum resolution of 640 × 512 pixels. LIT works on the fundamental principle of detecting heat produced by applying a pausing voltage to a defective point. LIT is also based on the principle of a thermal imaging sensor combined with noise reduction by applying a specific lock-in frequency that triggers the electrical signal driving the device being tested. A highly sensitive IR camera takes images of the device surface. In the results, the fault location with the highest resistance can be revealed by a hot spot on the specimen surface, as indicated by the white arrow in Fig. 2.

2.2 Experimental details

The PCB design and infrastructure were compliant with Nokia specifications.[17] There were 12 samples of daisy chain positions on one board, and nine pcs boards had to be tested. The load condition was a half-sine pulse with an amplitude of 1500 G and a pulse width of 1 ms. Both requests were +/−10%, and the process capability indexes (CPKs) were greater than 1.33. The typical drop test setup is shown in Fig. 3(a). Before the board-level drop test launches the calibration of the apparatus, the drop table must be released into freefall from the required height.

During the board-level reliability test, the electrical testers were applied for each daisy chain unit using real time monitoring. If the resistance reading was greater than 1000 Ω lasting 1 μs or longer,[17,18] this meant that a physical crack had formed somewhere and had occurred along the path of the daisy chain. The Nokia specification also suggests the critical units to be located at the PCB center. Therefore, units 5–8 must be considered for the Weibull analysis. These units are shown as a red square on the Nokia board in Fig. 3(a).

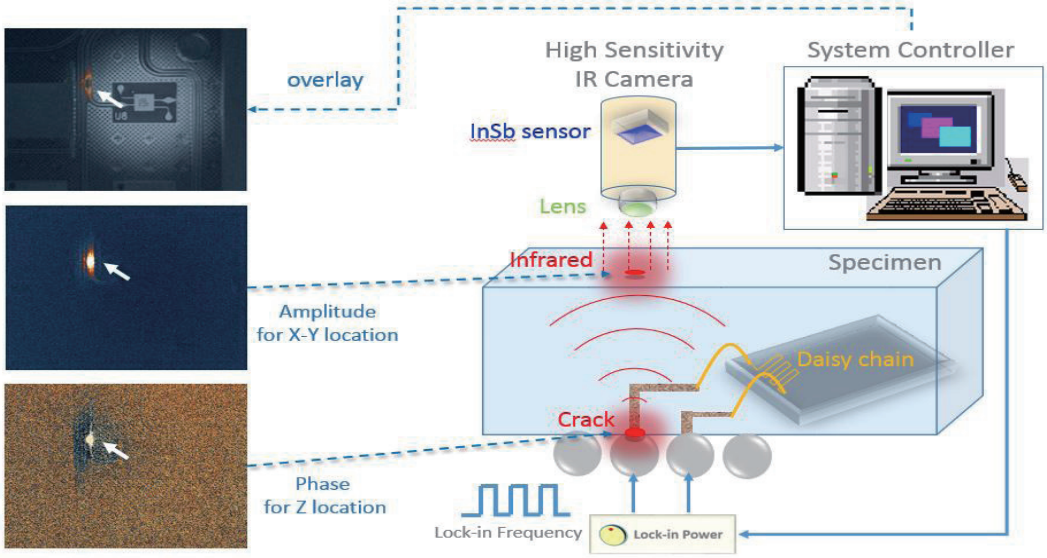
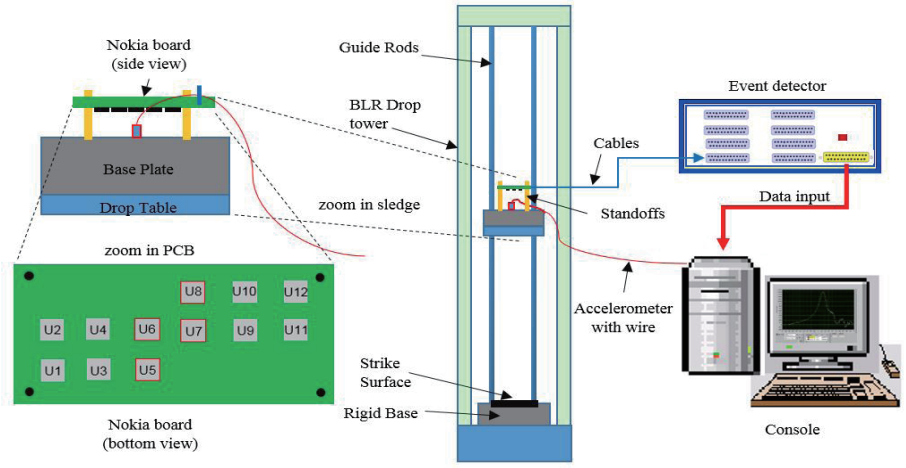


Fig. 2. (Color online) Experimental setup. The model is the DCG TDL640 IR camera applied in an InSb sensor.



(a)

(b)

Fig. 3. (Color online) (a) Typical setup of drop test equipment using the Nokia model board and (b) evaluation of dropping behavior using a high-speed camera.

After the experimental setup was ready, a high-speed camera was used to verify the behavior of the sample in slow motion at the moment of the strike. An Olympus i-SPEED TR is used, as shown in Fig. 3(b). Although it was difficult to find the fault location in the WLCSP package, it can be inferred that LIT is a good approach by which to achieve the target.

2.3 Experimental materials

In this work, the purpose was to use LIT to detect a fault location. We performed a controlled experiment to conduct the comparison. The test vehicle was a WLCSP49 package for an IoT product, and two different Sn–Ag–Cu (SAC) balls were selected for comparison owing to the fact that solder ball material is a key factor in the BLR drop test. Table 1 shows a detailed description of the specimen used in the SBC test. Lot 1 is the experimental lot, and Lot 2 is the control. Figure 4 provides a detailed package profile structure.

Table 1
Specimen description.

Lot No.	Solder bump	Package model	Bump pitch (μm)	UBM size (μm)	PCB pad size (μm)	Sample size	Critical units
Lot 1	SAC405	WLCSP49	350	200	200	Nine pcs	U5–U8
Lot 2	SAC405 + 3.5% Bi	WLCSP49	350	200	200	Nine pcs	U5–U8

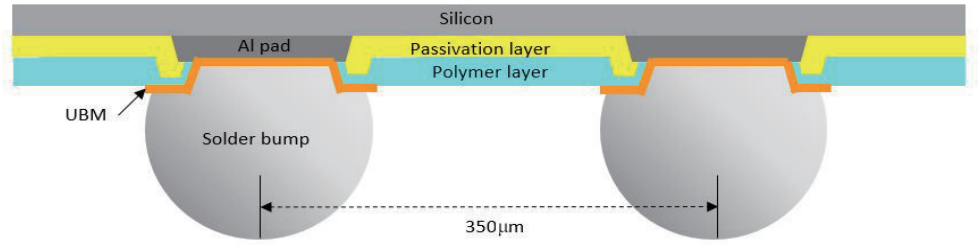


Fig. 4. (Color online) Construction of the WLCSP49 specimen.

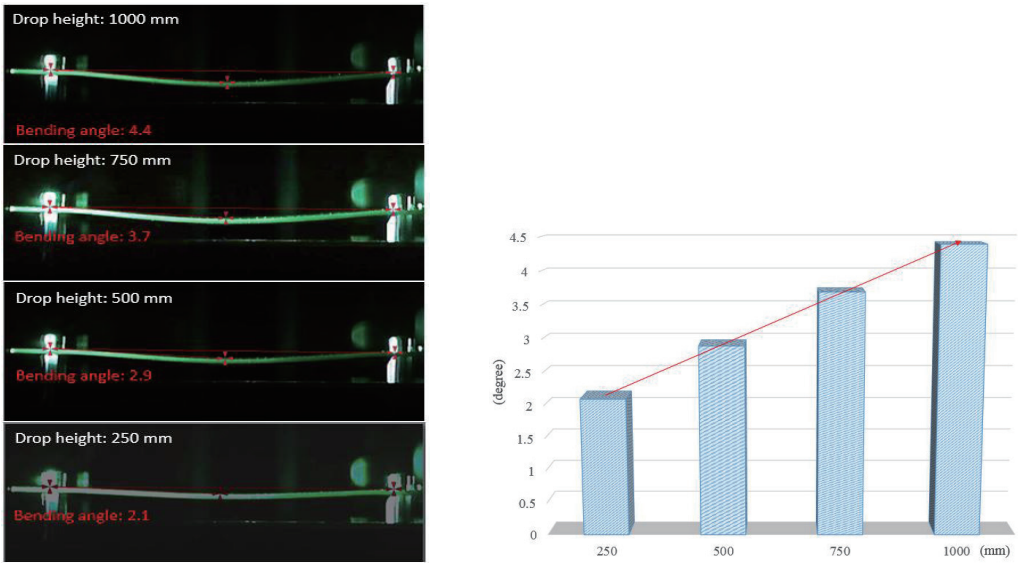
3. Experimental Results and Discussion

3.1 Response of the BLR drop test

The experiment was conducted under four different height conditions for the purpose of verification (250, 500, 750, and 1000 mm). The high-speed camera captured the PCB behavior, which was the maximum amplitude with the vibration bending angle at the moment of the strike, as shown in Fig. 5(a). It was clear that a greater height and centralized PCB units are very critical. On the other hand, the relationship between the drop height (250–1000 mm) and bending angle (2.1–4.4 deg) was linear, as shown in Fig. 5(b). The high-speed camera proved the critical units to be U5–U8 on the test board.

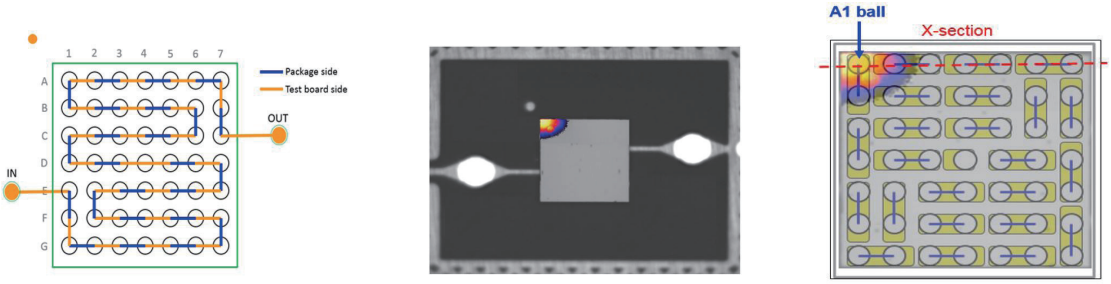
The daisy chain package in the SBC test was the WLCSP49 for IoT applications, the connection for which is shown in Fig. 6(a). The critical balls were at the package edges, and the corners were considered. Therefore, the daisy chain routing was around the boundary between the package and the PCB. Figure 7(a) shows the nine boards per lot used to perform this board-level drop test experiment, where 1000 drops were tested so as to obtain sufficient fails for the Weibull analysis. The β of Lot 1 was 6.49, and that of Lot 2 was 4.57, which means that the failures were under the wear-out region because β was greater than 1. In addition, the normal distribution of the probability density function is shown in Fig. 7(b). In other words, the defect mode should be uniform as per the statistical analysis.

In this Weibull analysis, the stop point was 1000 drops. Table 2 shows a summary of the test results. The SAC405 is better than the SAC405 + 3.5% Bi in terms of the BLR drop test lifetime. The B3U8 sample (board 3, unit 8) for Lot 1 and B9U8 sample (board 9, unit 8) failed at 63.2%. We selected both of them as the test vehicles for the LIT analysis[19] because they are representative of a real-world situation. Photos of the real samples reveal the topography in the LIT.



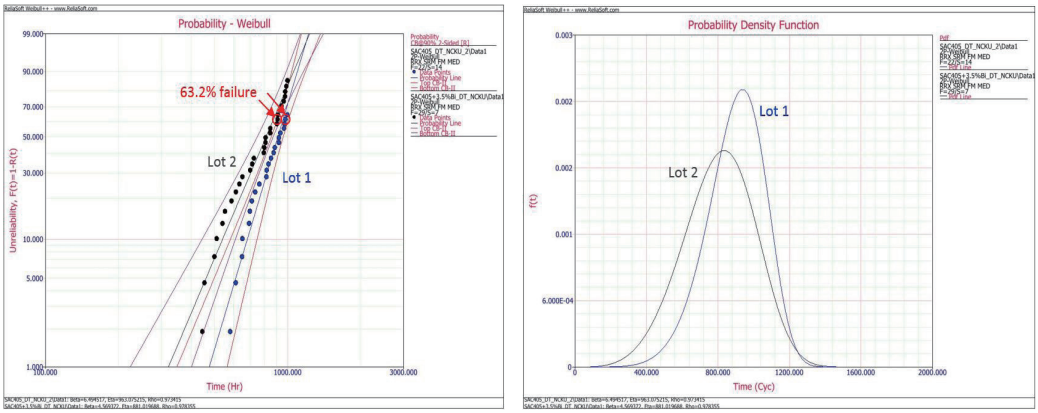
(a) (b)

Fig. 5. (Color online) (a) Capture of the maximum amplitude using the high-speed camera and (b) comparison between the drop height and the bending angle.



(a) (b) (c)

Fig. 6. (Color online) Lot 1, WLCSP49 SAC405. (a) Daisy chain design between PCB and WLCSP49. (b) The hot spot is the solder bump at the upper left corner of B3U8 using LIT. (c) Combination of the daisy chain, ball assignment, and the LIT image.



(a) (b)

Fig. 7. (Color online) Drop test analysis using the (a) Weibull plots and (b) probability density function of all failures.

Table 2
Results of the BLR drop tests.

Lot No.	β	1st failure	50% failure	63.2% failure	Last failure	Test vehicle
Lot 1	6.49	580 drops	921 drops	979 drops	998 drops	B3U8
Lot 2	4.57	445 drops	812 drops	909 drops	999 drops	B9U8

3.2 Response for the BLR drop test

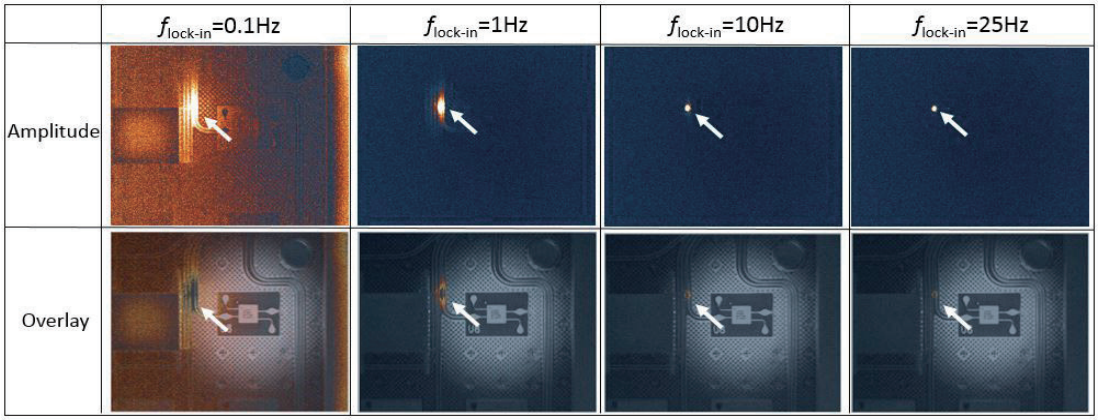
In the evaluation of LIT characteristics,[20] the test vehicle was a BLR sample that is damaged at the trace line with a resistive opening. The reading for the resistive opening was 75 kΩ based on a multimeter confirmation. The resistance was constant to provide a solid vehicle for the various subsequent evaluations. The SBC sample was not considered appropriate for these evaluations because the resistance varies.

Figure 8(a) shows the amplitude and overlay images for the influence of the lock-in frequency. Measured at 0.1, 1, 10, and 25 Hz lock-in frequencies differed by the same power dissipation of 330 μW and a reaction time of one min. In this study, LIT characteristics with amplitude and overlay showed higher accuracy dependence on the frequency for determining the area of the fault location. On the other hand, measured at 1, 10, 100, and 1000 μW, the power dissipation differed by the same frequencies (1 Hz). The power dissipation and reaction time had higher accuracy than was the case with lower power dissipation, as shown in Fig. 8(b). In summary, the LIT signals were compared and were found to be in good agreement with the experimental signal obtained using 3D defect localization.[7]

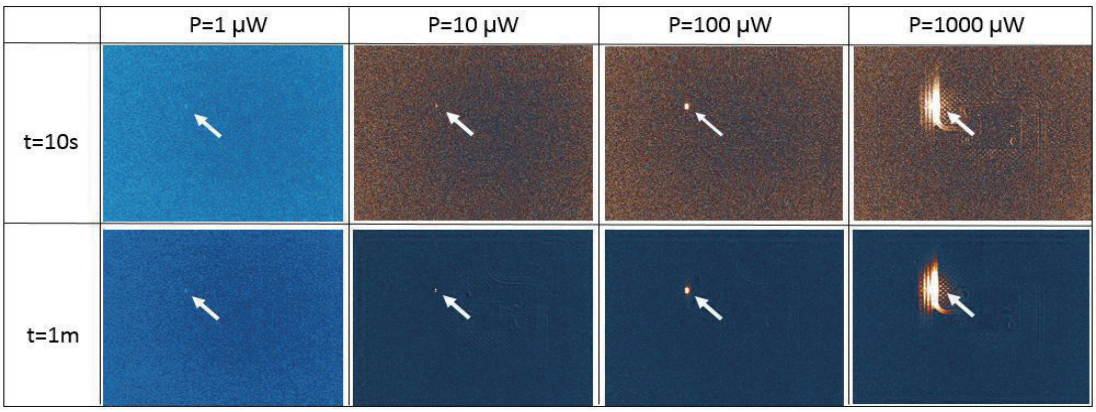
3.3 SBC using sensor applications

The failed samples could be sorted out on a timely basis during the drop test for this LIT application. After the drop test, all samples were verified again with a multimeter resistance measurement. The selected samples showed higher resistance between the in and out test pads. The route of the daisy chain was between the board and the WLCSP49 package. The blue lines are on the package side, and the brown ones are on the test board side, as shown in Figs. 6(a) and 9(a), respectively. It is very difficult to reflect certain highly resistive openings using an off-line measurement because of the strike moment in the drop test with critical bending. Even so, a slight amount of resistance can provide adequate conditions for an LIT analysis.

After the creation of the local resistance area, a single WLCSP49 daisy chain chip was measured using LIT with a supply voltage of 0.75 V and a lock-in frequency of 1 Hz, creating a local heat source with a power dissipation of 15 mW. Figures 6(b) and 9(b) show the overlay image as a combination of both amplitude and the topography pattern. The arrow shows the defect-related thermal emission, which clearly indicates that the fault location is at the corner of the devices.[21–25] The overlay image is combined with a daisy chain drawing on a chip, as shown in Figs. 6(c) and 9(c). The defect position is determined precisely. It is certain that the upper left solder ball A1 of B3U8 and the lower right solder ball G7 of B9U8 form a completed crack in the cross section. Figures 10 and 11 clearly show similar completed cracks in the

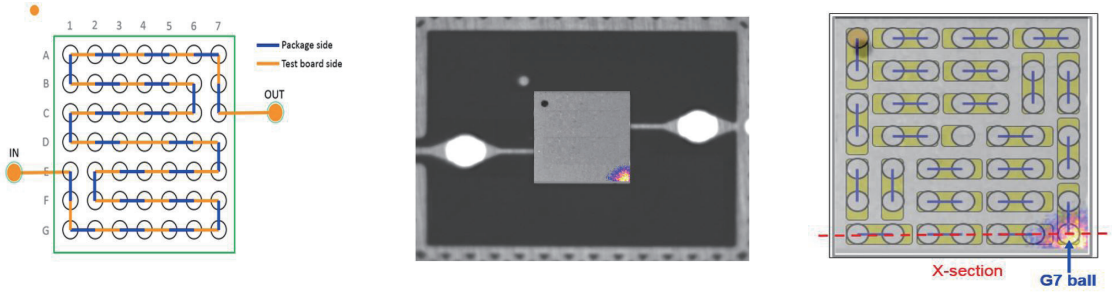


(a)



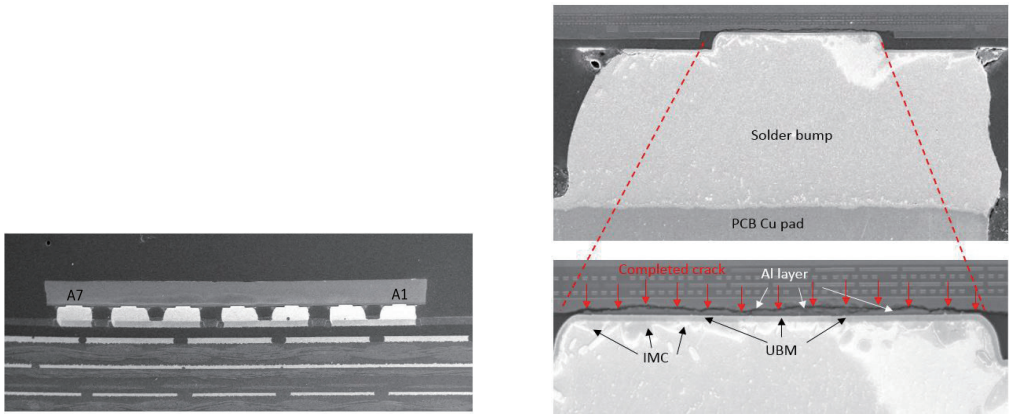
(b)

Fig. 8. (Color online) Evaluation of LIT characteristics for the hot spot. (a) LIT signals detected at lock-in frequencies of 0.1, 1, 10, and 25 Hz. (b) LIT power dissipation and reaction time evaluated at the power of one, 10, 100, and 1000 μW.



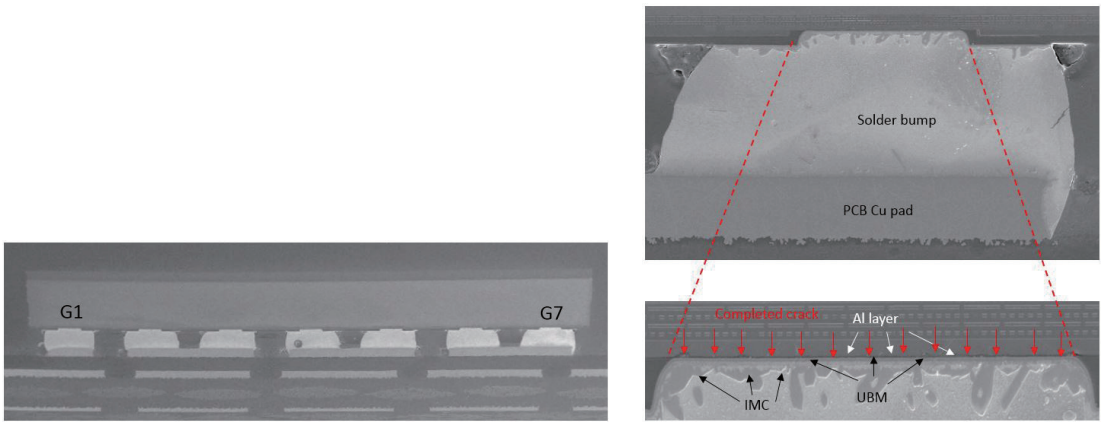
(a) (b) (c)

Fig. 9. (Color online) Lot 2, WLCSP49 SAC405 + 3.5% Bi. (a) Daisy chain design between PCB and WLCSP49. (b) The hot spot is the solder bump at the lower right corner of B9U8 using LIT. (c) Combination of the daisy chain, ball assignment, and the LIT image.



(a) (b)

Fig. 10. (Color online) Lot 1, SAC405. SEM inspection after cross section: (a) the side view of the package, and (b) the completed crack in the aluminum layer of the A1 ball, where the cracked area is shown using red arrows.



(a) (b)

Fig. 11. (Color online) Lot 2, SAC405 + 3.5% Bi. SEM inspection after cross section: (a) the side view of package, and (b) the completed crack in the aluminum layer of the G7 ball, where the cracked area is shown using red arrows.

aluminum layer of the two solder balls using SEM. This indicates that the LIT exhibited good performance for both the experimental and control lots.

4. Conclusions

In this study, (1) LIT was used to detect the IR emission through an InSb sensor. The LIT characteristics were determined according to different factors (e.g., lock-in frequency, power dissipation, and reaction time). (2) The BLR drop test behavior was verified using a high-speed camera. The critical units on the test board were at the center, and the relationship between the drop height and bending angle was linear. (3) The sample test was found to be better than SAC405 + 3.5% Bi in the lifetime of the BLR drop test. After the board-level reliability

evaluation drop test, it is always necessary to detect the fault location before the destructive analysis of a cross section. (4) The sensor LIT measurement application can detect the fault location efficiently and precisely for IoT products. In this study, solder bump cracks were analyzed based on LIT. Complex 3D cracks in an IoT application will be evaluated in future work.

Acknowledgments

This work was supported by the Department of Electrical Engineering of National Cheng Kung University, Republic of Taiwan.

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