Sensors and Materials, Vol. 30, No. 4 (2018) 683–691
MYU Tokyo

30th Commemorative Article

S & M 1530

Wafer-level Packaging, Equipment Made in House, and Heterogeneous Integration

Masayoshi Esashi*

Micro System Integration Center, Tohoku University,
519-1176 Aramaki-Aza-Aoba, Aoba-ku, Sendai 980-0845, Japan

(Received May 18, 2017; accepted June 15, 2017)

Keywords: wafer-level packaging, heterogeneous integration, ion-sensitive FET, deep RIE, massive parallel electron beam write system

Micro-electromechanical systems (MEMS) have been developed for sensors and other systems since 1971 at Tohoku University. Ion-sensitive FET (ISFET) probes made by micromachining were commercialized for pH and PCO_2 catheters. Special attention was paid to packaging and wafer-level packaging based on glass-to-Si anodic bonding was applied for integrated capacitive pressure sensors, capacitive diaphragm vacuum gauges, MEMS switches, and other devices. Process equipment for not only MEMS but also integrated circuits (ICs) has been made in house because it is important for flexible prototyping and fabrication of novel devices. Equipment for deep reactive ion etching (RIE) of Si was developed and applied for an electrostatically levitated rotational gyroscope and other devices. Heterogeneous integration as MEMS on LSI has been made possible by the transfer of MEMS on a carrier wafer to an LSI wafer or by stacking a MEMS wafer on an LSI wafer using electrical interconnection with a through Si via (TSV). A piezoelectric MEMS switch on an LSI chip, surface acoustic wave (SAW) filters on an LSI chip, a tactile sensor network, and an active matrix electron emitter array are shown as examples of these technologies.

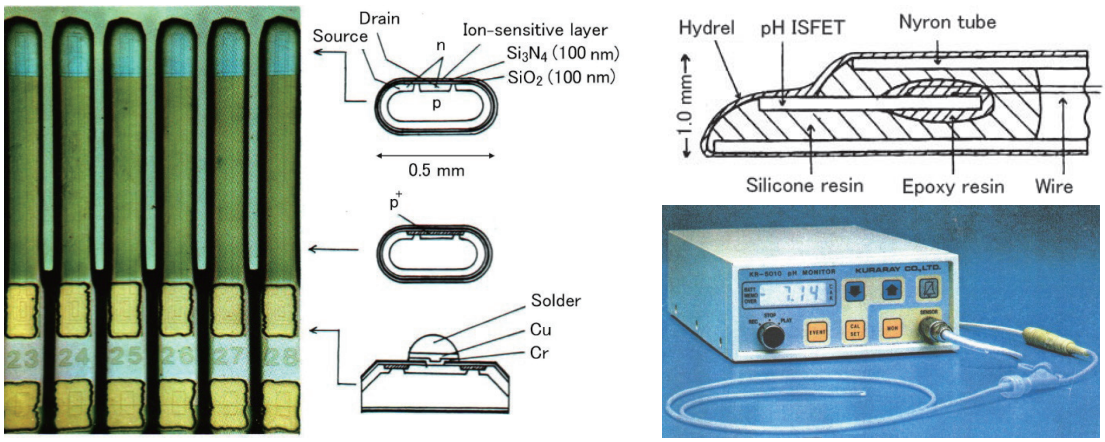
1. Introduction

The ion-sensitive FET (ISFET) has been studied since 1971. It has a structure like a MOS FET but its gate insulator is exposed to an electrolyte and can be used as an ion sensor. The probelike ISFET shown in Fig. 1(a) was fabricated for reliable assembly of a catheter pH sensor, shown in Fig. 1(b).[1] This was commercialized as a pH and PCO_2 sensor[2] in 1983 and used for pH measurement in the esophagus and stomach.

A process facility described in Sect. 3 for making 20 × 20 mm^2 wafers was used for fabricating the ISFET. Equipment made in house was used in the process facility. This facility is like a toy but is very effective even for beginners to gain experience in each process step and to fabricate sensors, because of its flexibility. The facility was used to make CMOS integrated circuits (ICs) as well in the 1980s and has been utilized up to now.

*Corresponding author: e-mail: esashi@mems.mech.tohoku.ac.jp
http://dx.doi.org/10.18494/SAM.2018.1638

ISSN 0914-4935
http://myukk.org/



(a) (b)

Fig. 1. (Color online) ISFET: (a) probelike ISFET and (b) catheter pH sensor.

Reliability and cost depend on the assembly and packaging. Wafer-level packaging explained in Sect. 2 was developed and applied for MEMS products.

Heterogeneous integration such as MEMS on LSI is important to enable advanced systems. Wafer-level transfer or chip-level selective transfer of MEMS on a carrier wafer to an LSI wafer was developed. MEMS and LSI wafers stacked and interconnected with a through Si via (TSV) were also developed. Examples of applications of these methods will be shown in Sect. 4.

2. Wafer-level Packaging

Figure 2 shows the fabrication process and a photograph of an integrated capacitive pressure sensor.[3] A CMOS IC to detect a small capacitance change upon applying pressure was made on the sensor chip using the 20 mm process facility. The Si wafer is anodically bonded to a glass wafer. Packaged chips are obtained by dicing the wafer after making thin diaphragms. This wafer-level packaging can reduce the size and cost because no extra packaging will be required.[4] The pressure sensor was commercialized by Toyoda Machine Works Ltd. for low-pressure measurement. Technologies to protect the circuits during the anodic bonding (400 °C, −500 V to glass wafer) were developed for this fabrication.

The wafer-level packaging was applied to MEMS switches, as shown in Fig. 3.[5] The switch is thermally actuated with a current by using different thermal expansion. The contact surface of the switch could be kept clean because of the wafer-level packaging. The switch was produced to be used in LSI testers by Advantest Corp.[6] One advantage of the MEMS switch is that it is immune to electrostatic discharge.

Figure 4 shows a capacitive diaphragm vacuum gauge. This has a thin diaphragm and a high-vacuum cavity in it. A small differential pressure between the two sides of the diaphragm is capacitively detected. A high-vacuum cavity can be realized by placing a nonevaporable getter (NEG) in the cavity.[7] The getter absorbs oxygen gas generated during anodic bonding by decomposition of the glass at the interface. The vacuum gauge was commercialized by Anelva Corp.[8]

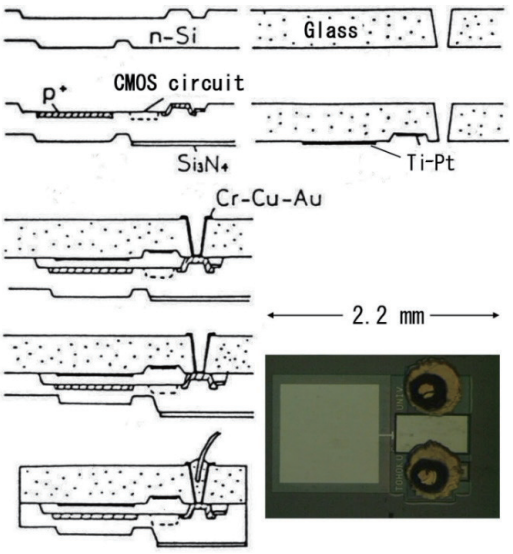


Fig. 2. (Color online) Integrated capacitive pressure sensor.

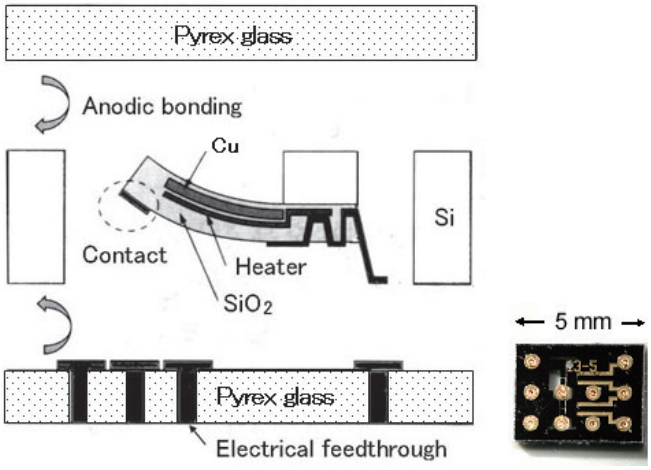


Fig. 3. (Color online) MEMS switch for LSI tester.

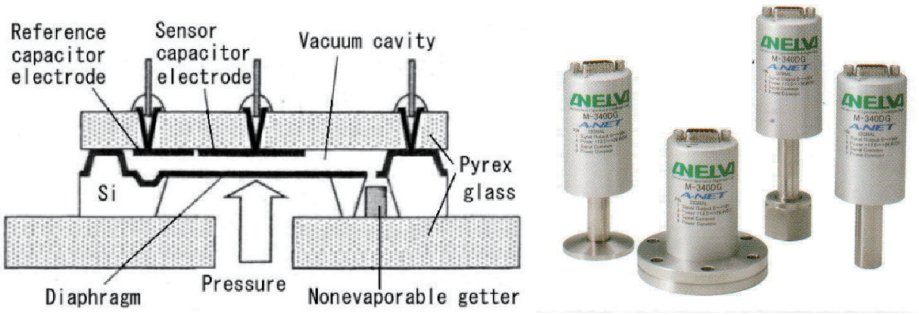


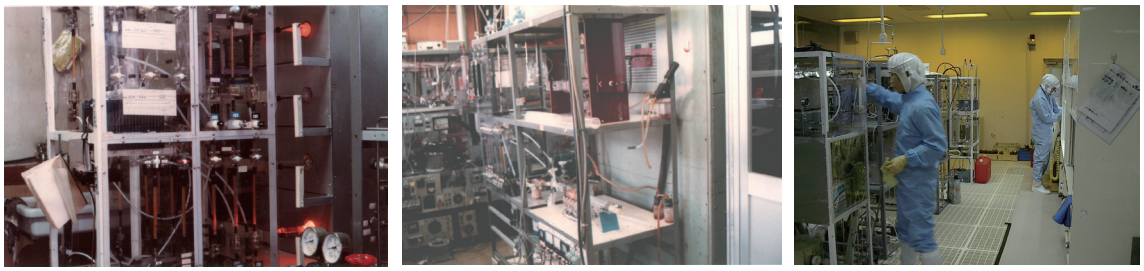
Fig. 4. (Color online) Capacitive diaphragm vacuum gauge using NEG in a vacuum cavity.

3. Equipment Made in House

It is advantageous to make process equipment in house. Figure 5 shows our process facility for 20 × 20 mm^2 wafers. Figure 5(a) shows an oxidation/diffusion furnace used for ISFET fabrication in 1975. This was extended to the facility for CMOS ICs, as shown in Fig. 5(b).[9] The facility has been used until now, as shown in Fig. 5(c). The facility has been shared by many laboratories and companies, facilitating fusion research and providing an ecosystem for commercialization. Great effort is needed for common use of the facility, but the resultant accumulated know-how is worthwhile.

An example of the equipment made in house is that used for the deep reactive ion etching (RIE) of Si. Figure 6 shows a low temperature deep RIE system[10] and a Si wafer etched through for use in a resonating gyroscope.[11] The deep RIE was presented in 1992, which was 4 years ahead of the commercial Si deep RIE.

The Si deep RIE developed in house played important roles in the fabrication of the MEMS gyroscopes, as follows. The electrostatically levitated rotational gyroscopes shown in Figs. 7



(a) (b) (c)

Fig. 5. (Color online) Process facility made in house for 20 mm wafer, (a) oxidation/diffusion furnace for ISFET fabrication in 1975, (b) facility for CMOS IC in 1985, and (c) facility for heterogeneous integration in 2010.

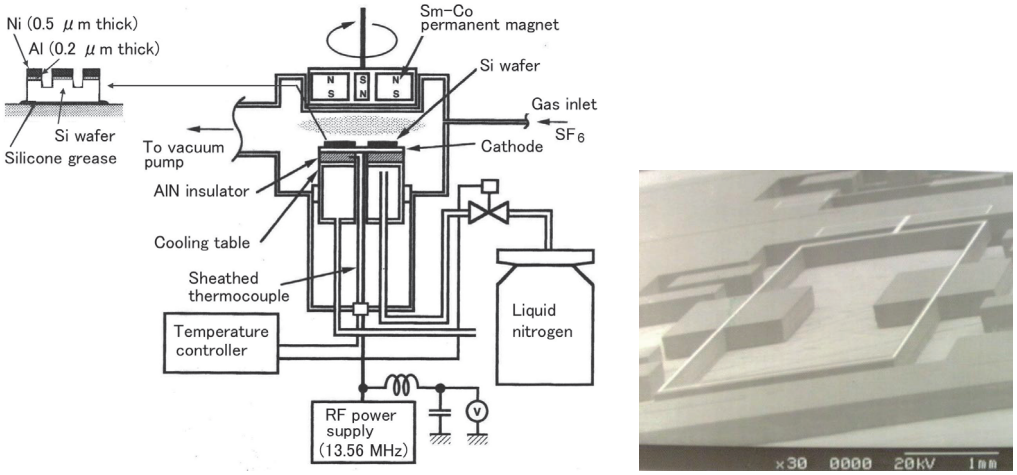


Fig. 6. (Color online) Low-temperature deep RIE equipment and Si wafer etched through for use in resonating gyroscope.

and 8 were developed to detect two-axis rotation and three-axis acceleration simultaneously with high precision. Figure 7 shows a disk-rotor gyroscope in which a Si disk is electrostatically levitated by capacitive position sensing and electrostatic actuation in all directions.[12] The wafer-level packaging was applied using the non-evaporable getter (NEG) in the cavity. This is needed to hold the vacuum cavity for high speed rotation of the disk.

Figure 8(a) shows the structure and photograph of the improved rotational gyroscope.[13] A ring rotor with 1.5 mm diameter is used to increase the lateral electrostatic force. It is levitated electrostatically by high-speed digital signal processing and it rotates at 74000 rpm. The ring-rotor gyroscope is not made with wafer-level packaging; it needs a conventional metal vacuum package. The gyroscope, as shown in Fig. 8(b), was commercialized by Tokyo Keiki Inc. and has been used as a motion logger for the subway in Tokyo.

4. Heterogeneous Integration

The heterogeneous integration of MEMS on LSI has been achieved by stacking MEMS on LSI.[14] This enables advanced microsystems. It is important not to damage the LSI. One

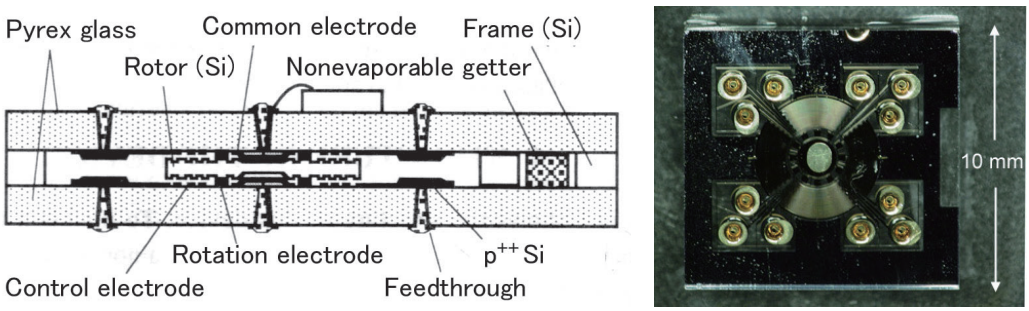


Fig. 7. (Color online) Electrostatically levitated rotational gyroscope (disk-rotor type) made by Si deep RIE and wafer-level packaging with a vacuum cavity.

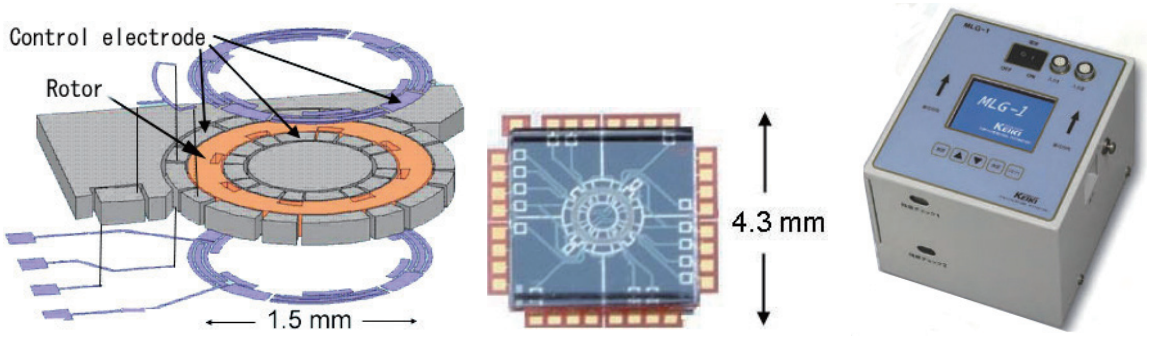
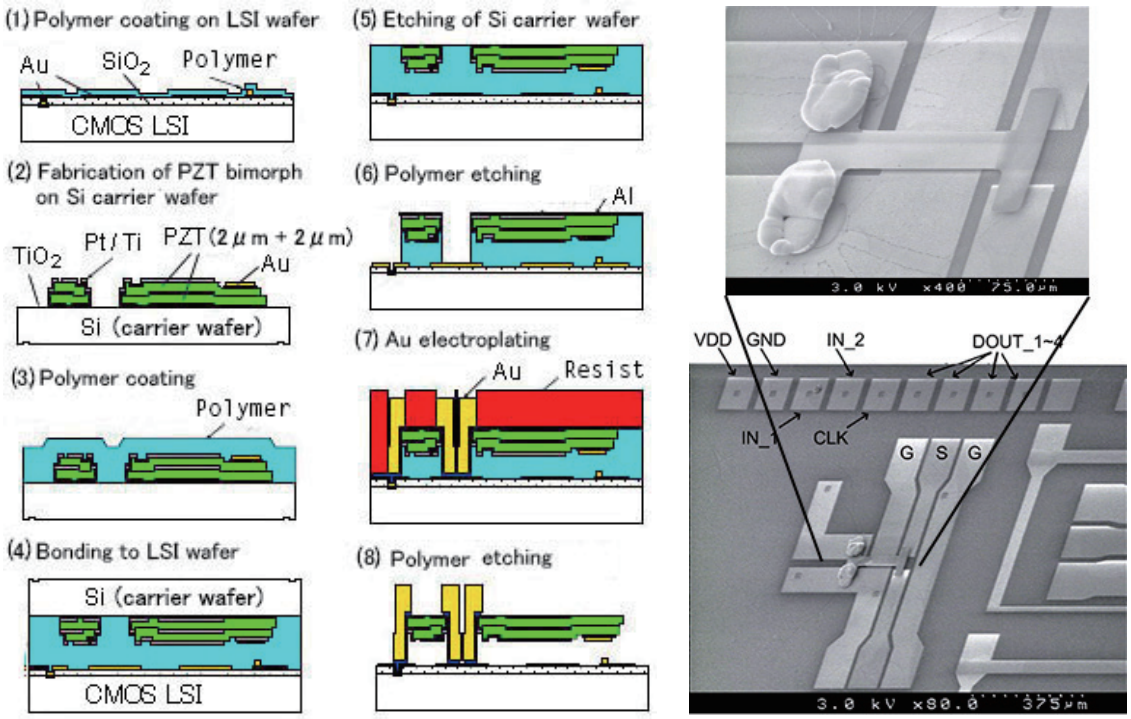


Fig. 8. (Color online) Electrostatically levitated rotational gyroscope (ring-rotor type); (a) structure and photograph and (b) motion logger using the rotational gyroscope.

method is to transfer the MEMS fabricated on a carrier wafer to an LSI wafer. This method is categorized as wafer-level transfer, explained below (Sect. 4.1), and chip-level selective transfer (Sect. 4.2). The other method is to stack a MEMS wafer and an LSI wafer. Electrical connection is made using a TSV formed in the MEMS wafer (Sect. 4.3) or the LSI wafer (Sect. 4.4).

4.1 Wafer-level transfer of MEMS on a carrier wafer to an LSI wafer

MEMS switches made of a piezoelectric bimorph were transferred to an LSI.[15] The fabrication process and a photograph are shown in Figs. 9(a) and 9(b). Lead zirconate titanate [$Pb(Zr,Ti)O_3$, PZT] made by the sol-gel method was used as the piezoelectric material. PZT requires high-temperature (750 °C) annealing, and for this reason, MEMS must be fabricated on a carrier wafer so as not to damage the LSI. The wafer-level transfer was used to fabricate a boron-doped diamond electrode array (20 × 20) on an LSI for amperometric measurement.[16] The diamond requires a high temperature (800 °C) for its deposition, and for this reason, the wafer-level transfer process is needed.



(a) (b)

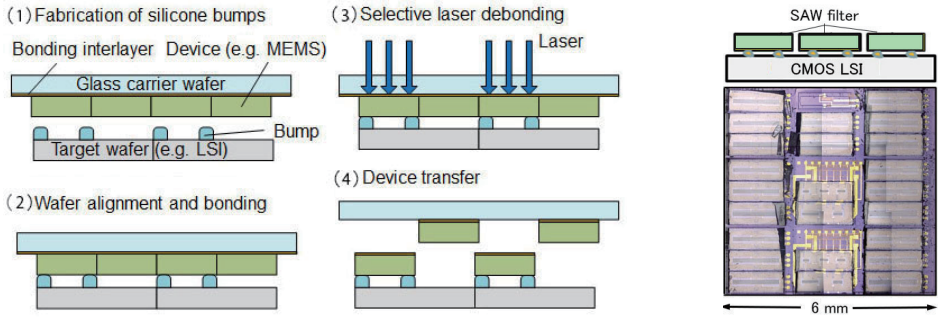
Fig. 9. (Color online) PZT MEMS switch on LSI; (a) fabrication process and (b) photograph.

4.2 Chip-level selective transfer of MEMS on a carrier wafer to an LSI wafer

Multiple SAW filters were formed on an LSI chip by a selective transfer process.[17] The process and the multiple SAW filters on the LSI are shown in Figs. 10(a) and 10(b). The SAW filters fabricated on a $LiNbO_3$ wafer are bonded to a glass carrier wafer using a photoresist and diced. After Au–Au bonding using bumps, selective laser debonding is accomplished by carbonizing the resist. SAW filters with different resonant frequencies are transferred to the same LSI wafer and residual SAW filters on the glass carrier wafer are transferred to another LSI wafer. Tunable bandwidth SAW filters were fabricated by bonding variable capacitors to a $LiNbO_3$ wafer via selective transfer.[18] The variable capacitors are ferroelectric capacitors made of barium strontium titanate [$Ba(SrTi)O_3$, BST], the capacitance of which can be controlled by applied voltage.

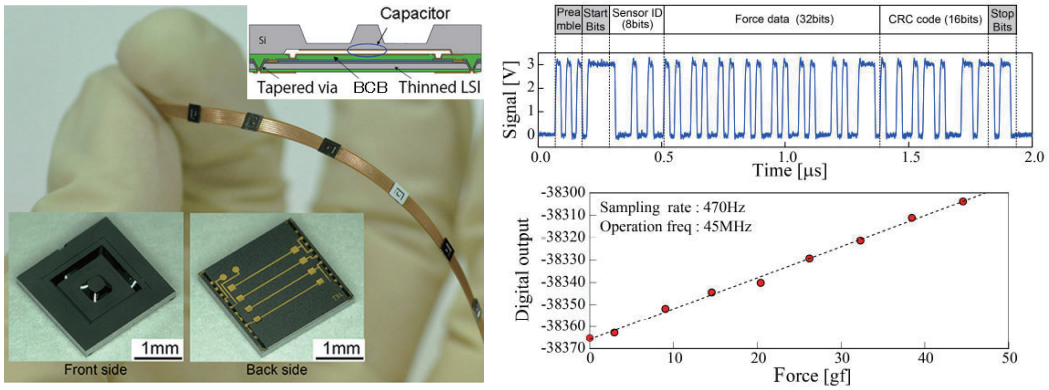
4.3 Stacked MEMS wafer and LSI wafer with TSV in LSI wafer

Distributed tactile sensors (tactile sensor network) are required on the skin of nursing care robots to ensure collision safety. The structure and a photograph are shown in Fig. 11(a).[19] Each tactile sensor is capable of packet communication, as shown in Fig. 11(b). MEMS wafers for capacitive force sensing are bonded on an LSI wafer, which has a TSV. Diced chips are connected to a flexible cable with a common bus and power supply.



(a) (b)

Fig. 10. (Color online) (a) Selective transfer process with laser debonding and (b) multiple SAW filters on LSI formed by the selective transfer process.



(a) (b)

Fig. 11. (Color online) Tactile sensor network; (a) structure and photograph and (b) packet signal for asynchronous communication using common bus.

4.4 Stacked MEMS wafer and LSI wafer with TSV in MEMS wafer

Digital fabrication of an LSI by maskless lithography is expected for cost-effective small-volume production and efficient development. Massive parallel electron beam (EB) write (MPEBW) systems, which have a 100 × 100 active matrix electron emitter array, are under development.[20] The electron emitter is made of nanocrystalline Si (nc-Si). The nc-Si is formed by anodizing Si in HF solution followed by electrochemical oxidation. The nc-Si consists of cascaded tunnel junctions. Accelerated ballistic electrons are emitted through a thin (10-nm-thick) Au layer at a low voltage (10 V). The structure of the active matrix electron emitter and photographs of the cross section of the nc-Si emitter and the driver LSI are shown in Fig. 12(a). The nc-Si emitter wafer is stacked on an LSI wafer and has a TSV for electrical interconnection to the LSI. Figures 12(b) and 12(c) show a photograph of a prototype and the structure of the MPEBW system, respectively. The prototype is constructed laterally to facilitate modification.

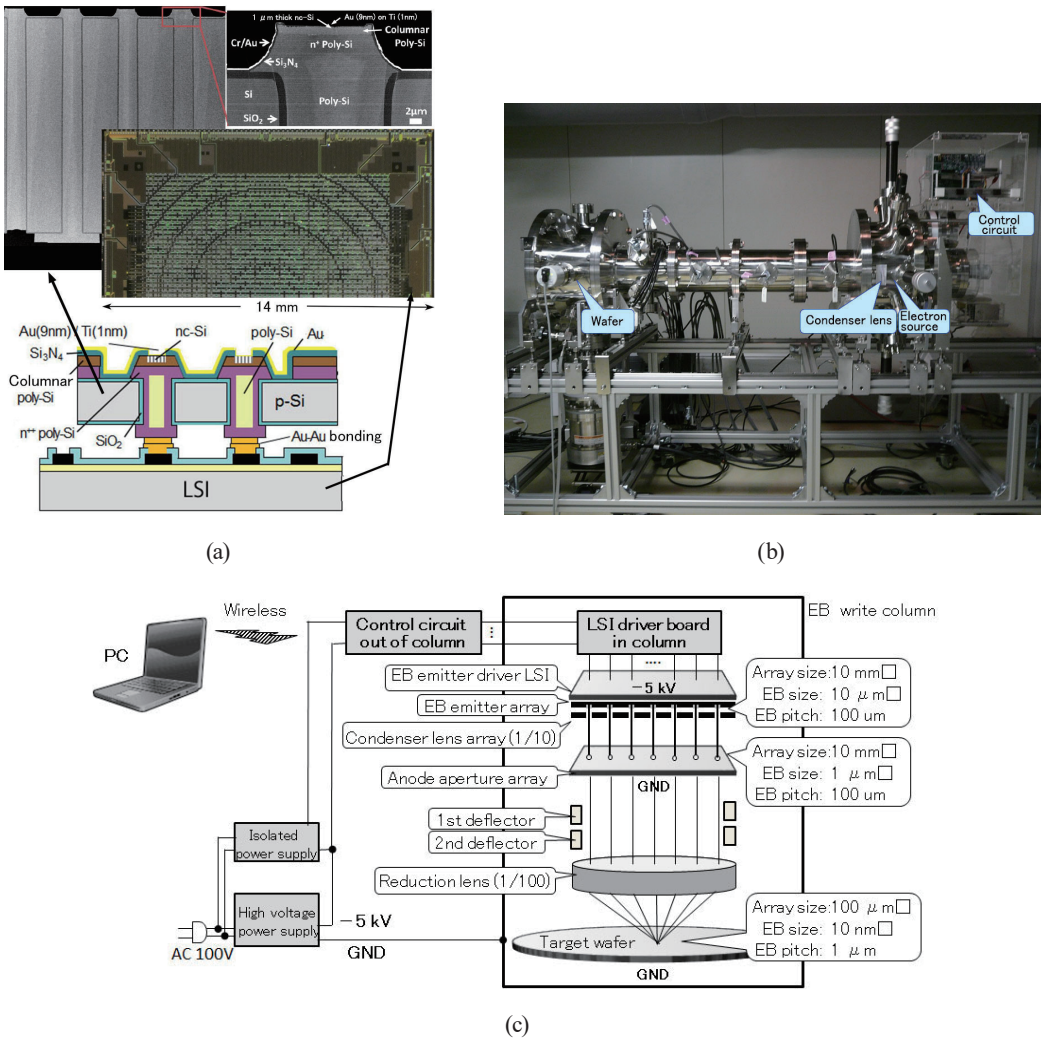


Fig. 12. (Color online) Massive parallel EB write system; (a) active matrix nc-Si electron source, (b) photograph of the prototype, and (c) MPEBW structure.

5. Conclusions

Our MEMS activities were initiated for the development of ISFETs 46 years ago in 1971. The process facility for 20 mm wafers was made in house and has been used up to now. The facility was used for fabricating CMOS ICs until 1992. Wafer-level packaging by anodic bonding was applied to various MEMS for commercialization. Taking advantage of the high degree of integration of LSI, advanced microsystems can be expected by applying heterogeneous integration. The LSI used are currently made in a foundry, but we have been reducing the manufacturing cost by sharing the wafer with 16 noncompetitive companies.

References

1 M. Esashi and T. Matsuo: Jpn. J. Appl. Phys. **44** Supplement (1975) 339.
2 K. Shimada, M. Yano, K. Shibatani, Y. Komoto, M. Esashi, and T. Matsuo: Med. Biol. Eng. Comput. **18** (1980) 741.
3 Y. Matsumoto and M. Esashi: Electron. Commun. Jpn. **76** (1992) 93.
4 M. Esashi: J. Micromech. Microeng. **18** (2008) 073001.
5 L. X. Liu, M. Nishio, and M. Esashi: 2000 Technical Digest of the 17th Sensor Symp. (IEEJ, 2000) 33.
6 K. Nakamura, F. Takayanagi, Y. Moro, H. Sanpei, and M. Onozawa: Advantest Tech. Rep. **22** (2004) 9 (in Japanese).
7 H. Henmi, S. Shoji, Y. Shoji, K. Yoshimi, and M. Esashi: Sens. Actuators, A **43** (1994) 243.
8 H. Miyashita and Y. Kitamura: ANELVA Tech. Rep. **11** (2005) 37 (in Japanese).
9 H. Seo, M. Esashi, and T. Matsuo: Frontiers Med. Biol. Eng. **1** (1989) 319.
10 M. Takinami, K. Minami, and M. Esashi: 1992 Technical Digest of the 11th Sensor Symp. (IEEJ, 1992) 15.
11 J. Choi, K. Minami, and M. Esashi: High Aspect Ratio Microstructure Technology (HARMST'95) (Forschungszentrum Karlruhe, 1995).
12 T. Murakoshi, K. Minami, and M. Esashi: 1996 Technical Digest of the 14th Sensor Symp. (IEEJ, 1996) 47.
13 T. Murakoshi, Y. Endo, K. Fukatsu, S. Nakamura, and M. Esashi: Jpn. J. Appl. Phys. **42** (2003) 2468.
14 M. Esashi and S. Tanaka: Micromachines **7** (2016) 137.
15 K. Matsuo, M. Moriyama, M. Esashi, and S. Tanaka: Technical Digest IEEE MEMS 2012 (IEEE, 2012) 1153.
16 K. Y. Inoue, M. Matsudaira, M. Nakano, K. Ino, C. Sakamoto, Y. Kanno, R. Kubo, R. Kunikata, A. Kira, A. Suda, R. Tsurumi, T. Shioya, S. Yoshida, M. Muroyama, T. Ishikawa, H. Shiku, S. Satoh, M. Esashi, and T. Matsue: Lab Chip **15** (2015) 848.
17 S. Tanaka, M. Yoshida, H. Hirano, and M. Esashi: 2012 IEEE Int. Ultrasonics Symp. (IEEE, 2012) 1047.
18 H. Hirano, T. Kimura, I. P. Koutsaroff, M. Kodato, K. Hashimoto, M. Esashi, and S. Tanaka: J. Micromech. Microeng. **23** (2013) 025005.
19 M. Makihata, S. Tanaka, M. Muroyama, S. Matsuzaki, H. Yamada, T. Nakayama, U. Yamaguchi, K. Mima, Y. Nonomura, M. Fujiyoshi, and M. Esashi: Sens. Actuators, A **188** (2012) 103.
20 M. Esashi, A. Kojima, N. Ikegami, H. Miyaguchi, and N. Koshida: Microsyst. Nanoeng. **1** (2015) 15029.