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Properties of 2×64 Linear HgCdTe Molecular Beam-Epitaxy-Grown Long Wavelength Infrared Arrays with Charged Coupled Devices Silicon Readouts

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Mercury cadmium telluride (MCT) 2×64 linear arrays for long-wavelength infrared (LWIR) applications with large area diodes and charged coupled devices (CCD) silicon readouts were designed, manufactured and tested. The HgCdTe layers were grown by molecular beam epitaxy (MBE) technology on (103) GaAs substrates with CdZnTe buffer layers and have a cutoff wavelength $\lambda_{co}\approx 10.0$–12.2 μm. To decrease the surface influence of the recombination processes of the carriers, layers with a graded composition increasing toward the surface of composition $Hg_{a-x}Cd_xTe$ were grown. Silicon readouts with CCD multiplexers with input direct injection circuits were designed, manufactured and tested. The testing procedure to qualify Read Out Integration Circuits (ROICs) on the wafer level at T=300 K was established. The silicon readouts for 2×64 arrays, with skimming and partitioning functions (because of large square diodes) included, were manufactured by *n*-channel MOS technology with buried or surface channel CCD registers. Designed CCD readouts are driven with four- or two-phase clock pulses. The HgCdTe arrays and Si CCD readouts were hybridized by cold welding In bumps technology. The parameters of the hybrid arrays measured have shown a 100% yield after the hybridization process. Even with a skimming mode used for long integration times of 24–30 μs for the large square MCT *n*-*p*-junctions needed for some applications, the detectivity was not less than $D^*\geq 2\times 10^{10}$ cm×Hz$^{1/2}$/W.

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1. Introduction

High-performance infrared (IR) imaging systems, for surveillance and reconnaissance applications, for example, currently basically include focal plane arrays (FPAs) with multielement scanning linear and staring two-dimensional matrices of photovoltaic (PV) detectors cooled down to cryogenic temperatures with a signal processor in the focal plane. The FPA technologies mainly include two major technologies, hybrid and monolithic. The concept of IR FPA hybrid technology is widespread and permits the optimization of separate parameters of the detector array, which has a large number of sensitive elements, and the typical silicon readout device coupled with the detector array.[1] The major hybrid technology uses MCT PV detector chips and silicon CCD or CMOS chips[1,2] for readout and multiplexing the sensed charge from the detectors; there are many designs for the interface, but either source coupling or gate coupling is usually used.[3–5]

Here we present some results on the technology, manufacturing and properties of 2×64 linear arrays with large area *n*-*p*-junctions and silicon CCD readouts for applications in the 8–12 micron wavelength region.

2. Growth Procedure and Diode Properties

The MBE growth technology on gallium arsenide was used with an intermediate CdZnTe layer which allows significant decrease in the CdHgTe material cost for the large-format IR focal plane arrays (FPAs) to be achieved. The advantage of the MBE technology for creating the epitaxial layers is that it seems to be the most adaptable for production of large, square MCT arrays.[6]

The HgCdTe epitaxial layers were grown on 3-inch diameter (103) GaAs substrates with an intermediate CdZnTe buffer layer. The growth temperature was within T=180–190°C for the HgCdTe layers and within T=240–300°C for the buffer layers. During the growth process, the composition of the layer was controlled by a built-in ellipsometer. The non-uniformity of the composition over an area of 1 cm^2 was not more than $\Delta x=\pm 0.001$. The as-grown layers were of *n*-type conductivity and should be converted to p-type conductivity to use boron implantation for receiving the *n*-*p*-diodes to be used with *n*-channel CCD readouts.

After 200 h of annealing at $T\approx 230$°C, the as-grown HgCdTe layers of *n*-type conductivity were converted to *p*-type conductivity layers. In the annealed samples the hole concentration P and mobility μ_p values in the film bulk at T=77 K were about $P_{77}\approx 6\times 10^{14}$ cm^{-3} and $\mu_{77}\approx 320$ $cm^2/V\cdot sec$, respectively.

To decrease the influence of surface recombination of the HgCdTe layers, they were grown with increased surface composition of x value.[7] The cross section of the structure is shown in Fig. 1. The sample has special wide gap regions ~0.5 μm thick with composition $x\approx 0.55$ near the surface, while in the interior of the layers the composition value was within x=0.219–0.220.

The epitaxial MCT films on CdZnTe buffer layers are lattice-matched and have sufficiently high crystal perfection, which is mainly determined by the substrate quality, allowing the possibility to design IR arrays operating in the BLIP regime (see, *e.g.*, refs.

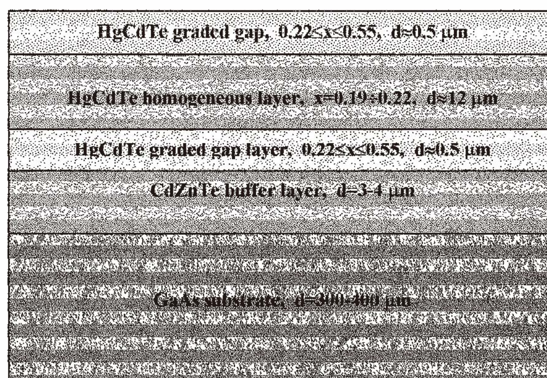

Fig. 1. Schematic cross section of MBE-grown HgCdTe heterostructure.

(6), (8) and (9)). Using gallium arsenide or silicon substrates, the growth of a large area of rather high-quality MCT epitaxial layers is possible. Still, the structural perfection of these layers is poorer than the analogous ones on CdZnTe substrates. Nevertheless, these layers are suitable for manufacturing large square arrays for the 8–12 μm wavelength range.

One of the most important parameters of MCT layers is the composition uniformity across the film area. For an FPA operating in the 8–12 μm spectral range, the changes in composition should not exceed the value Δx=0.001 across the array area, which, for a 256×256 array with pitch of about 40 μm, is about 10 mm. To provide uniformity in composition and thickness uniformity of epitaxial MCT layers across the wafer diameter, special molecular sources were designed with practically constant (during long-time processes) molecular flows. By knowing the changes in flow caused by decreasing the materials in crucibles, it was possible to correct the temperature of the source to maintain stable molecular flows.[10]

The MBE equipment was designed and manufactured with the ability to control the MCT layer growth at the level of a 76 mm GaAs wafer diameter. This equipment can still be used for epitaxial growth of MCT materials on different substrates with an automatic system controlling the technological process parameters and the layer quality *in situ.*[11] This system provides precise conditions for maintaining the buffer layer and MCT film growth on GaAs substrates. The automatic ellipsometer used allows control of the changes in thickness of layer composition and can maintain it at a constant value with high accuracy by correcting the temperature of the molecular sources. A schematic cross section of the heterostructure of the CdHgTe grown by MBE method is shown in Fig. 1.

In the grown and annealed *p*-type HgCdTe MBE epitaxial layers, the 2×64 focal plane arrays with 100 μm pitch and the large area 50×50 μm *n-p*-type photodiodes were manufactured by low-temperature planar technology as described in ref. (12). The photodiodes were obtained by boron implantation with particle energies E≈120–150 KeV.

Dark currents at $V\approx100$ mV reverse biases in diodes chosen for hybridization in the arrays with λ_{co}=12.2 μm as a rule did not exceed the values of 25–30 nA, and their zero-bias resistance-area product was within $R_0A\approx$20–30 Ohm×cm^2. The average R_0A values for array elements within the wafer were ≈6 Ohm×cm^2. The mean operability of the diodes in the arrays from 3 inch wafers was about 95–97%, and for the diodes in the arrays chosen for hybridization it was 97–100% with average sensitivity inhomogeneity values of (10–20)%.

Before hybridization with CCD multiplexers, the current-voltage characteristics of photodiode arrays and their dynamic resistance vs bias voltages were measured. The typical results are given in Fig. 2 for one of the diodes in the array. One can see that even for rather low values, compared to those of diodes with λ_{co}=10.0 μm, the values of dynamic resistance R shown at a reverse bias of 60–100 mV are sufficient to operate with direct injection input circuits of CCD readouts. For such reverse biases, the main contribution to dark current is from band-to-band tunneling.[13]

In Fig. 3 the typical responsivity spectra of the diodes from different parts of one of the arrays with λ_{co}=12.2 μm vs IR wavelength at an operating temperature T=78 K are presented. One can see rather good photoresponse homogeneity spectra for such MBE-grown HgCdTe diodes.

3. CCD Silicon Readouts

Silicon readouts with direct injection input circuits and CCD multiplexers to be used with n-p-photovoltaic multielement arrays were designed, manufactured and tested at T=77–300 K. The silicon readouts for 2×64 arrays, in which skimming and partitioning functions are performed, too, because of the need for large area diodes and a long cutoff wavelength of λ_{co}=12.2 μm, were manufactured by n-channel MOS technology with 1.2

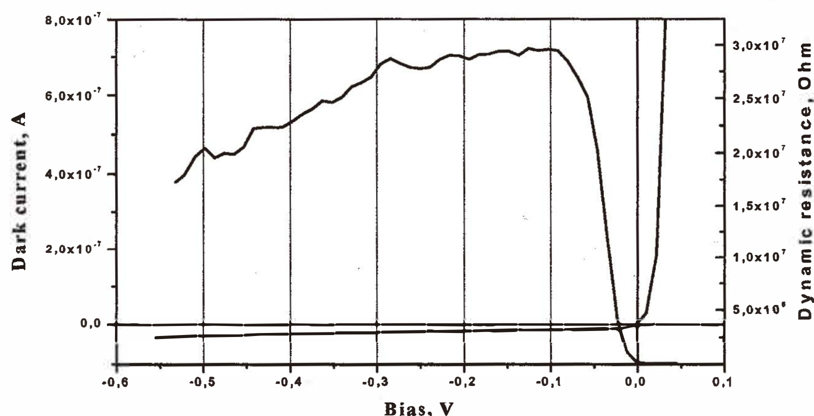

Fig. 2. Typical dependencies of dark current and dynamic resistance for one of the HgCdTe MBE-grown diodes (λ_{co} = 12.2 μm) vs bias voltage.

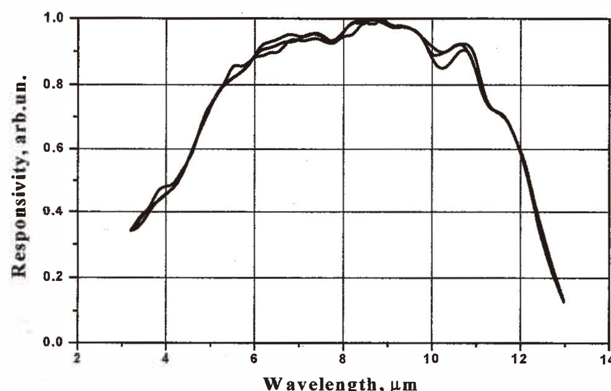

Fig. 3. Responsivity of three elements from different parts of a 2×64 MBE-grown linear array.

μm design rules with buried or surface channel CCD registers.[14,15] The designed CCD readouts are driven by four- or two-phase clock pulses. The amount of charge which can be stored in the readouts depends on the mode used. Without skimming and partitioning modes, it is 2.4 pC at an output signal of 5 V. With a partitioning mode included, it is about 4.8 pC, and it is about 7.0 pC with skimming and partitioning modes switched on.

Different operating modes depending on the application purposes can be selected, taking into account, among others, programmable integration time, required operating regime, availability of skimming level and partitioning factor. Before hybridization, CCD readouts chips were tested on wafer levels at 300 K with the help of testing transistors incorporated into inputs of the input transistors. In Fig. 4, the different operation modes of the input part of the readouts are shown schematically.

In Fig. 5, the possibilities of one of the silicon CCD readout circuits operating in different modes are presented. Currents from photodiodes were emulated by the input resistors R1...R6 (see Fig. 4) with different resistance values. By such testing it was confirmed that the CCD readouts could operate at high input currents correctly using one of the readout device modes presented.

4. Hybridization and Some Properties of FPAs

The HgCdTe arrays and Si CCD readouts were hybridized by In bumps technology. The FPA hybridization was performed by cold welding under external pressure on indium bumps[12,16] via MCT and CCD chips. In the process of chip compression, the autoplanarisation of surfaces is accomplished. When the cold welding is completed, the planar surfaces of the photodiode and the readout chips are stopped at a given distance from each other.

The maximum limit of mechanical load is determined from the measured curves of the plastic flow of indium bumps,[16] taking into account their height and area. The pressure required for plastic flow of the indium bumps lies in the range of 0.3–0.9 kg/mm^2.

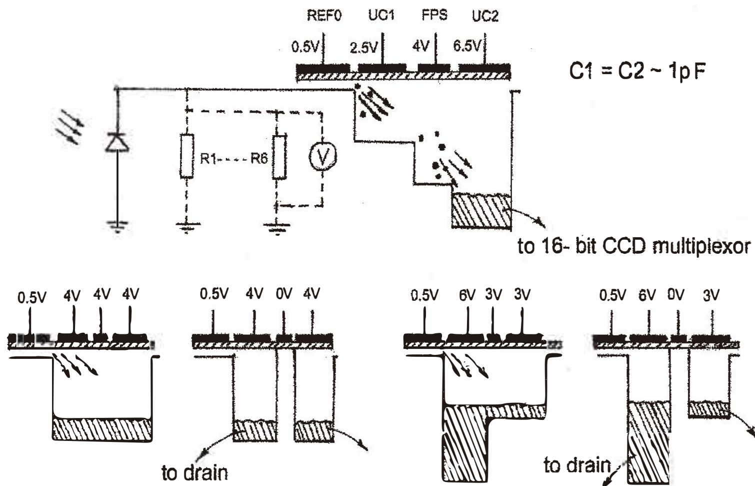

Fig. 4. Different operating modes of the input part of CCD silicon readouts.

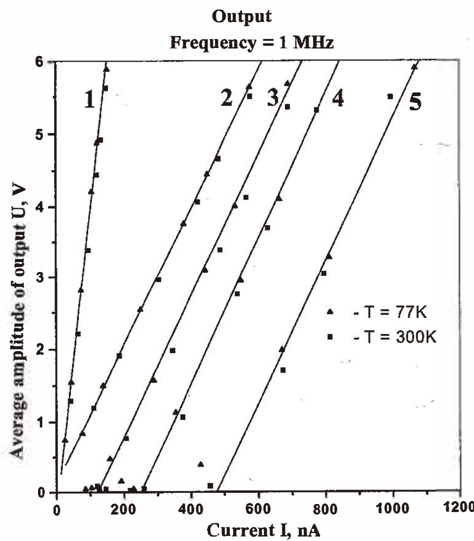

Fig. 5. Dependence of average output amplitude vs input current for a silicon readout device without a photodiode linear array. 1 — mode without skimming and partition (τ=16 μs): U_{c1}=2.5 V, U_{c2}=6.5 V, FPC =(1–1) V, FPS =(5–5) V. 2 — partition mode (τ= 8 μs): U_{c1} =5 V, U_{c2}=5 V, FPC =(1–5) V, FPS =(0–5) V. 3, 4, 5 – skimming and partition modes (τ= 8 μs): U_{c2}= 5 V, FPS =(0–5) V and 3 — U_{c1}=6 V, FPC=(1–6) V, 4 — U_{c1} =7 V, FPC =(1–7) V, 5 — U_{c1} =9 V, FPC =(1–9) V.

Investigations of the influence of vertical pressure on *n*-*p*-junction parameters on the HgCdTe layers have shown that degradation processes begin at pressures greater than 1.5 kg/mm^2.[17] Thus, for reliable welding of indium bumps with hybridized modules, a pressure of no more than 1.0 kg/mm^2 was used, and the yield of this operation reached 100 %. The total height of In bumps was about 12–15 μm. The parameters of the hybrid arrays measured have shown 100% yield after hybridization. The dark currents were the same as measured for HgCdTe arrays.

In Figs. 6 and 7 are shown the results of measurements of output signals from one of the channels with 16 diodes with and without skimming and partition modes switched on. From these figures, one can conclude that the uniformity of the signals from the diodes is about ±10%.

Even with the skimming mode used for the long integration times of 24–30 μs needed in some cases for large area *n*-*p*-junctions, the detectivity was near the ultimate performance limit for a given array. The dynamic range was not less than 60–65 dB, and the linearity transfer function was not valued at more than ±5%.

5. Test System

For measurements of photoelectric parameters of hybrid FPA arrays with silicon readout circuits, and also for measurements of the basic electrical parameters of the readout circuits at room and at liquid nitrogen temperatures, the test system was established.

As the source of infrared irradiation, a calibrated black body stabilized in the range of T=350–600 K was used. At T=500 K, under the experimental conditions chosen, the irradiation of FPA was about ~$6 \cdot 10^{-5}$ W/cm^2. The FPAs were located in optical cryostats with high-frequency coaxial lines. The temperature on the chip surfaces in cryostats was measured by a calibrated Ge thermometer. The input windows of cryostats are transparent in the spectral range from 1 to 30 microns. The cryostats have two multipin plugs to transfer 8-FPA output signals to the computer-programmable multiplexer of a registration system and to supply pulses and direct voltages from the control generator.

The amplitudes of FPA signals are defined according to the expression:

$$V_{\text{sig}}^{i} = \frac{1}{F}\sum_{j=1}^{F} V_{\text{sig}}^{j},$$

where F is the number of measurements for the i-th element in a linear array.

Uncorrelated noise signals are measured and calculated according to the expression:

$$V_{\text{nois}}^{i} = \{\frac{1}{F}\sum_{j=1}^{F}(V_{\text{sig}}^{j})^2 - [\frac{1}{F}\sum_{j=1}^{F} V_{\text{sig}}^{j}]^2\}^{-1/2},$$

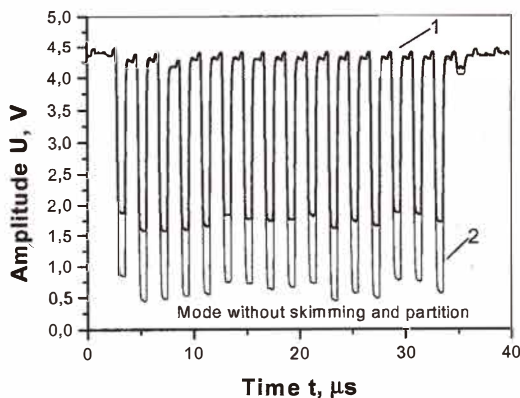

Fig. 6. FPA output signals from one of the channels of 16 MCT diodes without skimming and partition modes. Integration time $\tau = 12$ μs. 1 — Dark current regime without skimming and partition ($T = 92$ K), and 2 — background signal, flat angle of view ≈ 30°.

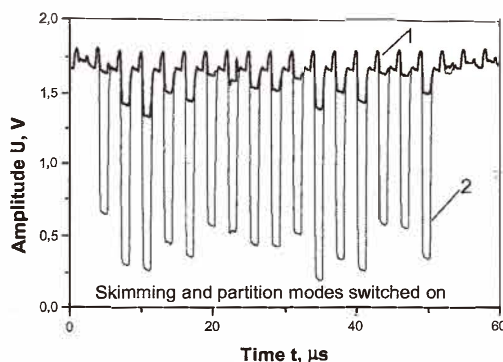

Fig. 7. FPA output signals from one of the channels of 16 MCT diodes with skimming and partition modes switched on. Integration time $t = 24$ μs. 1 — Dark current regime with skimming and partition ($T = 92$ K), and 2 — background signal, flat angle of view ≈ 30°.

To calculate detectivity D^*, the following expression was used:

$$D^* = \frac{V_{\text{sig}}}{V_{\text{nois}} \cdot H \cdot A} \left(\frac{A}{2 \cdot \tau} \right)^{1/2},$$

where H is the irradiance, A is the detector area and τ is the integration time.

In Table 1 some performance parameters for a 2×64 hybrid linear array of MBE-grown MCT diodes with silicon CCD readouts are presented at an elevated temperature

Table 1
Some performance parameters for 2 × 64 hybrid linear array of MBE-grown MCT diodes with silicon CCD readouts.

Operating temperature, K	90
Flat angle of view	30°
Black body irradiance in the range of 1–13 μm, W/cm^2	6×10^{-5}
Operating mode	Without skimming and partition
Integration time, μs	10
Photodiode area, μm^2	50 × 50
Dynamic range, dB	60
Cut-off wavelength, λ^{co}, μm	12.2
Clock frequency, MHz	0.5
Detectivity D^*, cm × Hz$^{1/2}$/W	$\geq 2 \times 10^{10}$

compared to the liquid nitrogen one. Even for this elevated temperature the detectivity is acceptable for many applications in imaging devices.

6. Conclusions

Designed, manufactured and tested 2 × 64 MCT LWIR linear arrays ($\lambda_{co} \approx 12.2$ μm) with large square diodes and CCD silicon readouts can operate even at elevated temperatures with acceptable parameters for some applications. The HgCdTe layers were grown by MBE technology on (103) GaAs substrates with CdZnTe buffer layers, and silicon CCD readouts were manufactured according to traditional CCD technology.

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