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Collective Flip-Chip Technology for Infrared Focal Plane Arrays

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After a description of the flip-chip technique developed at LETI, we present its main advantages and its evolution. Using this technique, a mass production procedure has been developed to decrease the cost of the technological step. With this method, we are able to simultaneously hybridize several linear or two-dimensional (2D) arrays directly onto readout circuits on silicon wafers. The electrical accessibility to the components provided by this method enables more detailed electrical tests to be carried out with an automatic prober before integration in cryogenic conditions, which is done only for good electrical devices. We have also developed a highly reliable method to hybridize a very large infrared focal plane array (IRFPA). With this improved technique, 2D arrays can undergo several thousand 300 K–77 K cycles without any degradation.

1. Introduction

The second-generation infrared focal plane arrays based on CdHgTe have required the development of new techniques for interconnecting the detection circuit to the readout circuit. These flip-chip techniques were developed at LETI/LIR from the end of the seventies and have enabled the start of various industrialization stages for the detection components of the third-generation anti-tank program (AC3G - TRIGAT). Following this, the technology has evolved to take into account the need to increase the performance of the components and especially to reduce manufacturing costs.

In the first part of this paper we review the principle upon which the manufacturing process being used today is based. We then describe its evolution and applications.

2. Standard Flip-Chip Technology

The LETI has substantial experience in the assembly of micro-electronic chips, and several flip-chip technologies have been studied depending on the intended applications. For military requirements, the need to cool components down to 50 K has led to the development of a technology based on indium microbumps.

The various technological phases required for the hybridization of the detectors with their readout circuits are as follows:

- Collective production of microbumps on the readout circuits,
- Dicing readout circuit chips and hybridization.

These stages are described below.

2.1 *Production of microbumps*

This first stage is an indium bump fabrication stage on the entire readout circuit wafer. The process is carried out using traditional silicon micro-electronic techniques in a back-end-type clean room and is described below. After reception of the readout circuit (Fig. 1(a)), the first step begins with the deposition of a metallic layer which has two functions (Fig. 1(b)):

- making contact with the input and output aluminum pads of the circuit in spite of the natural oxidation of the aluminum surface,
- adhesion to the indium bumps.

After this step, the indium is deposited and localized by a lift-off technique as shown

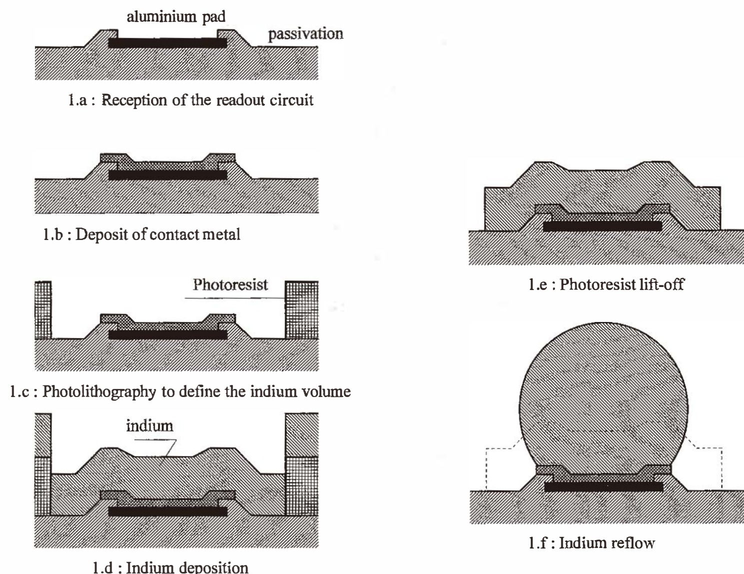


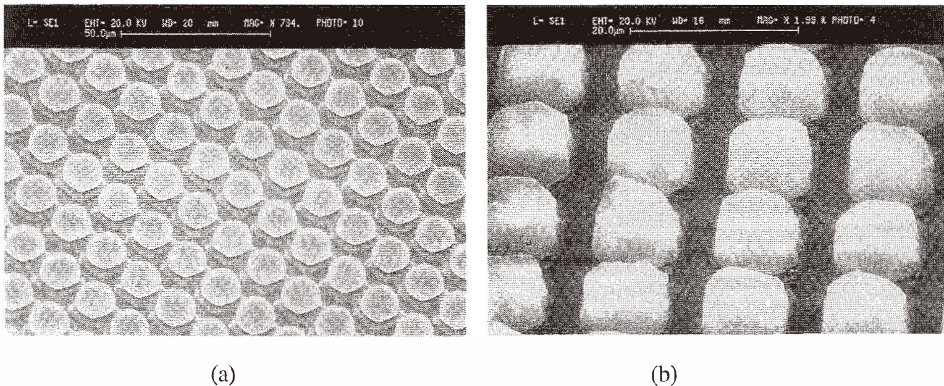
Fig. 1. Production of indium microbumps.

in Figs. 1(c), 1(d) and 1(e). The bumps are obtained by fusing of indium, which forms into balls under the influence of the surface tension of the molten metal (Fig. 1(f)). This is the reason for the high degree of homogeneity of the bumps, whose size is determined by the volume of metal deposited and the coating surface, which in turn is fixed by a photolithographic treatment (cf. Fig. 2(a)). Once the bumps have been made, the readout circuits with the bumps attached are separated by dicing the silicon wafer and are ready to be hybridized with the detection components.

2.2 *Description of the hybridization of the detection components to the readout circuits*

After the dicing procedure, the hybridization operation is carried out using specifically developed equipment which works in three steps, as shown in Fig. 3.

Step 1: Alignment of the components to be hybridized. This operation is carried out manually or automatically using previously printed keys on the components and a microscope which can mix images from each component to position them correctly relative to each other.



(a) (b)

Fig. 2. (a) View of a field of indium microbumps with a pitch of 20 μm and (b) view of a field of unreflowed indium microbumps with a pitch of 15 μm.

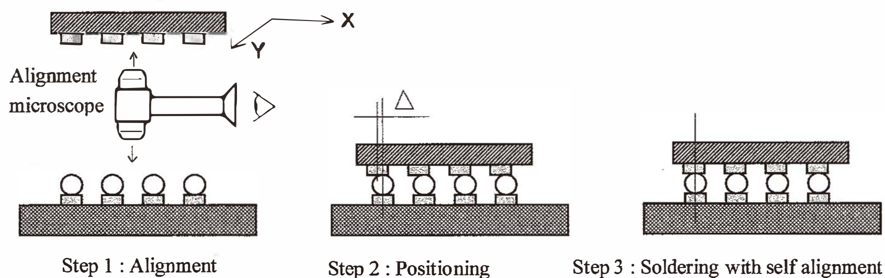


Fig. 3. Flip-chip process flow.

Step 2 : Placing the detection element onto the readout circuit while keeping alignment within a few microns. This machine can detect the contact between the components to carry out the assembly without contact pressure.
Step 3 : Welding of the two components by indium melting. The upper component is no longer held; it aligns to the lower component by the surface tension of the molten indium. The alignment accuracy is better than 1 μm (standard deviation) whatever the dimension of the hybridized chip. This accuracy was verified using glass die test vehicles which were flip-chip bonded with optical on-site measurement aids to control alignment.

This technique, developed for CdHgTe detectors (cf. Fig. 4), has been successfully used at LETI/LIR for the flip-chip on silicon readout circuits of various sources of detectors like extrinsic silicon (Si:x),[1] GaAs multi-quantum wells (QWIP), platinum silicide (PtSi), Si-Ge, or silicon detectors.

2.3 *Flip-chip method advantages*

The standard flip-chip method developed at LETI/LIR is characterized by:

- a 100% interconnection efficiency
- a proven reliability of the bonds by soldering of the components
- self-alignment of the assembled components
- a wide diversity of possible applications.[2]

The process uses only proven techniques currently employed in silicon micro-electronics, which leads to a high degree of homogeneity of the indium bumps and therefore a 100% efficiency in the interconnections. In addition, using a true soldering technique means that the interconnection reliability is maintained during thermal cycling and takes advantage of the self-alignment effect. This interconnection method therefore constitutes a solid technological base from which further evolution has been studied to take into account new requirements for components such as linear arrays of several thousand pixels or large two-dimensional arrays. The technology is now under development to take into account the pitch reduction involved because of the necessity to make use of megapixel arrays in visible and infrared spectral bands. A pitch of 15 μm is now achievable for these new devices (cf. Fig. 2(b)).

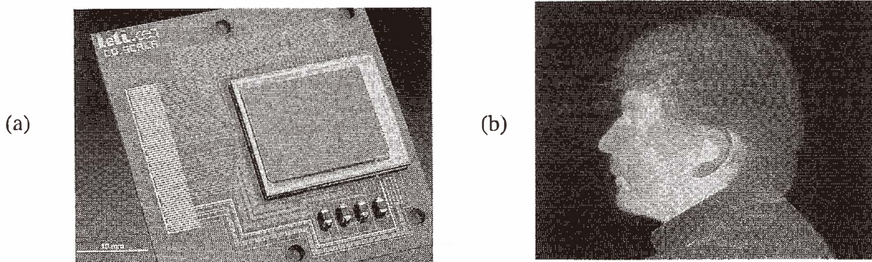


Fig. 4. IRFPA 640 × 480 pitch 25 μm and IR image (3–5 μm wavelength band).

3. Collective Flip-Chip Technology

The requirements for complex components and the need to take into account the cost reductions for infrared CMOS (IRCMOS) or infrared CCD (IRCCD) has led us to develop a collective flip-chip technology which can be used either to assemble several detectors on one readout circuit or to make several IRCMOS devices in a single operation.

The first applications of this new technique are the production of linear arrays with a large number of pixels(3,4) or the simultaneous hybridization of two-dimensional array components.(5) In this case, processing is performed on a wafer scale-up to this stage before dicing into individual detector components.

3.1 *Collective flip-chip on a wafer*

Within the framework of research to reduce the cost of infrared components, collective flip-chip makes it possible to make several components in a single operation. The procedure developed uses steps 1 and 2 concerning the alignment and placing of the components described in section 2. 2 as many times as there are components to position before carrying out a collective hybridization (step 3) of the components onto the wafer. This collective flip-chip technique is made easier since the procedure uses high temperature welding rather than cold welding. The soldering enables simultaneous hybridization of components with different surfaces and thicknesses using identical operating parameters. Figure 5 shows as an example 16 two-dimensional CdHgTe arrays (256^2 - 3–5 μm range) with a pitch of 35 μm hybridized onto a ϕ 100 mm silicon wafer comprising 16 CMOS readout circuits. This represents more than 10^6 interconnections made in one operation.

In addition to the obvious advantage over individual flip-chip operations, this technique enables more extensive electrical and opto-electrical pretests to be made because of the feasibility of addressing the input functions of each pixel. This addressing was not possible before hybridization. These tests, carried out on a test machine at low temperature, are used to select only those components having the desired performance for integration in the operational cryostat.

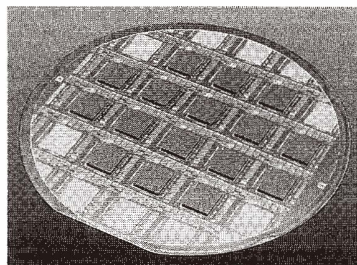


Fig. 5. Collective hybridization of 256 × 256 components on a silicon readout circuit wafer.

3.2 *The production of linear arrays with a large number of pixels*

The production of linear detector arrays with several thousand pixels requires butting methods since their length often exceeds the dimension of substrates used in the process. In addition, the level of performance required is such that it would be difficult to make them in a single module with a satisfactory manufacturing yield. The architecture of such large dimension linear components is different from traditional structures in that the detection components are no longer hybridized onto the associated readout circuit but onto an electrical interconnection network which also acts as the mechanical support.

Figure 6 shows a demonstrator made with this new architecture. In this example, 1500 CdHgTe staggered detectors with a pitch of 30 μm spread over 5 modules are interconnected to a readout circuit made up of 5 CCD chips each with 300 stages. This assembly therefore represents 10 components hybridized in a single operation onto an interconnection network[6] with the collective technique previously described in section 3.1. The technique also enables the pitch of the detectors to be respected at the seam between two modules since each module aligns automatically onto the interconnection network made using silicon micro-electronic techniques, which imposes the pitch by its design. The optical centers of each detector are situated within a cylinder with a radius of 1 μm and a height of < 4 μm centered on an ideal position. Figure 7 shows the NETD obtained along the 1500 detectors of a 3–5 μm device.

The precision of the aligner and bounder machine enables the placing and hybridization of each submodule within less than 6 μm of its neighbor; consequently, one can remove a module which proves defective and replace it with another. This repair technique is especially important for complex components with a high added value given the number of defect-free modules which must be assembled to make them up.

3.3 *Special case of flip-chip of very large arrays*

For very large two-dimensional components, one must take into account the differential thermal expansion between CdHgTe and silicon. For these components, the elasticity of the indium interconnections is too low to guarantee a large number of thermal cycles between 300 K and 77 K. To overcome this difficulty, it is essential to spread the stress

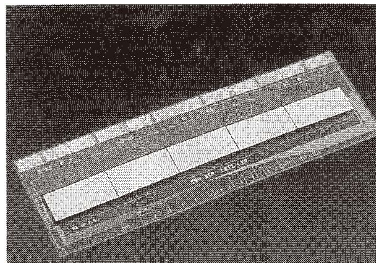


Fig. 6. Linear component with 1500 pixels at a pitch of 30 μm made by simultaneous flip-chip of several CdHgTe submodules and several silicon readout integrated circuits.

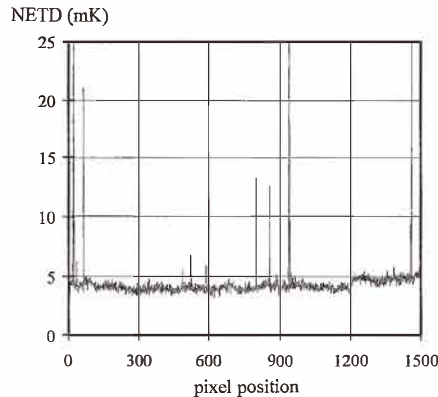


Fig. 7. Spatial distribution of NEDT along 1500 pixels in 3–5 μm wavelength band.

more equally between the CdHgTe layer and the indium bumps. The method developed at LETI/LIR is based on the collective flip-chip process shown schematically in Fig. 8. The arrays of detectors are first hybridized onto the silicon readout circuit wafer using the method previously described. The space between the detector and the readout circuit of each component is filled with an epoxy resin which is fluid enough to penetrate by capillary action. Once the hybridized components have been under-filled in this way, the CdZnTe substrates of the detector chips are thinned by polishing and coated with an antireflection layer adapted to the wavelength of the detectors. The thinning processes used were specially developed not to degrade the performance of the detectors. For instance, at 77 K the characteristics of the detectors are unchanged after thinning.

4. Conclusion

The flip-chip technology developed to make second-generation infrared detectors was carried out with the aim of increasing the performance of the components and reducing costs by replacing operations on single components by a collective production process. The validation of these improvements and the total control of the new procedures has allowed us to transfer the process to Sofradir for industrial production which will offer a solution to the needs of the market for lower-cost, high-performance infrared detectors. Flip-chip studies are continuing at LIR to reduce the detector pitch of components to be hybridized down to 15 μm or less in the 3–5 μm range with the aim of making focal plane arrays with a greater number of pixels for high-resolution infrared imaging applications.

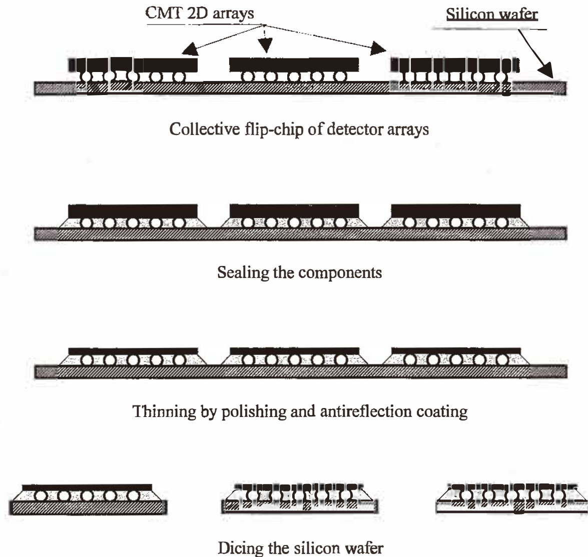


Fig. 8. Diagram of the stages needed for hybridization of very large components.

Acknowledgements

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