Sensors and Materials, Vol. 35, No. 6 (2023) 1941–1955
MYU Tokyo

S & M 3300

MEMS Electrostatic Energy Harvester Developed by Simultaneous Process for Anodic Bonding and Electret Charging

Hiroaki Honma,* Sho Ikeno, and Hiroshi Toshiyoshi

Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan

(Received March 24, 2023; accepted June 15, 2023)

Keywords: IoT, MEMS, vibrational energy harvester, electret, anodic bonding

In this paper, we present a new structure and a process for electrostatic energy harvesters fabricated using a silicon-on-glass wafer. Conventional electret-based MEMS energy harvesters are produced using a silicon-on-insulator (SOI) wafer, which is inevitably accompanied by parasitic capacitances across the buried oxide layer. The new harvester, on the other hand, can be formed by individually developing silicon and glass parts and subsequently putting them together by anodic bonding, thereby virtually eliminating parasitic capacitance. Special caution is taken not to cause the destruction of the electret layer during high-temperature anodic bonding. The device has been successfully fabricated and experimentally confirmed to function as an energy harvester. This silicon-on-glass structure is beneficial in not only suppressing the parasitic capacitance but also increasing its output power compared with those made by the conventional SOI-based process.

1. Introduction

The operating power for wireless sensor nodes is usually provided through batteries for ease of installation.[1] However, batteries require periodical replacement when depleted, leading to extra maintenance and labor cost.[2] As their alternative, power sources called energy harvesters that generate energy from the surrounding environment have attracted attention as an enabling technology to realize, for example, a sensor network for infrastructure monitoring.[3] There are various types of ambient energy source, among which environmental vibration is popular. The power density of vibrations is not as high as that of sunshine, but it ubiquitously exists regardless of the weather conditions[4] and the time of day. Most environmental vibrations are seen in the acceleration range of 1 G (G = 9.8 m/s^2) or smaller,[5,6] and they can be converted into electrical power using a carefully designed MEMS-based energy conversion mechanism such as the piezoelectric effect,[7–11] electromagnetic induction,[12–16] and electrostatic induction.[17–32] Amongst them, electrostatic energy harvesters using the permanent electrical charge or so-called electret can effectively convert small mechanical vibrations into electrical power, owing

*Corresponding author: e-mail: honma-hh@mech.kobe-u.ac.jp
https://doi.org/10.18494/SAM4402

ISSN 0914-4935 © MYU K.K.
https://myukk.org/

to the advantage that the mechanical resonator part and power-generating electrodes can be independently designed to optimize the harvester performance as a velocity-damped resonance generator (VDRG).[33]

Figure 1(a) shows a photograph of an electret-type vibrational energy harvester reported elsewhere.[34] The device structures were produced by the deep reactive ion etching (DRIE) of a silicon-on-insulator (SOI) wafer. The scanning electron microscopy (SEM) image of the electrodes and electrical interconnections is shown in Fig. 1(b). Symmetric comb structures (total of 900 pairs on each side) were fabricated using the top silicon layer. Figure 1(c) schematically shows the comb electrodes coated with a silicon oxide layer of electret doped with potassium ions. The device generates electrostatic inductive currents when the relative distance

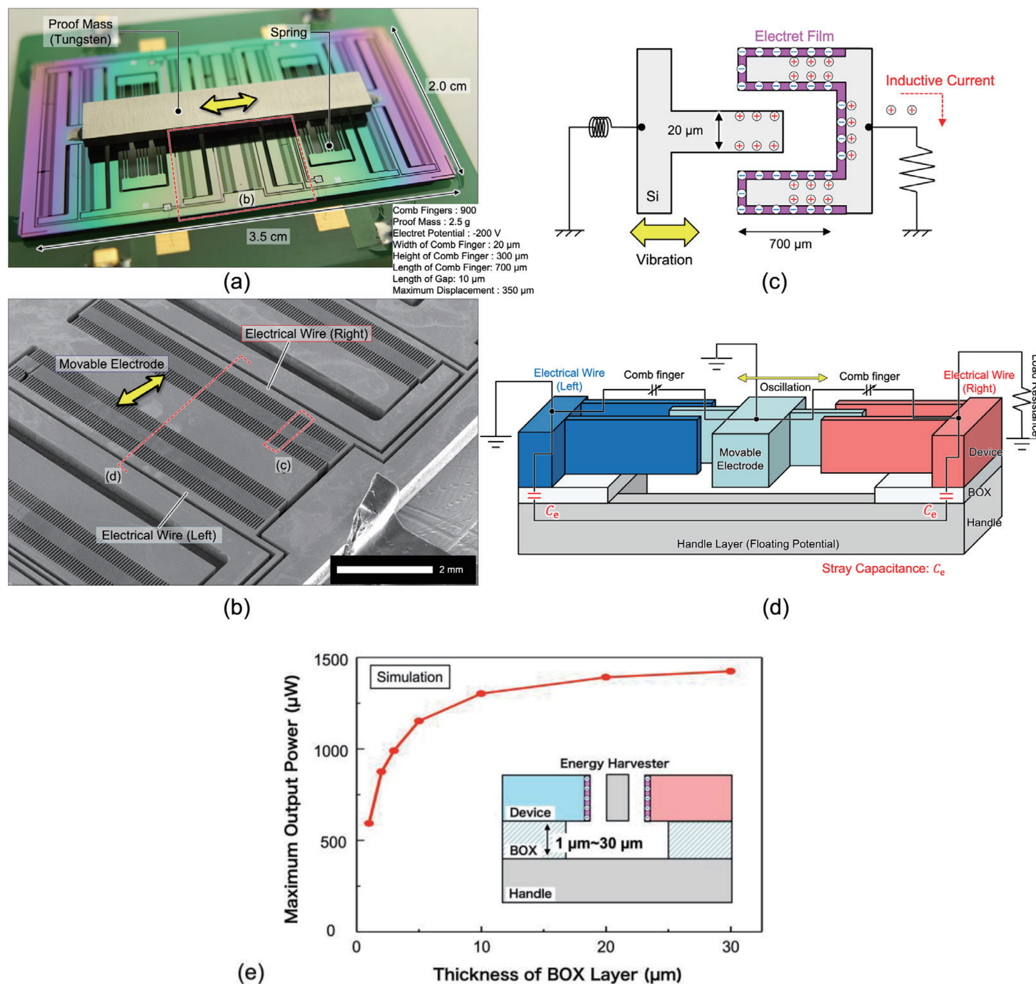


Fig. 1. (Color online) Energy harvester composed of comb electrodes covered with electrets, which is developed by DRIE of an SOI wafer. (a) Photograph of the entire chip. (b) SEM image of the comb electrodes and electrical interconnection lines. (c) Schematic of the comb electrodes covered with a silicon oxide electret film doped with potassium ions. (d) Comb electrodes and equivalent electrical circuit. The two electrical contact pads on the left- and right-hand sides are coupled via the handle layer of silicon forming a series of stray capacitances. (e) Output power when the BOX layer behaves as an internal parasitic capacitance.

between the comb electrodes changes owing to mechanical vibrations. As reported elsewhere,[34] the output power is enhanced using a higher electret potential (−200 V with respect to the electrically grounded movable electrodes) and a large surface area of the electrodes (i.e., using a high aspect ratio of the comb fingers of ~40). Owing to recent improvements, the maximum deliverable power of 435 μW has been realized from the input vibrations of 138 Hz at 0.2 *G*.[35]

Although the use of an SOI wafer is beneficial for forming mechanically movable electrodes, the electrical interconnection patterns formed in the SOI layer inevitably have parasitic capacitances with respect to the handle layer as illustrated in Fig. 1(d). Figure 1(e) shows the output power when the buried oxide (BOX) layer of different thickness is used. The output increases when the BOX layer is made thicker and the parasitic capacitance decreases. The stray capacitance can be lowered to some extent using an SOI of a thick BOX layer as reported elsewhere.[36] Nonetheless, an equivalent circuit model suggested that the BOX layer thickness needed to eliminate the effect of the stray capacitance would be more than 10 μm, which is not practically available from a cost and residual-stress viewpoint of SOI wafers.

In this paper, we describe an electrostatic energy harvester formed in a silicon-on-glass (SoG) structure to virtually eliminate the effect of parasitic capacitance. Presuming that the SoG device in this work is equivalent to the SOI device with a very thick BOX layer, the output is estimated to have been improved more than ×1.5 compared with the SOI device with a 2-μm-thick BOX layer. A fabrication process of anodic wafer bonding that is compatible with the electret forming is discussed in detail. To the best of the authors' knowledge, this is the first report of a MEMS vibrational energy harvester made as an SoG layer structure.

2. SoG-type Electrostatic Energy Harvester

Figure 2(a) shows a schematic of an electrostatic energy harvester produced using a silicon substrate bonded on a Tempax® glass substrate, instead of an SOI wafer. The electret-comb electrodes and suspensions functioning as a VDRG are located in the silicon substrate. On the other hand, the glass substrate functions as an electrically insulating frame with a cavity to avoid friction with the movable electrode formed in the SOI substrate. These two substrates are firmly joined by anodic bonding.

Figure 2(b) shows the cross-sectional diagram, corresponding to structures in the red box shown in Fig. 2(a). When using an SOI wafer, the active and handle layers face each other having an electrical insulator in between, which produces a series of parasitic capacitors connected through the handle wafer. When using an SoG substrate, on the other hand, the comb electrodes formed in the silicon substrate are mechanically fixed by the insulating glass frame without having another silicon handle layer, thereby virtually eliminating the internal parasitic capacitance. As a result, the inductive charge is delivered to the load resistance without bypassing the reactive current.

In this work, the silicon oxide film doped with potassium ions is utilized as an electret film because it can be formed even on the sidewalls of comb electrodes. Anodic bonding and electret charging are schematically shown in Figs. 2(c-1) and 2(c-2), respectively. When bonding a sodium-doped Tempax® glass and a silicon wafer, sodium ions move away from the bonding

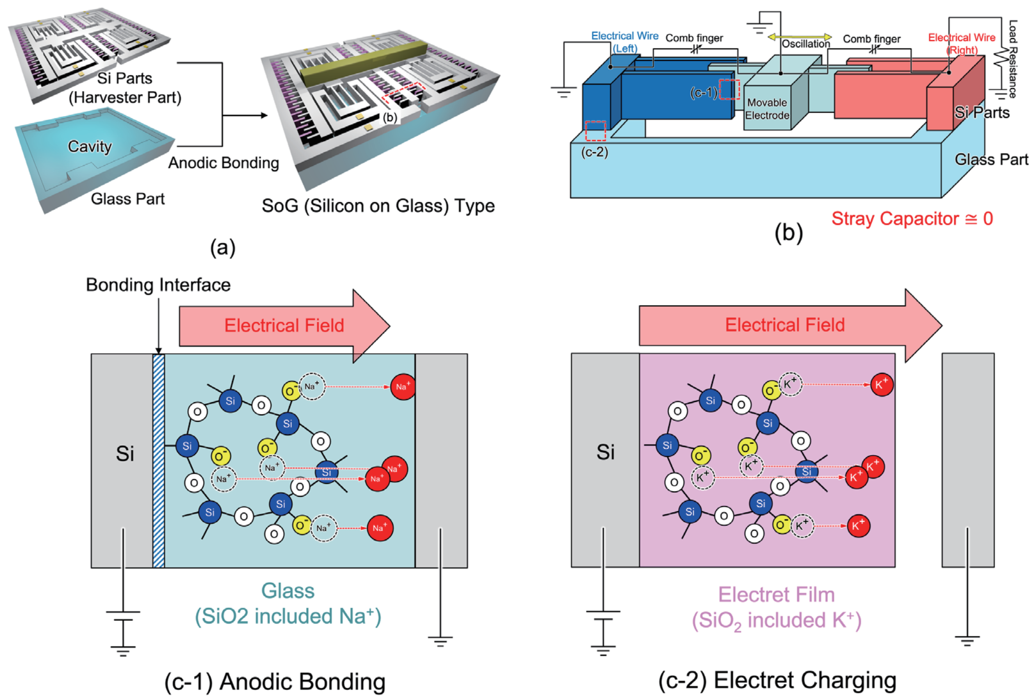


Fig. 2. (Color online) SoG-type electrostatic energy harvester composed of silicon and glass substrates. Schematics of (a) entire chip and (b) comb electrodes, and equivalent electrical circuit. Schematics of (c-1) anodic bonding and (c-2) electret charging.

interface (i.e., the anode) owing to the high electrical field and temperature as high as 500 ℃. When polarizing the electret film in this work, on the other hand, potassium ions are displaced to the cathode side using the physics similar to that of anodic bonding as documented in detail elsewhere.[37–39] These two processes are substantially the same from an ion-migration viewpoint. We only need to figure out a total process so as not to mitigate the built-in potential of anodic bonding during the subsequent electret formation.

3. Fabrication

Before discussing the details, we show a brief outline of the whole process using the schematics shown in Fig. 3. The top views of the silicon and glass substrates are shown in the upper part of the figure, whereas Figs. 3(A)–3(F) show the process flows of two cross sections a-a’ and b-b’. Photographs on the right-hand side are the chip appearances during the process.

In step (A), the process begins with a silicon wafer of 525 µm thickness. A silicon nitride (SiN) layer of 200 nm thickness is deposited on both the top and bottom surfaces of the wafer by low-pressure chemical vapor deposition (LPCVD). In step (B), the SiN layers are patterned using reactive ion etching (RIE) equipment (Samco Inc., RIE-10NR); the SiN layers serve as a protective mask against the local oxidation of silicon (LOCOS) process later. The half-etching of silicon is performed from the back side of the wafer by deep reactive ion etching (DRIE) (SPP

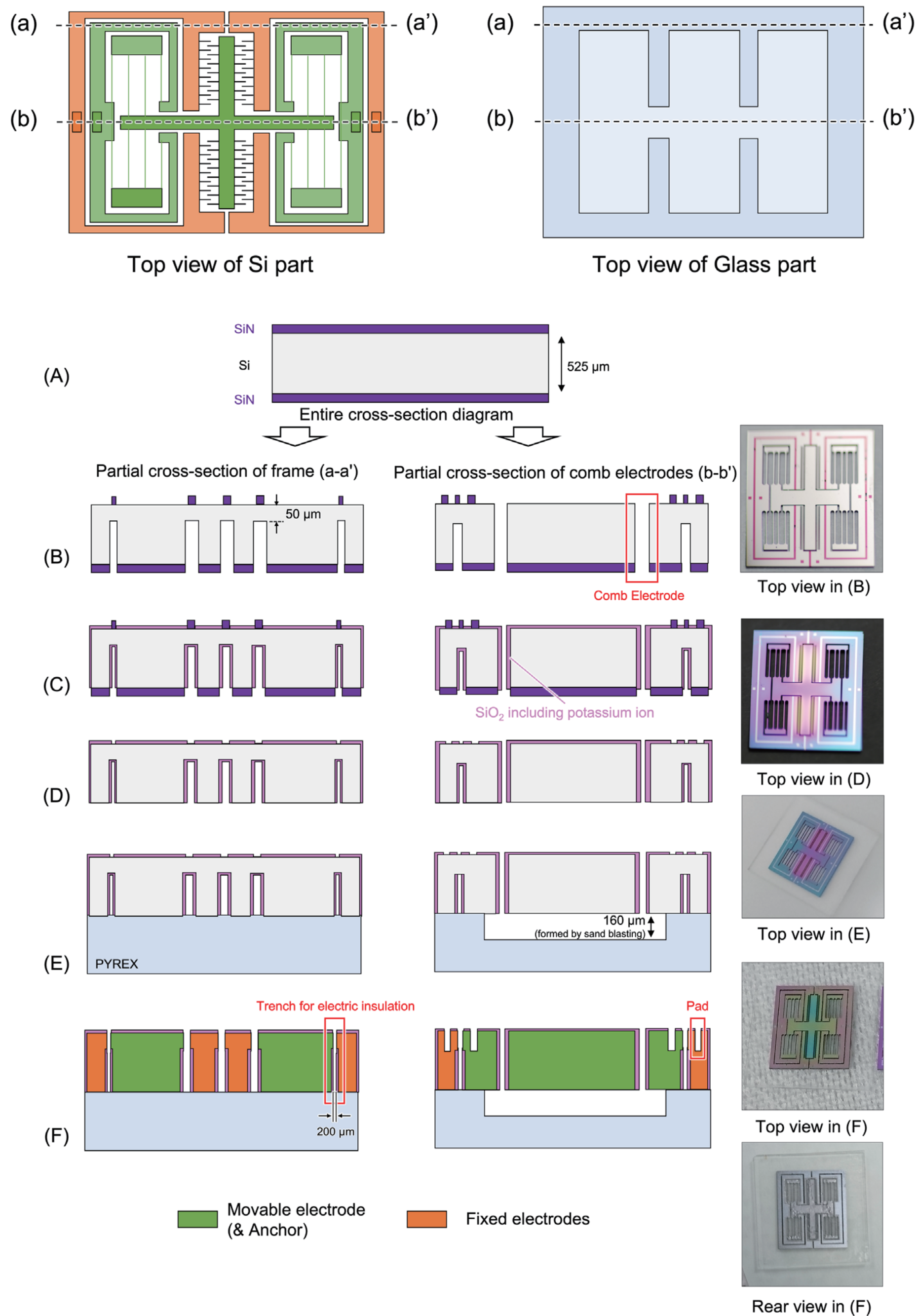


Fig. 3. (Color online) Fabrication process flow of the SoG structure.

Technologies Co., Ltd., Predeus), leaving only 50 μm of silicon. The purpose of this half-etching is to minimize the surface damage that will occur at the final etching process separating the movable and fixed electrodes. After half-etching, the full etching of the comb patterns is carried out from the top side of the wafer. In this etching process, a soft dummy mask is added to temporarily protect the wider aperture, aside from a hard mask, to cope with the loading effect resulting from the different aperture widths in the comb electrode patterns.

In step (C), to form the silicon oxide film including potassium ions, the surface of the silicon substrate is thermally oxidized for 8 h at a furnace temperature of 1000 °C using a water bubbler containing an aqueous solution of potassium hydroxide (KOH); the detailed process has been reported elsewhere.[37–39] In step (D), the SiN patterns on both sides of the silicon substrate are removed by RIE, partially exposing the silicon surface for later use. In step (E), a 500-μm-thick Tempax glass is prepared by sand blast to form a 160-μm-deep recess. The silicon substrate is then mounted on the glass substrate and put together by anodic bonding. In this process, the two substrates are annealed directly on a heater and electrically biased with 700 V_{dc} for 15 min.

In step (F), another half-etching is performed by DRIE from the top side of the SoG structure; the SiN film formed for the LOCOS process is removed by RIE, and the silicon areas that have been hidden under the SiN film reappear, allowing the subsequent DRIE using the oxide patterns as an etching mask. The trenches formed in the silicon substrate isolate the movable electrodes from the fixed ones.

4. Fabrication Details

4.1 Sacrificial photoresist masks for uniform trench DRIE

In this section, we describe the fabrication method for the tall comb structures using a silicon wafer. Vibrational energy harvesters are known to deliver relatively large power when excited at large strokes, and therefore utilizing electrodes of long comb fingers is preferred. Such an electrode design, however, inevitably requires etching mask patterns of different aperture widths, including the small gap between the comb fingers and a relatively wide opening between the fingertip and the comb pocket.

The mixed use of different aperture sizes usually causes different trench etching rates and profiles including lateral notches, leading to inhomogeneous trench depths and profiles distributed over the wafer, usually referred to as aspect-ratio-dependent etching (ARDE).[40] To mitigate this effect, we utilized photoresist masks (S1805, Microposit) as a soft compensation mask filling the gap made in the regular aluminum mask patterns for the comb electrodes, as shown in Fig. 4(a).

Figure 4(b) shows the cross-sectional views of trench etching using the combination of the photoresist and aluminum masks. The soft photoresist mask temporarily protects the wide aperture between the comb electrodes until the latter half of etching; the area protected under the photoresist is eventually removed as a final shape by time-delayed etching. The opening between the photoresist and an aluminum mask is intentionally designed to be equal (15 μm) to that between the aluminum masks shown in Fig. 4(c), and therefore, the etching is programmed to finish at the same time throughout the wafer without causing lateral notches at the bottom of the trenches. The top and rear surfaces of electrodes are shown in Figs. 4(d-1) and 4(d-2), respectively; no notch etching is seen, and the mask patterns have been transferred to the bottom with high fidelity. In the device, the comb electrode thickness is 525 μm, which is identical to the wafer thickness.

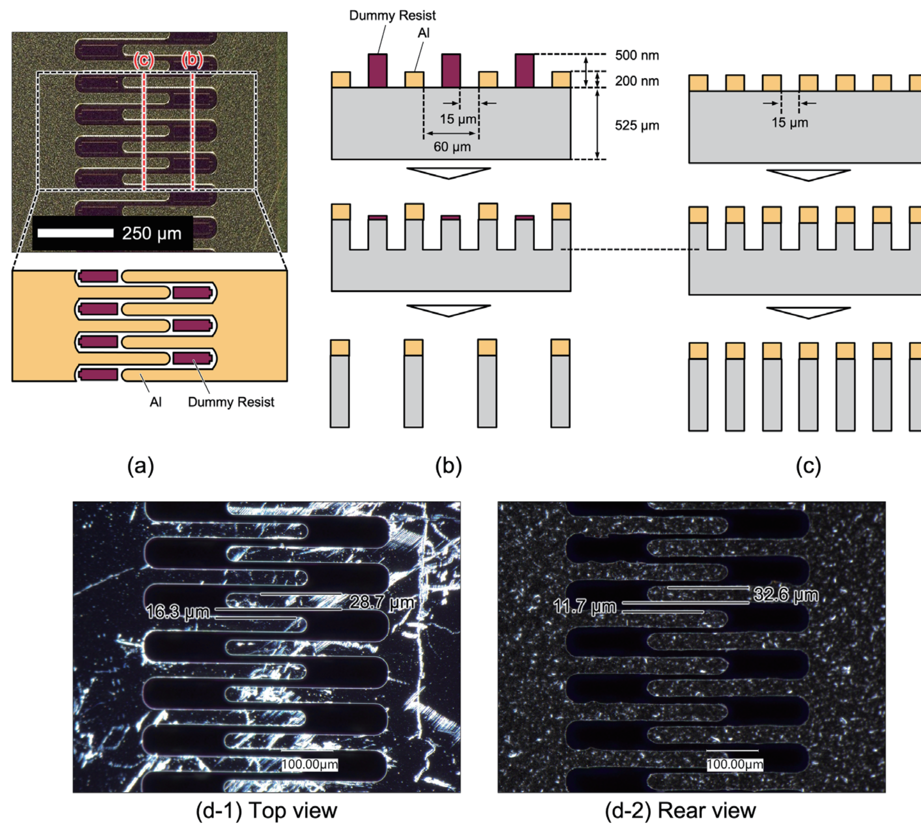


Fig. 4. (Color online) (a) Two types of dry etching mask for the comb structure formed in a silicon wafer. Aluminum and photoresist (S1805, Microposit) are used as a hard mask and a soft dummy mask, respectively. Cross sections of the etching process flow in the (b) narrow- and (c) wide-aperture areas. (d-1) Top and (d-2) rear surfaces of the comb fingers after etching.

4.2 Trench for electric insulation

Most electrostatic energy harvesters made of an SOI wafer use electrically isolated movable and fixed electrodes that are placed on a handle wafer with an electrical insulator layer in between, so that they can be individually biased at arbitrary voltages. The electrodes in an SoG wafer, on the other hand, are made out of a single silicon wafer; for this reason, any patterns surrounded by a trench would have fallen off the substrate. In this work, therefore, we developed a process to create isolation trenches after bonding the single silicon wafer onto a glass substrate.

The total process was deliberately designed not to cause excess production errors in the outline dimensions of the electrodes. First, we utilized half-etching from the rear side of the single silicon wafer by DRIE before wafer bonding, leaving an unetched thickness of 50 µm on the front side as shown in Fig. 3(B). The silicon nitride layers on both surfaces of the wafer are used to protect a few spots of the silicon area from the subsequent LOCOS process so that they can be used as bonding pads later. After oxidation, the silicon nitride mask was removed by RIE using CF_4 gas. The RF power and the pressure were set to be 100 W and 5 Pa, respectively.

During this process, the etching into the silicon oxide layer was negligible owing to the high etching speed contrast between silicon and silicon oxide. The silicon nitride layer also protects another part of the silicon surface so that the remaining 50-µm-thick silicon layer can be etched from the front side to complete the electrical isolation between the electrodes. This additional DRIE takes place after bonding the silicon wafer onto the glass substrate, and therefore, the individual electrodes are firmly fixed without causing mechanical defects.

Figure 5(a) shows a photograph of the entire chip after forming the trenches from the front side. The surface is the silicon oxide layer including potassium ions. Figure 5(b) indicates the area where there are trenches and the electrode pad. The trenches with an opening of 258 µm width are formed into the substrate down to the interface to the glass substrate. Figure 5(c) shows the three-dimensional profile of the electrode pad measured using an optical microscope (Keyence, VHX-7000). The pad was recessed by 40 µm from the top face of the silicon by the final silicon etching, but it did not affect the wire-bonding result. Figure 6 shows the photographs before and after separating the electrodes. The top silicon oxide layer is slightly thinned by the

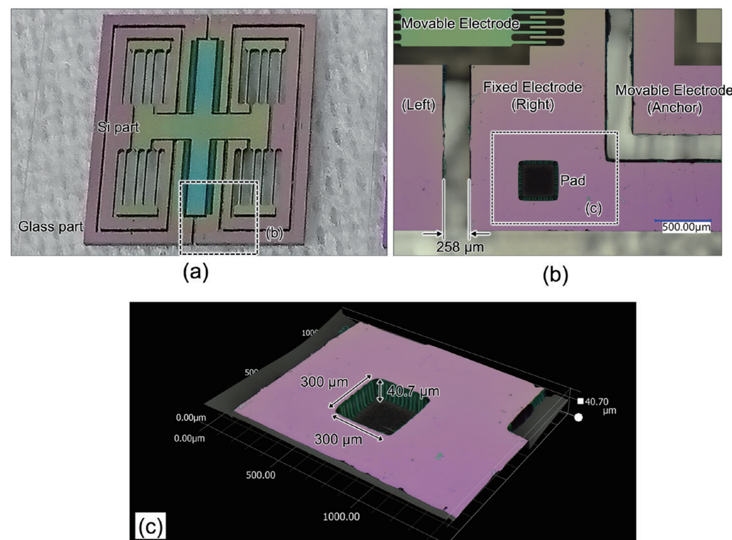


Fig. 5. (Color online) (a) Entire chip after forming the trenches for electrical isolation. (b) Trenches and the electrode pad. (c) Three-dimensional shape data of the electrode pad measured using a microscope (Keyence, VHX-7000).

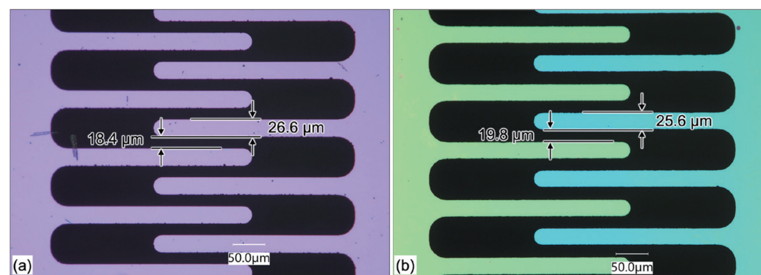


Fig. 6. (Color online) Comb fingers (a) before and (b) after completing the trench isolation etching.

final etching, and the interference color has changed from violet to green. Owing to the half-etching performed in advance, the total etching time has been shortened to minimize the thinned film of the silicon oxide layer, which still functions as an electret. Isolation trench etching was successful without causing the deformation of outline dimensions of the comb structures.

4.3 Simultaneous process for anodic bonding and electret charging

Since the electret forming process also utilizes high-temperature annealing, silicon and Tempax® glass substrates that have been anodically bonded might fall apart owing to the rediffusion of the sodium ions. Considering that the physical mechanism of anodic bonding is substantially the same as that of electret formation, which only uses different species of ions, we have developed a method of charging the electret without causing the delamination of the anodically bonded interface, i.e., applying voltage to maintain the bonding between the wafers while electrically biasing the electrodes for electret charging.

The electrical setup using three tungsten probes applying voltage to the chip is shown in Fig. 7(a). Two voltages, 700 and 800 V, are applied to the chip frame and fixed electrodes, respectively, as schematically shown in Fig. 7(b), thereby electrostatically holding the entire chip on the glass substrate. At the same time, the said voltages are applied to the fixed and movable electrodes as shown in Fig. 7(c), leaving the differential voltage of 100 V across the air gap to form an electret skin on the fixed electrodes.

To verify the polarization process, the surface potential formed by the electret was examined using a surface potential profiler (TREK Japan, Model 344) as shown in Fig. 8(a). The sensor head was held and scanned over the chip as shown in Fig. 8(b) to monitor the space-averaged potential within the area of the sensor head. Figure 8(c) shows the result of potential

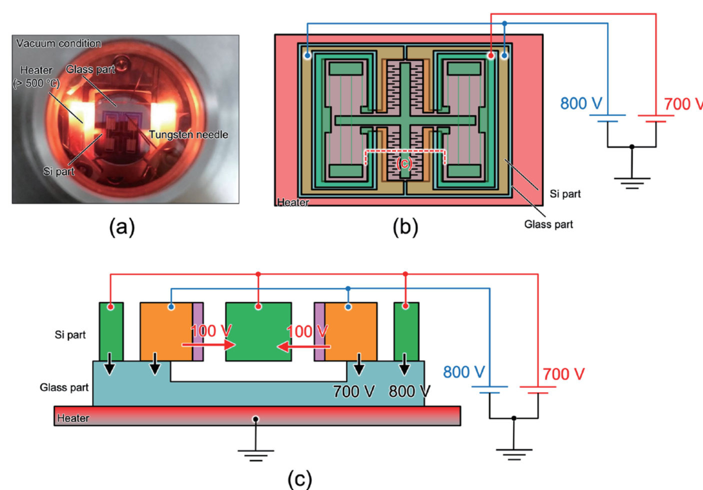


Fig. 7. (Color online) Simultaneous process for anodic bonding and electret charging. (a) Experiment setup in the vacuum chamber. (b) Top and (c) side views of voltage application.

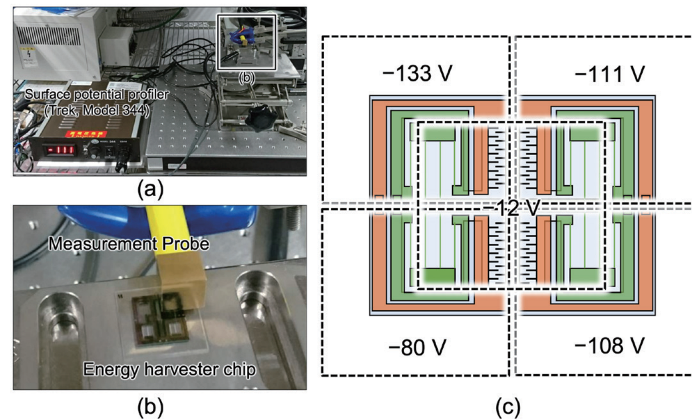


Fig. 8. (Color online) (a) Entire system for determining the surface potential. (b) Close-up view of the measurement probe. (c) Potential distribution measured using the surface potential profiler (TREK Japan, Model 344).

measurement. The potential in the middle part of the chip was as small as −12 V, reflecting the fact that the suspended electrodes are pulled down to GND; the surface potential profiler used in this work has a sensing head of as large as 1 cm, and the potential distribution within this area is averaged for sensing. The potentials measured near the corners of the chip were relatively high, −80–−133 V, because the silicon parts fixed on the glass substrate retain higher potentials for anodic bonding as well as electret formation.

Figure 9(a) shows a photograph of the completed device. The size of the silicon part is 12.5 × 14.3 mm^2, and that of the glass part is 18.5 mm^2. After polarization, the chip was glued onto the printed circuit board and then the electrode pads were interconnected by wedge wire bonding.

Figures 9(b) and 9(c) show photographs of the rear side of the chip. The grainy silver surfaces seen in the figure show the anodically bonded interface. Trenches for electrical isolation can be seen between the silicon structures. In addition, the anchor part of the movable electrode was found to have been firmly fixed on the glass part. The springs and comb electrodes were off the focal plane owing to the cavity formed on the glass surface, which can be seen through the glass substrate from the rear side.

5. Experimental Results

To verify the power generation performance, the completed chip was tested using the electromagnetic shaker (Emic, 9514-AN/SD 373-A, DCS-98S Smart) as shown in Fig. 10(a). A high-speed microscope camera (Keyence VW9000SP) was used in the upright position above the shaker to monitor the harvester's mechanical motion. Figure 10(b) shows the snapshot images of the chip in operation when an input vibration was applied in the lateral direction with a magnitude of 0.8 *G* at 1694 Hz. The movable electrodes were found to oscillate to the full scale, while the fixed electrode seemed to be stationary, implying that the incoming oscillation

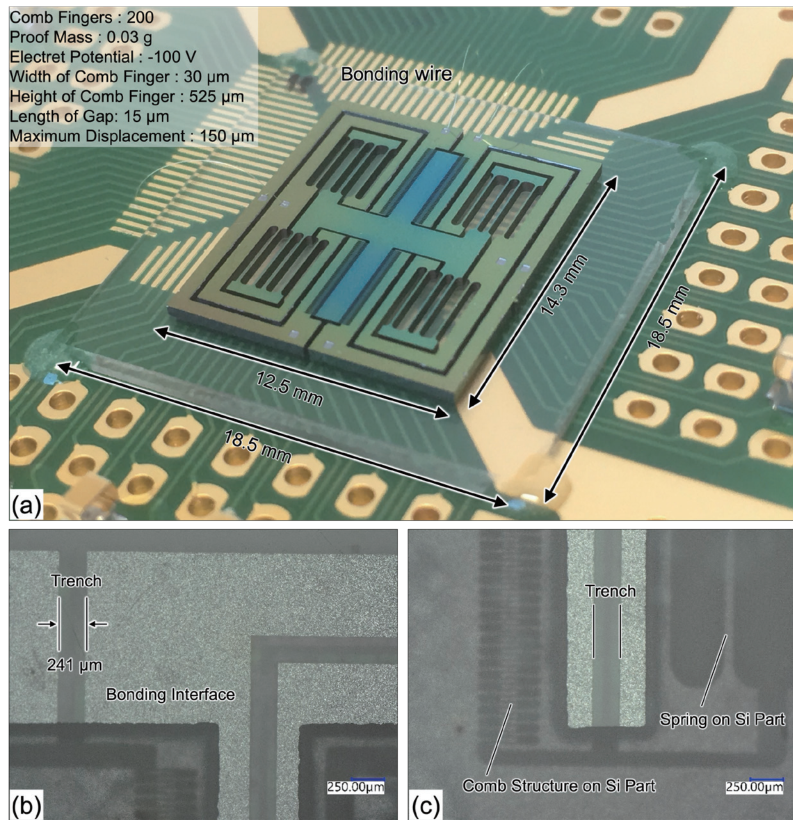


Fig. 9. (Color online) (a) Photograph of the energy harvester chip. (b) Rear side view of the bonded part. (c) Rear view of the bonded and suspended parts.

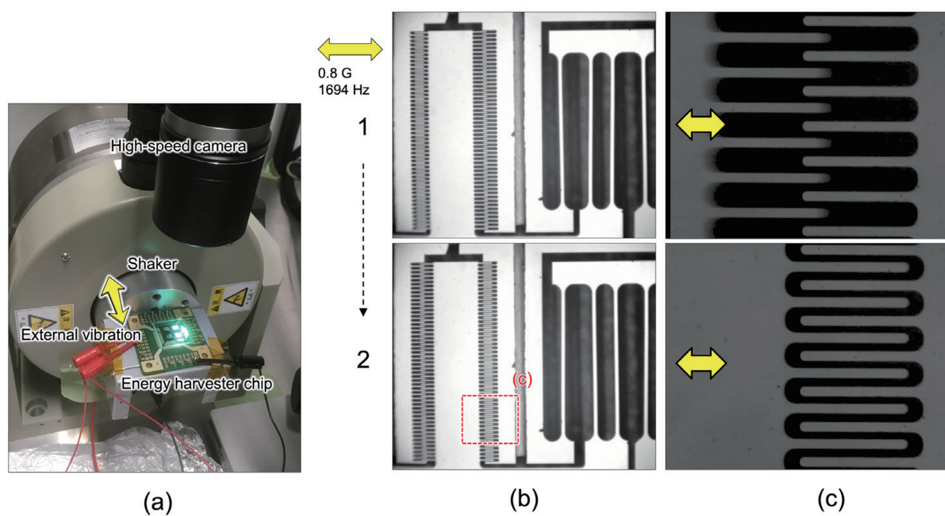


Fig. 10. (Color online) (a) Photograph of the energy harvester chip under vibration test. Snapshot images of the (b) elastic springs and (c) comb electrodes in operation taken with a high-speed camera.

was effectively amplified within the suspended resonance system to cause a large oscillation of the suspended mass. Figure 10(c) shows the detailed snapshot images of the comb electrodes under an acceleration of 1.5 *G*. The electrodes' motion was close to the maximum displacement of ±150 μm.

Figure 11(a) illustrates the electrical circuit for the measurement of the output power. A current–voltage converter (Hamamatsu, C7319) was used to electrically decouple the device under test from the input impedance of the oscilloscope. An experimentally observed short-circuit current waveform is shown in Fig. 11(b) when the chip was shaken by an acceleration of 0.8 *G* at 1694 Hz. This waveform suggests that the movable electrodes oscillated with a sinusoidal wave similar to the input acceleration waveform. Figure 11(c) shows the experimental result of the output power as a function of the input acceleration, when the chip was loaded by 3 MΩ and excited to the stroke limit at 1694 Hz. From this result, the output power was found to have been increased by the square of the input acceleration. In addition to this, no mechanical failure was observed on the device even when the input acceleration was increased to 1.5 *G*, where the mechanical stroke reached its limits.

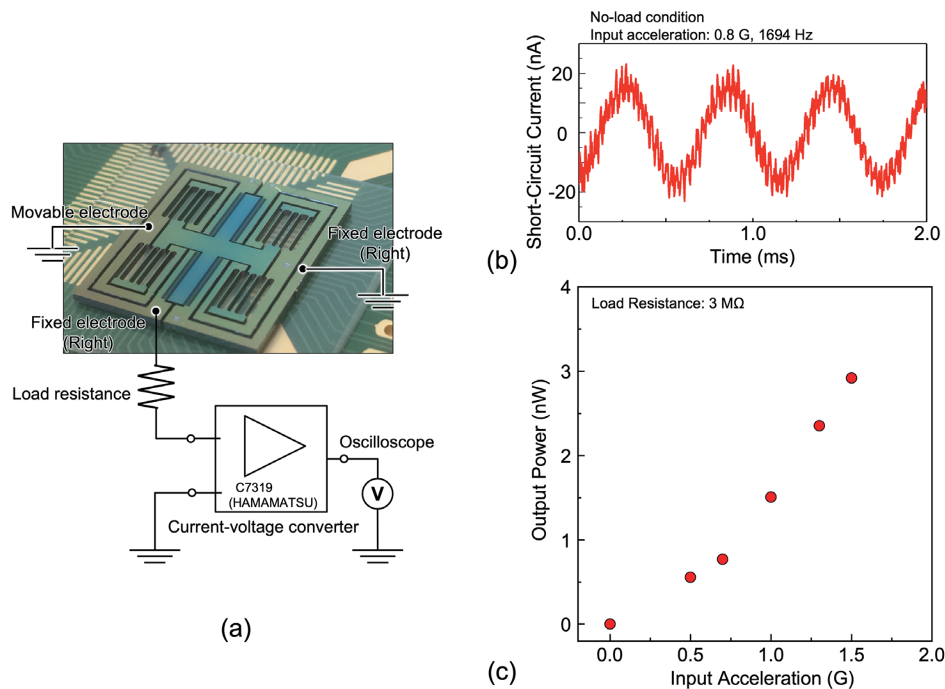


Fig. 11. (Color online) (a) Circuit diagram for measuring the output current and power. A load resistance is inserted between the output terminal of the chip and the virtual ground point of the amplifier. (b) Short-circuit current waveform under a sinusoidal oscillation with acceleration of 0.8 *G* at 1694 Hz. (c) Output power as a function of the input acceleration when the energy harvester was loaded by 3 MΩ and operated to the stroke limit (±150 μm) at 1694 Hz.

6. Conclusions

In this work, an electrostatic energy harvester formed in an SoG structure was proposed as a new design to mitigate the effect of internal parasitic capacitance. The newly developed structure was realized by the combination of (1) sacrificial photoresist masks for uniform trench DRIE, (2) deep trenches for electrical isolation in a single silicon wafer, and (3) the simultaneous process of anodic bonding and electret charging. After polarization, we confirmed that the device surface had a potential of approximately −100 V, which was close to the differential voltage between the voltages applied for electret charging and anodic bonding. Electrostatic induction current was observed as expected during mechanical excitation. No mechanical delamination of layers was observed even when the mechanical stroke reached its limits under hard excitation of 0.8 *G* at 1694 Hz, indicating a sufficiently large bonding strength for vibrational energy harvester applications. When the chip was loaded by 3 MΩ and operated at the resonance, the output power was enhanced to 3 nW at 1.5 *G*. In conclusion, electrostatic energy harvester structures fabricated using the conventional SOI wafer can be replaced with the newly developed SoG structures to suppress the reactive power that does not contribute to the net output power.

Acknowledgments

This work was supported by JST CREST Grant Numbers JPMJCR15Q4 and JPMJCR19Q2. This work was also supported by JSPS Grant-in-Aid for Scientific Research (B), Grant Numbers 18H01490 and 19K15038.

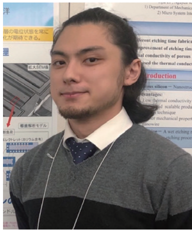
References

1 L. Atzori, A. Iera, and G. Morabito: Comput. Netw. **54** (2010) 2787. https://doi.org/10.1016/j.comnet.2010.05.010
2 S. Roundy, P. K. Wright, and J. Rabaey: Comput. Commun. **26** (2003) 1131. https://doi.org/10.1016/S0140-3664(02)00248-7
3 H. Toshiyoshi, S. Ju, H. Honma, C.-H. Ji, and H. Fujita: Sci. Techno. Adv. Mater. **20** (2019) 124. https://doi.org/10.1080/14686996.2019.1569828
4 N. S. Hudak and G. G. Amatucci: J. Appl. Phys. **103** (2008) 101301-1. https://doi.org/10.1063/1.2918987
5 S. P. Beeby, M. J. Tudor, and N. M. White: Meas. Sci. Technol. **17** (2006) R175. https://doi.org/10.1088/0957-0233/17/12/R01
6 P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green: Proc. The IEEE **96** (2008) 1457. http://doi.org/10.1109/JPROC.2008.927494
7 H.-C. Song, P. Kumar, D. Maurya, M.-G. Kang, W. T. Reynolds, D.-Y. Jeong, C.-Y. Kang, and S. Priya: 2017 J. Microelectromech. Syst. **26** (2017) 1226. http://doi.org/10.1109/JMEMS.2017.2728821
8 K. Morimoto, I. Kanno, K. Wasa, and H. Kotera: Sens. Actuators, A **163** (2010) 428. https://doi.org/10.1016/j.sna.2010.06.028
9 H. Liu, C. Lee, T. Kobayashi, C. J. Tay, and C. Quan: Microsyst. Technol. **18** (2012) 497. http://doi.org/10.1007/s00542-012-1424-1
10 Q. C. Tang, Y. K. Yang, and X. Li: Smart Mater. Struct. **20** (2011) 125011-1. http://doi.org/10.1088/0964-1726/20/12/125011
11 E. E. Aktakka and K. Najafi: IEEE J. Solid-State Circuits **49** (2014) 2017. http://doi.org/10.1109/JSSC.2014.2331953
12 E. Sardini and M. Serpelloni: Sens. Actuators, A **172** (2011) 475. https://doi.org/10.1016/j.sna.2011.09.013
13 A. R. M. Foisal, C. Hong, and G.-S. Chung: Sens. Actuators, A **182** (2012) 106. https://doi.org/10.1016/j.sna.2012.05.009
14 B. Yang and C. Lee: Microsyst. Technol. **16** (2010) 961. http://doi.org/10.1007/s00542-010-1059-z

15 P. Wang, K. Tanaka, S. Sugiyama, X. Dai, X. Zhao, and J. Liu: Microsyst. Technol. **15** (2009) 941. http://doi.org/10.1007/s00542-009-0827-0
16 J. C. Park, D. H. Bang, and J. Y. Park: IEEE Trans Magn. **46** (2010) 1937. http://doi.org/10.1109/TMAG.2010.2044757
17 Q. Fu and Y. Suzuki: J. Phys.: Conf. Ser. **476** (2013) 012112-1. http://doi.org/10.1088/1742-6596/476/1/012112
18 K. Tao, S. Liu, S. W. Lye, J. Miao, and X. Hu: J. Micromech. Microeng. **24** (2014) 065022-1. http://doi.org/10.1088/0960-1317/24/6/065022
19 K. Tao, S. W. Lye, J. Miao, L. Tang, and X. Hu: J. Micromech. Microeng. **25** (2015) 104014-1. http://doi.org/10.1088/0960-1317/25/10/104014
20 Y. Zhang, T. Wang, A. Luo, Y. Hu, X. Li, and F. Wang: Appl. Energy **212** (2018) 362. https://doi.org/10.1016/j.apenergy.2017.12.053
21 H. Asanuma, M. Hara, H. Oguchi, and H. Kuwano: AIP Adv. **6** (2016) 075206-1. https://doi.org/10.1063/1.4958884
22 P. Basset, D. Galayko, F. Cottone, R. Guillemet, E. Blokhina, F. Marty, and T. Bourouina: J. Micromech. Microeng. **24** (2014) 035001-1. http://doi.org/10.1088/0960-1317/24/3/035001
23 Y. Chiu and Y.-C. Lee: J. Micromech. Microeng. **23** (2013) 015012-1. http://doi.org/10.1088/0960-1317/23/1/015012
24 C. P. Le and E. Halvorsen: J. Micromech. Microeng. **22** (2012) 074013-1. http://doi.org/10.1088/0960-1317/22/7/074013
25 Y. Suzuki, D. Miki, M. Edamoto, and M. Honzumi: J. Micromech. Microeng. **20** (2010) 104002-1. http://doi.org/10.1088/0960-1317/20/10/104002
26 F. Wang and O. Hansen: Sens. Actuators, A **211** (2014) 131. https://doi.org/10.1016/j.sna.2014.02.027
27 A. Crovetto, F. Wang, and O. Hansen: J. Micromech. Microeng. **23** (2013) 114010-1. http://doi.org/10.1088/0960-1317/23/11/114010
28 T. Masaki, K. Sakurai, T. Yokoyama, M. Ikuta, H. Sameshima, M. Doi, T. Seki, and M. Oba: J. Micromech. Microeng. **21** (2011) 104004-1. http://doi.org/10.1088/0960-1317/21/10/104004
29 H. Koga, H. Mitsuya, H. Honma, H. Fujita, H. Toshiyoshi, and G. Hashiguchi: Micromachines **8** (2017) 293-1. https://doi.org/10.3390/mi8100293
30 H. Honma, H. Mitsuya, G. Hashiguchi, H. Fujita, and H. Toshiyoshi: Sens. Mater. **34** (2022) 1527. https://doi.org/10.18494/SAM3785
31 H. Honma and H. Toshiyoshi: IEEJ Trans. SM **142** (2022) 215. https://doi.org/10.1541/ieejsmas.142.215
32 H. Honma, Y. Tohyama, S. Ikeno, and H. Toshiyoshi: Sens. Mater. **32** (2020) 2475. https://doi.org/10.18494/SAM.2020.2821
33 P. D. Mitcheson, T. C. Green, E. M. Yeatman, and A. S. Holmes: J. Microelectromech. Syst. **13** (2004) 429. http://doi.org/10.1109/JMEMS.2004.830151
34 H. Honma, H. Mitsuya, G. Hashiguchi, H. Fujita, and H. Toshiyoshi: J. Micromech. Microeng. **28** (2018) 064005-1. https://doi.org/10.1088/1361-6439/aab514
35 H. Honma, Y. Tohyama, H. Mitsuya, G. Hashiguchi, H. Fujita, and H. Toshiyoshi: J. Micromech. Microeng. **29** (2019) 084002-1. https://doi.org/10.1088/1361-6439/ab2371
36 H. Honma, Y. Tohyama, H. Mitsuya, G. Hashiguchi, H. Fujita, and H. Toshiyoshi: J. Micromech. Microeng. **31** (2021) 125008-1. https://doi.org/10.1088/1361-6439/ac2e46
37 G. Hashiguchi, D. Nakanone, T. Sugiyama, M. Ataka, and H. Toshiyoshi: AIP Adv. **6** (2016) 035004-1. https://doi.org/10.1063/1.4943528
38 T. Nakanishi, T. Miyajima, K. Chokawa, M. Araidai, H. Toshiyoshi, T. Sugiyama, G. Hashiguchi, and K. Shiraishi: Appl. Phys. Lett. **117** (2020) 193902-1. https://doi.org/10.1063/5.0029012
39 Y. Ohata, T. Nakanishi, K. Chokawa, M. Araidai, T. Ishiguro, H. Mitsuya, H. Toshiyoshi, Y. Shibata, G. Hashiguchi, and K. Shiraishi: Appl. Phys. Lett. **121** (2022) 243903-1. https://doi.org/10.1063/5.0129247
40 J. Yeom, Y. Wu, J. C. Selby, and M. A. Shannon: J. Vac. Sci. Technol. B **23** (2005) 2319. https://doi.org/10.1116/1.2101678

About the Authors

Hiroaki Honma received his M.E. and Ph.D. degrees in electrical engineering from Toyohashi University of Technology, Aichi, Japan, in 2013 and 2016, respectively. He joined the Institute of Industrial Science (IIS) of The University of Tokyo in 2016 as a project researcher. Since 2020, he has been a project research associate with IIS. His research interests include optical MEMS, power MEMS, and CMOS-MEMS. (honma-hh@iis.u-tokyo.ac.jp)



Sho Ikeno received his B.S. degree from Sophia University, Japan, in 2018 and his M.S. degree from The University of Tokyo, Japan, in 2020. His research interests are in MEMS vibrational energy harvesters and fabrication techniques. (ikeno@iis.u-tokyo.ac.jp)

Hiroshi Toshiyoshi received his M.E. and Ph.D. degrees in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1993 and 1996, respectively. He joined the Institute of Industrial Science (IIS) of The University of Tokyo in 1996 as a lecturer. From 1999 to 2001, he was a visiting assistant professor at the University of California, Los Angeles, CA, USA. In 2002, he became an associate professor with IIS. From 2005 to 2008, he was the project leader of the Optomechatronics Project at Kanagawa Academy of Science and Technology, Kawasaki, Japan. Since 2009, he has been a professor with IIS. His research interests include optical and power MEMS.
(hiro@iis.u-tokyo.ac.jp)