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Ka-band Quadrature Quintupler for Wireless Sensors

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A Ka-band quadrature quintupler fabricated in the 90 nm CMOS process is demonstrated. The multiplier consists of quadrature regenerative frequency dividers, single-balanced mixers, triplers, and buffers. The quadrature regenerative frequency divider and mixer produce a $5f_o/3$ (f_o, the input signal of the quintupler) signal and the tripler output produces a $5f_o$ signal. This quintupler has a wide frequency range of 22.5–28.5 GHz, high input and output powers of 3.9 and 1.8–2.3 dBm, respectively, and a power consumption of 14.8 mW. The size of the multiplier is 0.99 mm^2. This quintupler can be used in Ka-band wireless sensors.

1. Introduction

Over the last ten years, the research on RF CMOS circuits has focused on the realization of a complete system-on-a-chip (SOC), which can reduce the cost and help to improve the performance of an RF system. An external receiver is difficult to fabricate for SOCs owing to the large size of the intermediate frequency (IF) filter. However, a direct-conversion receiver is a good alternative owing to its compact size. In a conventional Ka-band direct-conversion receiver,[1–3] a local oscillator (LO) is very close to the RF signal, and the digital systems at the rear of the receiver require orthogonal carriers for demodulation. Hence, the LO must provide an orthogonal signal to an IQ mixer (I refers to the real part and Q refers to the imaginary part) for frequency reduction. In general, an LO is produced by a frequency synthesizer, which is composed of a voltage-controlled oscillator (VCO) and a phase-locked loop (PLL). If the frequency synthesizer is operating in the Ka band, there are several problems. An oscillator operating in the Ka band requires a large current to produce a sufficient loop gain. Output power and phase noise deteriorate as frequency increases. The locking range becomes limited with increasing power consumption. To solve the above problems, reducing the operating frequency of the frequency synthesizer and cascading a quintupler can overcome the performance limitation of the synthesizer, as shown in Fig. 1. The common triplers are of the balanced type,[4] self-mixing type,[5] and injection-locked type.[6] The balanced type uses the nonlinear characteristics of the transistor itself to extract the tripler frequency signal. The disadvantages of this type are its low conversion efficiency and large chip area. The self-mixing

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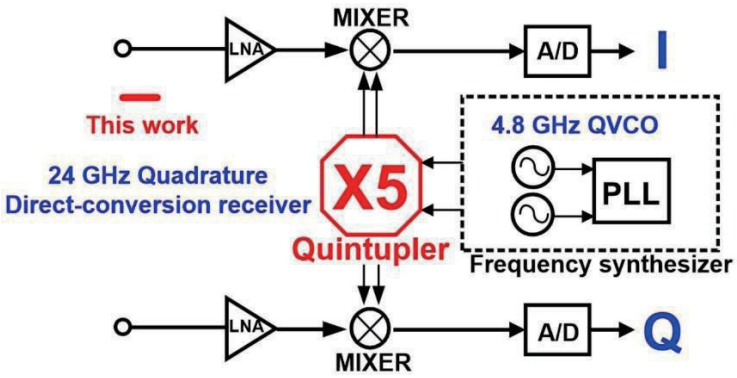

Fig. 1. (Color online) Structure of 24 GHz direct-conversion receiver with quintupler.

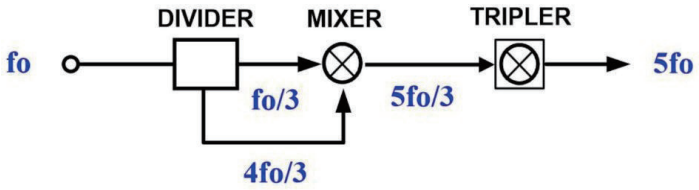

Fig. 2. (Color online) Block diagram of quintupler.

and injection-locked types are both differential triplers, making them unsuitable for a cascaded circuit with a hard driving feature. Figure 2 shows the quadrature regenerative frequency divider-by-three and the mixer used in this study to produce the $5f_o/3$ (f_o, the input signal of the quintupler) signal and the quadrature tripler subsequently used to raise the frequency to $5f_o$. Compared with the above architectures, in this work, we use a current-mode logic (CML) frequency divider, which has the characteristics of high output power and low input sensitivity. Also, the quintupler can provide high conversion efficiency and orthogonal injection and output, making it suitable for Ka-band direct-conversion receivers. In the future, this work can help to improve the performance of sensors applied to high-frequency usage.

2. Circuit Design and Implementation

Figure 3 shows the structure of the quadrature quintupler, which is composed of a quadrature regenerative divider, a single-balanced mixer, a tripler, and an output buffer. In the quadrature regenerative frequency divider, the CML loop divider reduces the $2f_o/3$ signal in half mixed with the band-pass filter and produces $f_o/3$ output signals with orthogonal phases (0, 90, 180, and 270°) that are then fed back to the RF port of a Gilbert mixer. On the other hand, the $4f_o/3$ signal produced by the clock-driven stage of the CML and the orthogonal output signal $f_o/3$ are mixed in the single-balanced mixer in the next stage. The IF port produces orthogonal $5f_o/3$ (0, 180, 90, and 270°) mixed signals, and finally, through the orthogonal tripler, we obtain $5f_o$ signals. To drive the 50 ohm loading resistance of the measurement instrument, two sets of differential amplifiers are used for the output buffer.

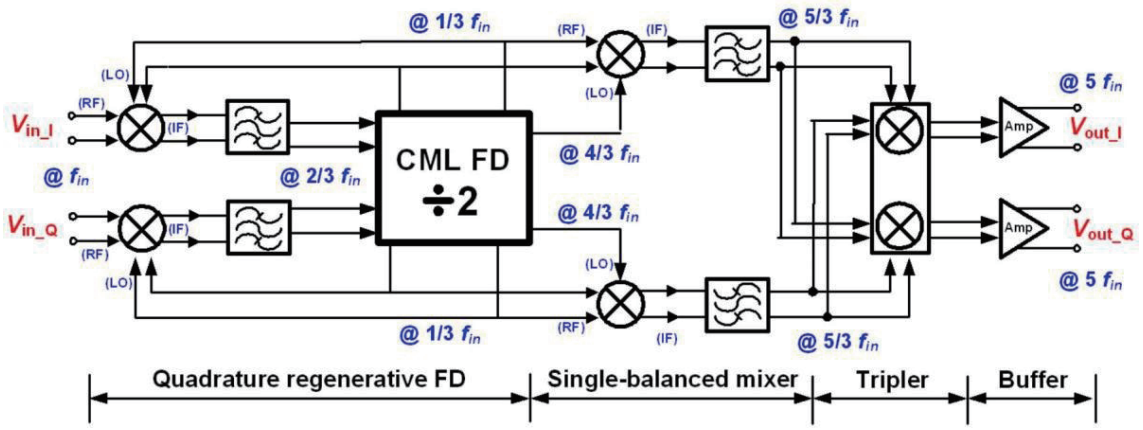

Fig. 3. (Color online) Structure of quadrature quintupler.

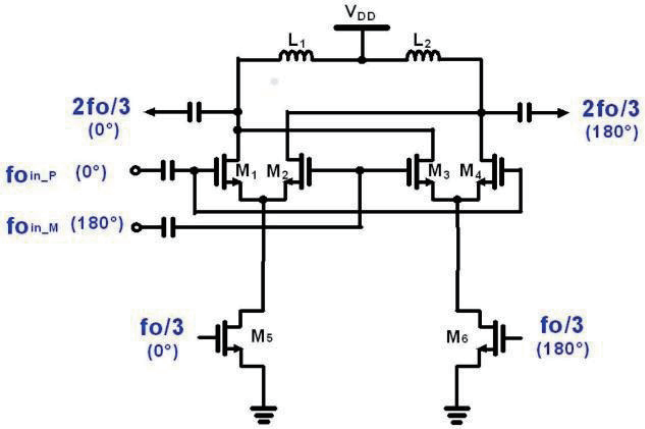

Fig. 4. (Color online) Schematic of Gilbert mixer and band-pass filter.

The schematic of the Gilbert mixer is shown in Fig. 4. It is divided into two parts: the RF transduction and the LO switch. The RF transduction consists of the source coupling pair (M5 and M6), while the LO switch consists of two sets of differential pairs (M1–M4), which are stacked above the transduction. Input signals (f_{oin_p}, f_{oin_m}) are injected into the LO switch, and the RF transduction source coupling pair is driven by feedback differential signals $f_o/3$ (0 and 180°). Each transistor of the transconductor stage is introduced once during the 1/3 cycle of the signal, and the LO switch pair is switched by the input signal. Finally, the IF output produces the $f_o \pm 1/3f_o$ output mixed signal, and then $2f_o/3$ signals are taken out through the band-pass filter. In addition, the RF stage has a transduction gain, allowing the subharmonic mixer to provide a conversion gain to the entire circuit to ensure that the feedback signal is not attenuated.

Figure 5 shows a schematic of the divider, which is composed of two CML circuits. The whole circuit provides a divisible function and orthogonal output signals. Figure 6 shows a schematic of the single-balanced mixer. It is used to mix the $f_o/3$ and $4f_o/3$ signals, and the band-pass filter removes the signals to produce a $5f_o/3$ signal. A schematic of the tripler is shown in Fig. 7. At the end of the circuit, a differential pair is formed by grounding the

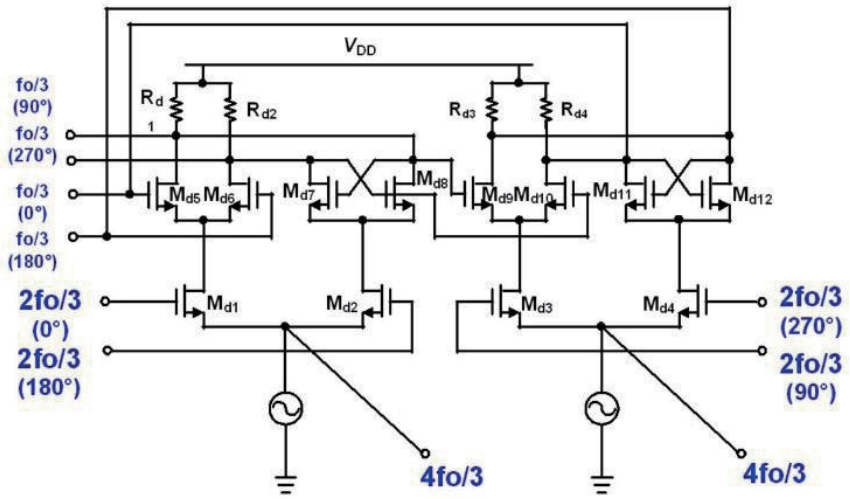

Fig. 5. (Color online) Schematic of divider.

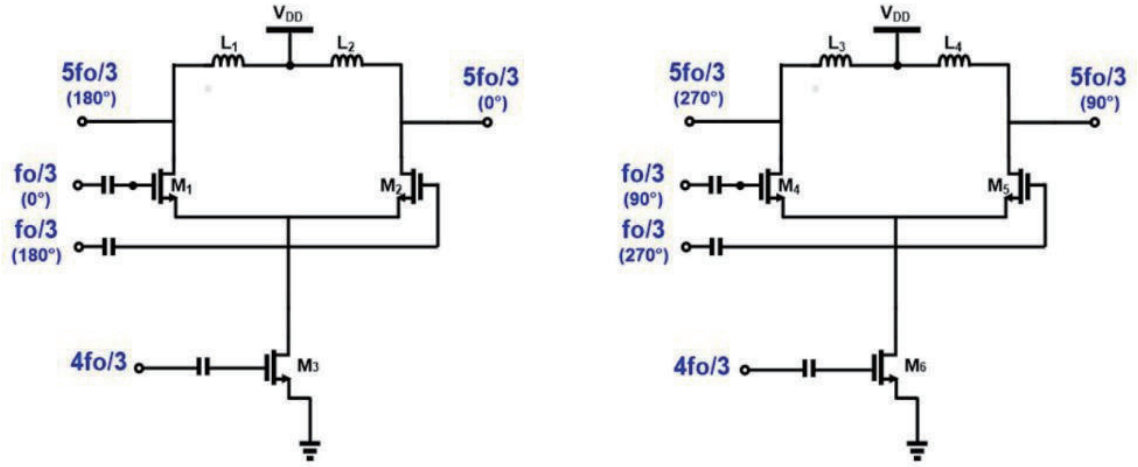

Fig. 6. (Color online) Schematic of single-balanced mixer and band-pass filter.

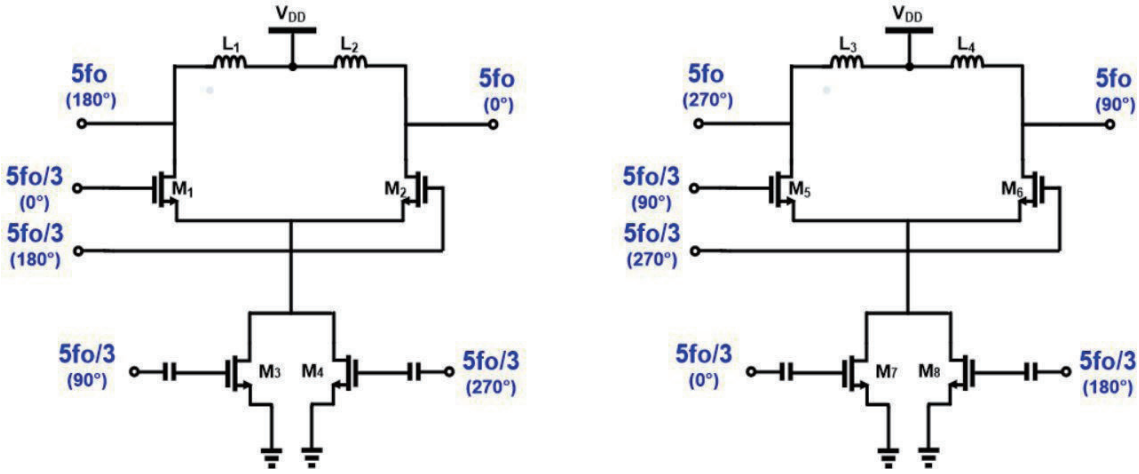

Fig. 7. (Color online) Schematic of tripler.

extremities of the two transistors, and a differential signal is the input because the differential pair only inputs the signal in a positive half cycle. A $10f_o/3$ signal is generated at the drain and then mixed with the input $5f_o/3$ signal. Finally, the $5f_o$ signal is taken out through the band-pass filter. Figure 8 shows the buffer stage. It consists of a pair of differential amplifiers. The buffer is designed for good impedance matching of the input and output, and the production of sufficient output power.

3. Results and Discussion

The layout of the quintupler is shown in Fig. 9. It is designed and fabricated in 90 nm CMOS technology and the chip area is 0.99 mm^2. Figure 10 shows the results of the post-layout simulation of output signal spectra at the output frequency of 25.5 GHz. The input signal has a frequency of 5.1 GHz with a power of 3.9 dBm, and the results show that the output power is 1.871–2.392 dBm. Figure 11 shows the input power versus output power curves at a fixed output signal frequency of 25.5 GHz. There is good agreement between the pre-layout and post-layout results. The results of the post-layout simulation of the output power versus output frequency curves at a fixed input power of 3.9 dBm are shown in Fig. 12. The amounts of

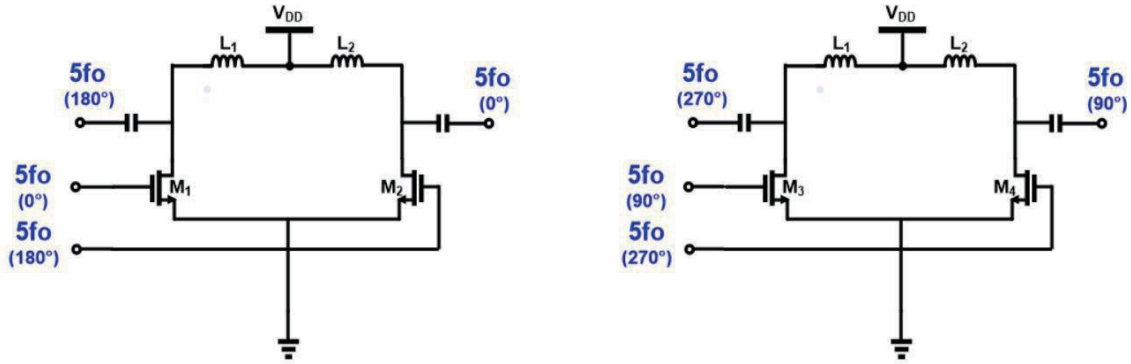

Fig. 8. (Color online) Schematic of buffer.

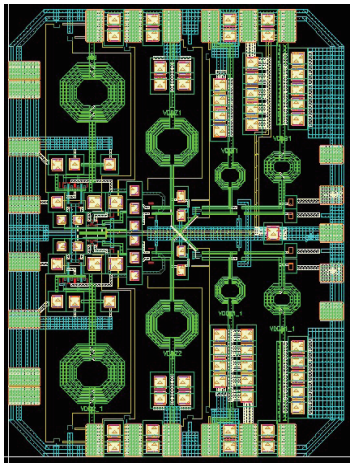

Fig. 9. (Color online) Chip layout.

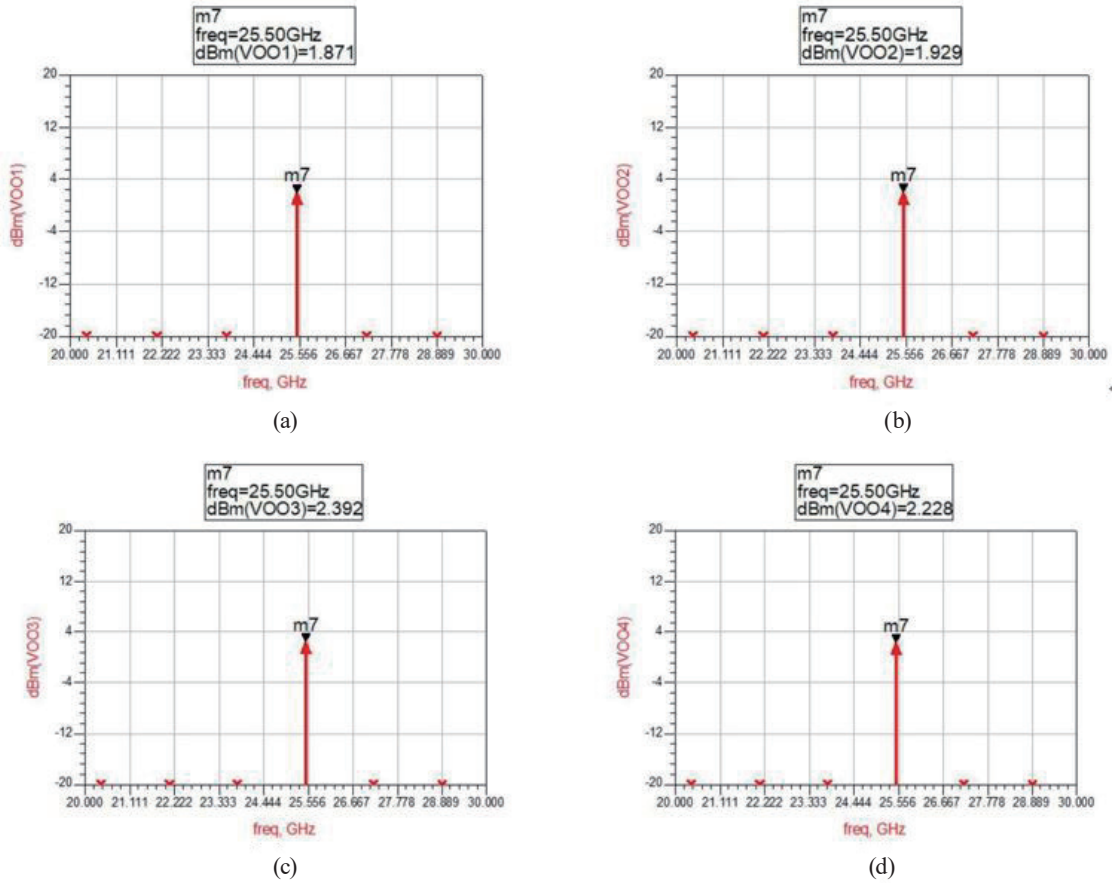

Fig. 10. (Color online) Results of post-layout simulation of output signal spectra (output signal of this component f_{out} = 25.5 GHz).

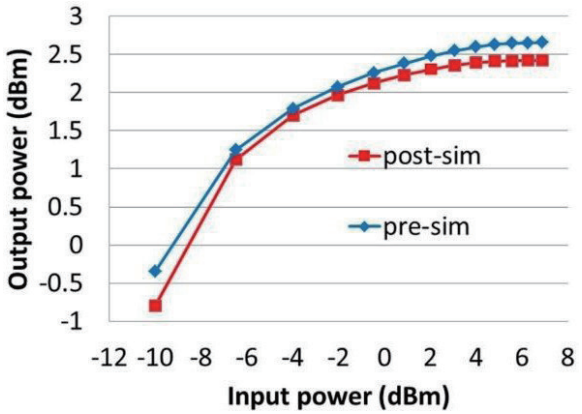

Fig. 11. (Color online) Input power versus output power curves (f_{out} = 25 GHz).

suppression of the fundamental, double, triple, and quadruple frequency output powers are 39, 20, 26, and 30 dB, respectively. These values show the excellent performance of the quintupler for sensor applications.

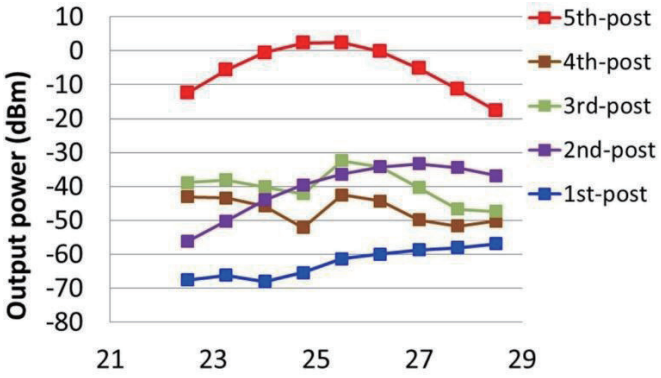

Fig. 12. (Color online) Output power versus output frequency curves obtained by post-layout simulation (input signal power P_{in} = 3.9 dBm).

Table 1
Comparison of reported multipliers.

Ref.	Technology	Multiplier Ratio	Frequency (GHz)	f_{in} (GHz)	P_{in} (dBm)	P_{out} (dBm)	VDD (V)	P_{diss} (mW)
5	0.18 µm CMOS	3	18–21.9	7	3	−6.5	1.8	18.8
6	0.18 µm CMOS	3	22.5–26.5	8.83	4	−9.5	1.5	2.95
7	0.18 µm CMOS	3	21.83–27.33	8.5	N/A	−6.5	1.8	11.1
8	0.18 µm CMOS	3	21.18–24.98	20	N/A	−3.6	1.8	9
This work	90 nm CMOS	5	22.5–28.5	5.1	3.9	1.8–2.3	1.2	14.8

P_{out} stands for the output signal power.
VDD stands for the bias voltage.
P_{diss} stands for the overall power consumption of the components.

The performance of the proposed multiplier compared with those reported in other papers is summarized in Table 1.[5–8] The proposed quintupler can provide quadrature input and output signals with a wide operating frequency range. It also has a high output power of 1.8–2.3 dBm with a power consumption of 14.8 mW.

4. Conclusion

A Ka-band quadrature quintupler fabricated in a 90 nm CMOS process has been presented. Its novel structure helps to remove the restrictions of conventional multipliers for receiver SOCs. The circuit has good performance for wireless communication systems and also for sensors.

Acknowledgments

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References

1 A. W. L. Ng, G. C. T. Leung, K.-C. Kwok, L. L. K. Leung, and H. C. Luong: IEEE J. Solid-State Circuits **41** (2006) 1236.
2 P. S. Weng and L. H. Lu: IEEE Microw. Wireless Compon. Lett. **22** (2012) 433.
3 Y. P. Ding and K. O. Kenneth: 2007 IEEE Symp. VLSI Circuits (2007) 264.
4 J. C. Chiu, C. P. Chang, M. P. Houng, and Y. H. Wang: IEEE Microw. Wireless Compon. Lett. **16** (2006) 19.
5 Y. T. Lo and J. F. Kiang: IEEE Microw. Wireless Compon. Lett. **22** (2012) 79.
6 M. C. Chen and C. Y. Wu: IEEE Microw. Wireless Compon. Lett. **56** (2008) 1869.
7 P. K. Tsai, C. Y. Liu, and T. H. Huang: IEEE Microw. Wireless Compon. Lett. **21** (2011) 492.
8 P. K. Tsai and T. H. Huang: IEEE Trans. Circuits Syst. II, Exp. Briefs **59** (2012) 199.