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Design of Planar Si Thermoelectric Generators with Phononic Crystal Patterning

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This paper presents the design and optimization of planar poly-Si thermoelectric generators (TEGs) for energy harvesting application. Temperature and electric potential distributions are simulated using material parameters, which were experimentally obtained from test structures, by the finite element method to evaluate the performance of TEGs. TEGs with unpatterned membranes or membranes with phononic crystal (PnC) nanostructures are investigated to evaluate the increase in power density by nanopatterning. The power density is increased by PnC nanopatterning with larger holes and the optimal bridge length decreases owing to a higher thermal resistance. The series of simulations shows that nanopatterning increases the power density 2.5 times at a smaller bridge length and is also advantageous from the viewpoint of mechanical strength.

1. Introduction

The concept of smart dust, which was followed by the internet of things (IoT) and ubiquitous computing, has been waiting for advanced technologies including energy harvesting for practical use in society for more than two decades. Thermoelectrics is one of the promising energy conversion technologies to realize an energy autonomous wireless sensor node for this purpose. Various thermoelectric materials were developed and their thermoelectric properties were investigated.[1–3] Silicon (Si) is the most practical material in electronics, but not for thermoelectric application at room temperature owing to its very high thermal conductivity.[4,5] However, researchers found that thermal conduction in nanostructures is much lower than in bulk and can be dramatically reduced by nanostructuring.[6–10] This is due to the enhancement of diffusive surface scattering, and the figure of merit ZT can be as high as 0.6 at room temperature in nanowires.[11,12] We investigate thermal phonon transport and heat conduction in

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nanostructured Si membranes, especially in membranes with PnC nanostructures, and develop planar Si thermoelectric devices.[13–17] A planar Si thermoelectric device can be fabricated using CMOS and micro-electromechanical system (MEMS) technologies, and is suitable for low-cost mass production.[18,19] In addition, the high reliability and environmental friendliness of Si are also advantageous for its widespread use in the environment and society. However, a planar device requires careful thermal design to generate sufficient electric power to drive microelectronic devices, because the temperature difference between the edges of a bridge structure of a thermoelectric membrane is normally small. Xie *et al.* designed and fabricated devices with peripheral cavity structures formed by CMOS and MEMS processes, and reported their high performance.[20,21] We also fabricate planar devices but with nanostructuring in Si membranes to increase the thermal resistance, which results in higher power generation.

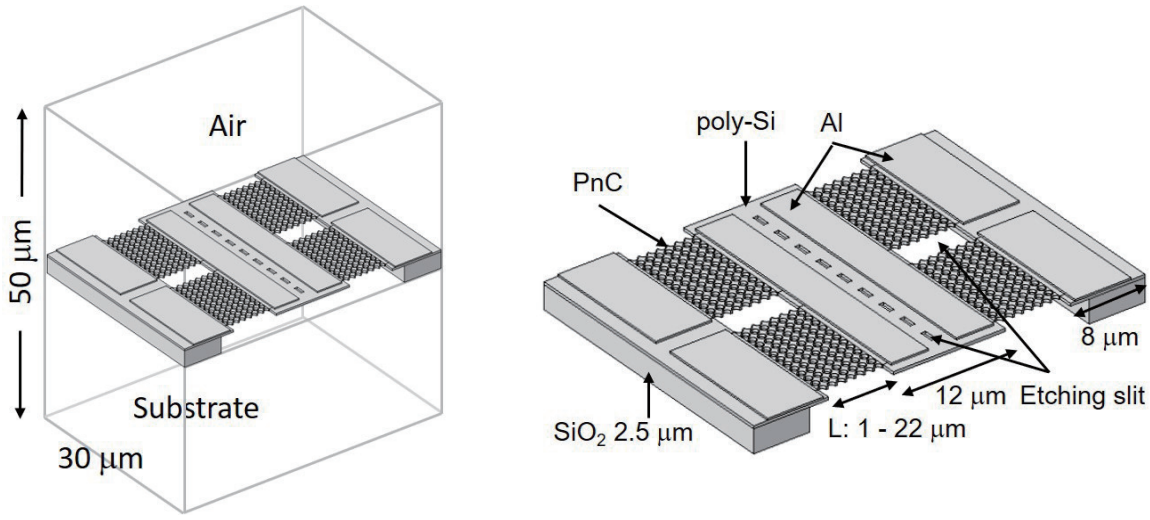
In this work, we report the design and simulated performance of planar Si thermoelectric devices with PnC nanostructures at room temperature based on parameters experimentally obtained using test structures. A thermal analysis was performed by the finite element method for various bridge lengths for optimization. We also investigated the importance of a substrate and compared the maximum power density at the optimum bridge length.

2. Simulation and System

In this section, the simulated structures and details of the simulation are explained. A three-dimensional model [50 × 30 × (30–72)] μm^3 was built as shown in Fig. 1(a). The simulated system is composed of device [Fig. 1(b)], air, and substrate parts. The boundary condition in the in-plane directions is periodic, but the upper plane of the air part and the bottom plane of the substrate part were fixed and their temperature difference (ΔT_{env}) was set at 10 K. In this simulation, the substrate was heated and heat escaped to the air via gas-solid heat exchange with natural convection. The thermal analysis in the solid was based on the diffusive model using Eq. (1) with the density ρ and heat capacity C_p,

$$\rho C_p \partial T / \partial t = \kappa \nabla^2 T. \tag{1}$$

The details and dimensions of the device part are shown in Fig. 1(b). Two pairs of n- and p-type poly-Si thermoelectric generators are fabricated on a SiO_2 sacrificial layer and connected by Al electrodes. PnC nanostructures are formed in the bridges and function as thermoelectric materials. Etching slits are formed in the central island part to isolate it from the substrate. The width of the bridge is 12 μm and the widths of the Al electrodes in the central island and on SiO_2 are 4 and 6 μm, respectively. The thicknesses of the poly-Si, Al electrode, SiO_2, air box, and substrate are 300 nm, 200 nm, 2.5 μm, 25 μm, and 25 μm, respectively. The material and other parameters are summarized in Table 1. Thermal analysis was performed by the finite element method for unpatterned membranes and membranes with PnCs with circular airholes with radii of 60, 100, and 120 nm. Each PnC has arrays of through holes aligned as a square lattice with a periodicity a of 300 nm in the suspended membrane. The electrical conductivity



(a) (b)

Fig. 1. (a) Schematic of the simulated system. (b) Details of the central part of the thermoelectric material with PnC patterning and Al electrodes.

Table 1
Parameters for n- and p-type poly-Si layers and the device used in the simulation.

Values for n-type/p-type	Membrane	PnC, r = 60 nm (r/a = 0.2)	PnC, r = 100 nm (r/a = 0.33)	PnC, r = 120 nm (r/a = 0.4)
σ (kS/m)	84/20	78/15	72/15	70/14
κ (W/mK)	11/18	4.0/8.7	2.5/7.5	2.0/7.2
S (μV/K)	−80/240			
ZT at 300 K	0.015/0.019	0.037/0.030	0.055/0.035	0.067/0.034
R_{cont} (Ωμm^2)	123/95			

σ, thermal conductivity κ, and Seebeck coefficient S were taken from our previous work,[14] and R_{cont} was taken from the literature.[20]

3. Simulation Results and Discussion

Temperature and electric potential distributions in the device part were simulated at an environmental temperature difference ΔT_{env} of 10 K (Fig. 2). The temperature distribution simulated for a structure with a PnC structure with airholes of r = 120 nm is shown in Fig. 2(a). The poly-Si part on the SiO_2 layer is hotter and the suspended central island is cooler, but the temperature difference between edges of the suspended thermoelectric material, ΔT_{mat}, is only 560 mK, which is only about 6% of ΔT_{env}. However, ΔT_{mat} is increased 3.2 times by PnC nanopatterning compared with the increase for an unpatterned membrane at the bridge length L = 7 μm.

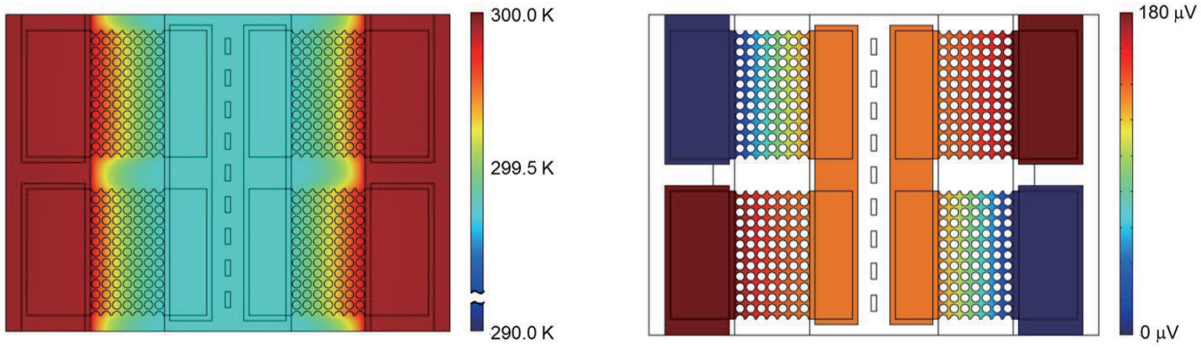


Fig. 2. (Color online) Examples of simulated (a) temperature and (b) electrical potential distributions in the thermoelectric device at ΔT_{env} = 10 K. The upper left and lower right bridges are p-type Si.

This finding indicates that the thermal design is very important for a planar device and emphasizes the importance of the high thermal resistance of the bridges. The simulation also gives the electrical potential distribution shown in Fig. 2(b). One pair of n- and p-type thermocouples generates 180 μV. The p-type Si bridge generates a higher thermoelectric voltage than the n-type Si bridge owing to its larger Seebeck coefficient. The open-circuit output voltage V_0 is given by $V_0 = (|S_n| + S_p)\,\Delta T_{mat}$, where S_n and S_p are the Seebeck coefficients for the n- and p-type poly-Si membranes, respectively.

The output power P_0 was estimated for unpatterned and PnC-nanopatterned membranes using various bridge lengths to optimize at a fixed bridge width of 12 μm. P_0 was calculated with load resistance given by the internal electrical resistance of one unit, R_{total}, and P_0 is given by

$$P_0 = \frac{V_0^2}{4R_{total}} = \frac{|S_n| + S_p}{4R_{total}} \Delta T_{mat}^2 . \tag{2}$$

Figure 3 shows the length dependence of the power density. When the bridge is short, ΔT_{mat} is low owing to a low thermal resistance. As the bridge becomes longer, ΔT_{mat} saturates and the foot print of one unit becomes unnecessarily large. Therefore, an optimum bridge length exists and continuously decreases as the thermal resistivity of the bridge increases, i.e., for a PnC nanostructure with larger holes. The maximum power density is increased 2.5 times by PnC patterning. This increase mainly stems from a larger ΔT_{mat} and an increased ZT, both of which result from thermal conductivity reduction by nanopatterning. In addition, a shorter bridge is better for practical use in a harsh environment because the bridge is mechanically more robust. Therefore, nanopatterning is an effective approach for improving the performance of a planar thermoelectric device as long as the process cost is low. The nanoholes used in this study are large enough to be fabricated by nanoimprint lithography, which enables low-cost large-area patterning.

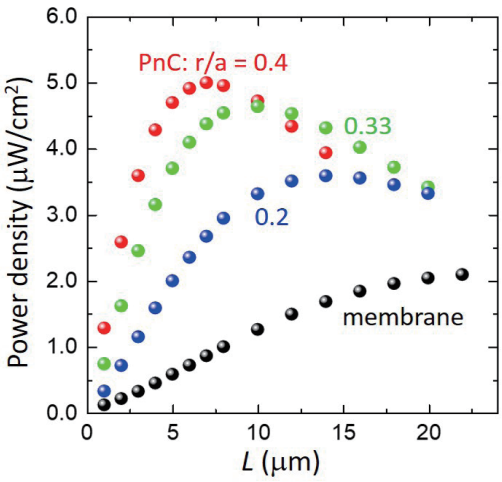


Fig. 3. (Color online) Simulated power densities at various bridge lengths (L) for TEGs with unpatterned membranes or membranes PnC-nanopatterned with different circular hole radii.

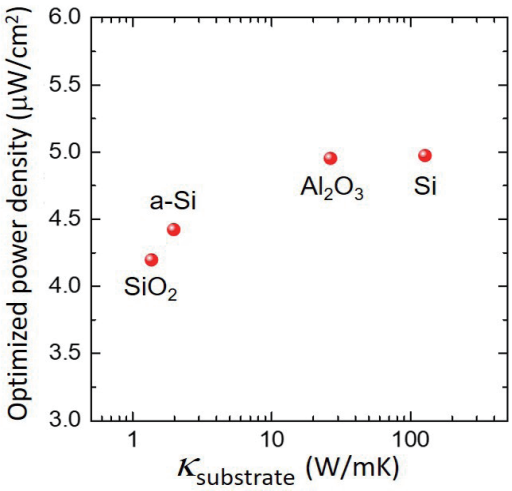


Fig. 4. (Color online) Calculated power density at each optimum bridge length with different substrates.

Finally, we investigated the importance of the substrate in the thermal design. As the thermal conductivities ($\kappa_{substrate}$) of the substrate, 1.38, 2, 27, and 130 W/mK were used as the values of SiO_2, amorphous Si (a-Si), Al_2O_3, and single-crystalline Si, respectively. Figure 4 shows that a higher power density is achieved with a thermally more conductive substrate. This is because a higher thermal gradient is formed in the thermoelectric material. It is also found that the power density does not change markedly above $\kappa_{substrate} \sim 10$ W/mK. This conclusion is also valid for a 500-μm-thick standard substrate. This is a useful finding because the substrate may not necessarily be thermally highly conductive, and thus low-cost ceramics can also be used as substrates.

4. Conclusions

Planar poly-Si thermoelectric devices were designed and their performance at room temperature was investigated by thermal analysis using the finite element method. The thermal design to increase the temperature difference between the edges of a suspended thermoelectric material is very important for the enhancement of power generation. PnC patterning with a periodicity of 300 nm reduces the thermal conductivity and results in a ZT improvement and a 2.5-fold power generation enhancement. The analysis also indicates that the substrate does not necessarily have to be thermally conductive; a low-cost substrate with a moderate thermal conductivity is available. The nanopatterning of a thermoelectric material by a low-cost and large-area fabrication process is a practical approach for obtaining high-performance planar thermoelectric devices.

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